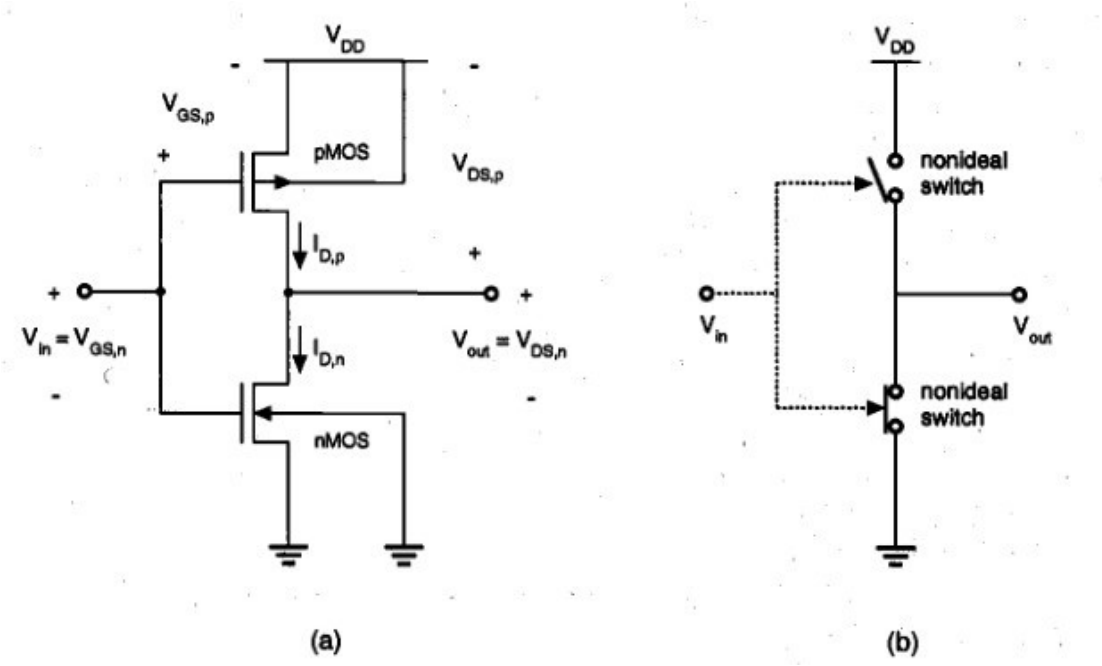
4. CMOS Inverter

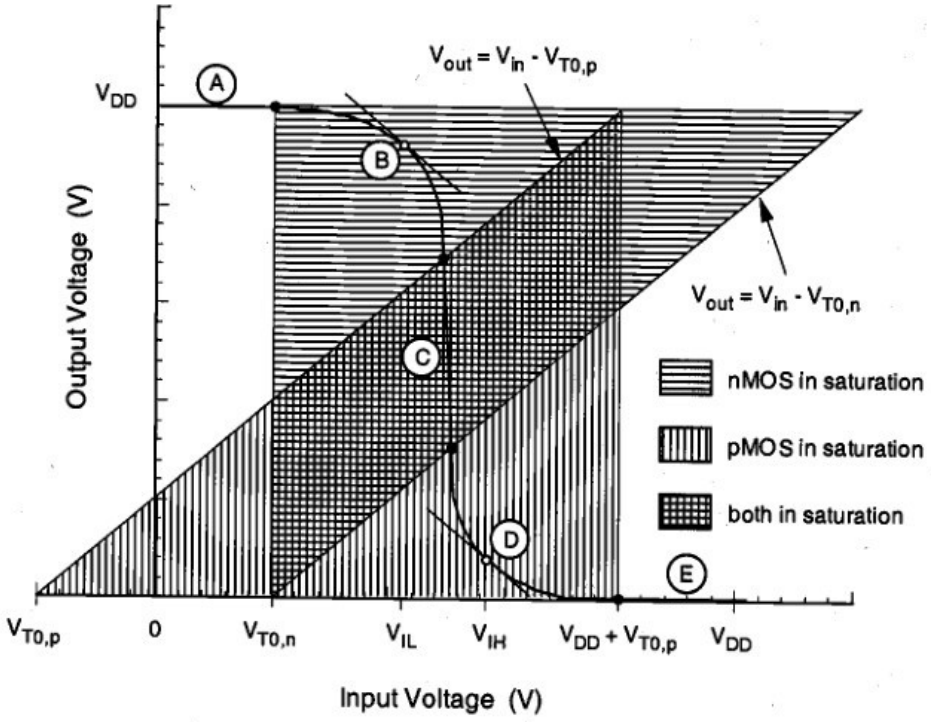
The CMOS inverter has two important advantages over the other inverter configurations.

The first and perhaps the most important advantage is that the steady-state power dissipation of the CMOS inverter circuit is virtually negligible, except for small power dissipation due to leakage currents. In all other inverter structures examined so far, a nonzero steady-state current is drawn from the power source when the driver transistor is turned on, which results in a significant DC power consumption.

The other advantages of the CMOS configuration are that the voltage transfer characteristic (VTC) exhibits a full output voltage swing between 0 V and VDD, and that the VTC transition is usually very sharp. Thus, the VTC of the CMOS inverter resembles that of an ideal inverter.



VTC Characteristic:



A :P Lin N Off

B : P Lin N Sat

C : P sat N Sat

D : P Sat N Lin

E :Poff NLin

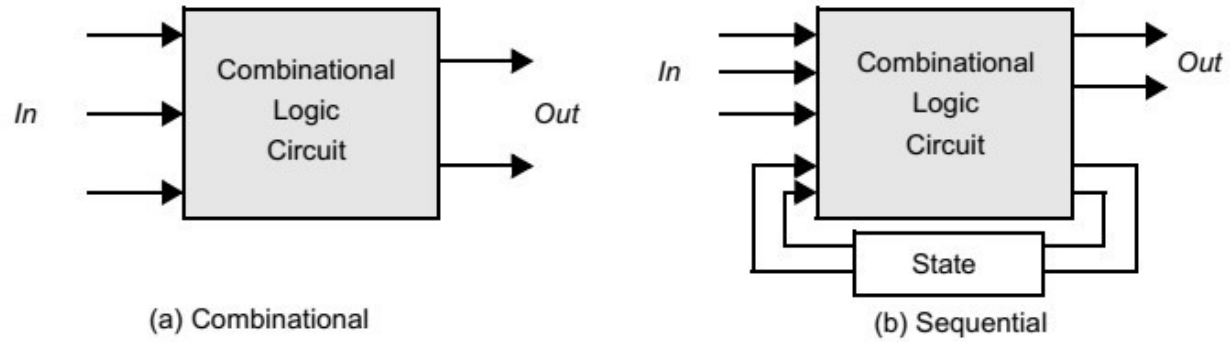
$$\frac{k_n}{k_p} = \frac{\mu_n C_{ox} \cdot \left(\frac{W}{L}\right)_n}{\mu_p C_{ox} \cdot \left(\frac{W}{L}\right)_p} = \frac{\mu_n \cdot \left(\frac{W}{L}\right)_n}{\mu_p \cdot \left(\frac{W}{L}\right)_p}$$

For Symmetric Inverter $V_{t0}=V_{t0n}=-V_{t0p}$: $K_R=1$

$$\frac{\left(\frac{W}{L}\right)_n}{\left(\frac{W}{L}\right)_p} = \frac{\mu_p}{\mu_n} \approx \frac{230\ \text{cm}^2/\text{V}\cdot\text{s}}{580\ \text{cm}^2/\text{V}\cdot\text{s}}$$

$$\left(\frac{W}{L}\right)_p \approx 2.5\left(\frac{W}{L}\right)_n$$

MOS Combinational Circuit



High level classification of logic circuits.

Different Logic Families:

1. **Static CMOS Design**
   a. Complementary CMOS
   b. Ratioed Logic
   c. Pass-Transistor Logic
2. **Dynamic CMOS Design**
   a. Domino logic
   b. NORA logic
   c. Zipper CMOS Circuits