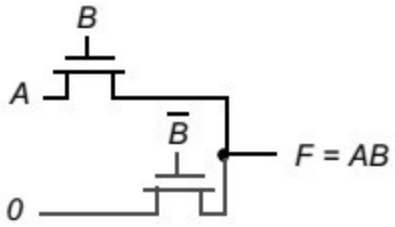
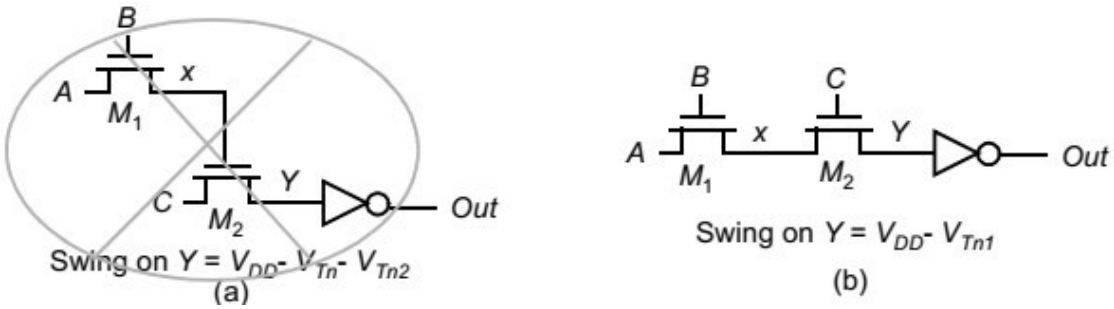
c. Pass-Transistor Logic

A popular and widely-used alternative to complementary CMOS is pass-transistor logic, which attempts to reduce the number of transistors required to implement logic by allowing the primary inputs to drive gate terminals as well as source/drain terminals. This is in contrast to logic families that we have studied so far, which only allow primary inputs to drive the gate terminals of MOSFETS.



Pass-transistor implementation of an AND gate

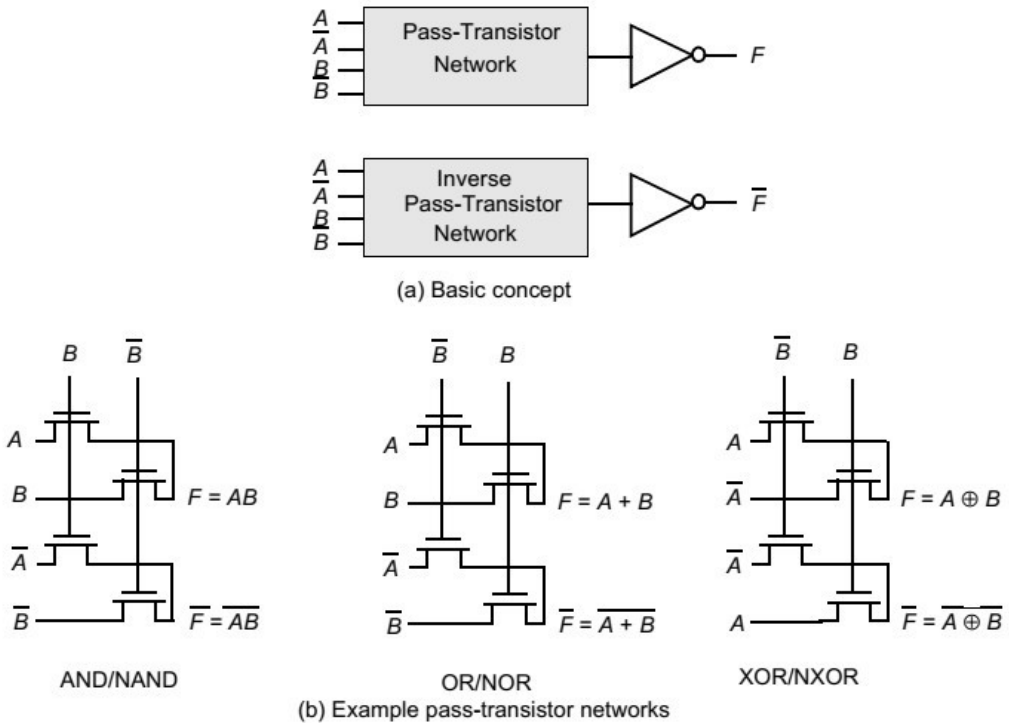
pass-transistor gates cannot be cascaded by connecting the output of a pass gate to the gate input of another pass transistor.



Pass transistor output (Drain/Source) terminal should not drive other gate terminals to avoid multiple threshold drops.

Differential Pass Transistor Logic:

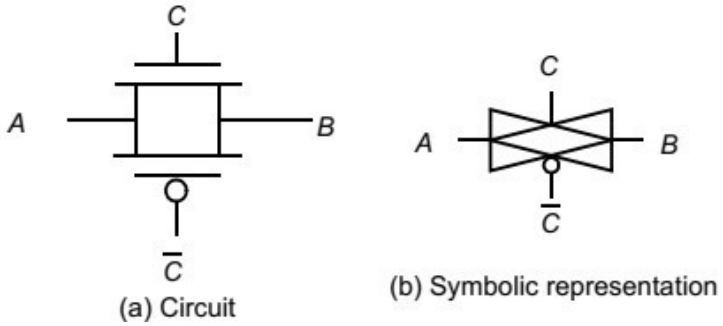
For high performance design, a differential pass-transistor logic family, called CPL or DPL, is commonly used. The basic idea (similar to DCVSL) is to accept true and complementary inputs and produce true and complementary outputs. A number of CPL gates (AND/NAND, OR/NOR, and XOR/NXOR) are shown in Figure.



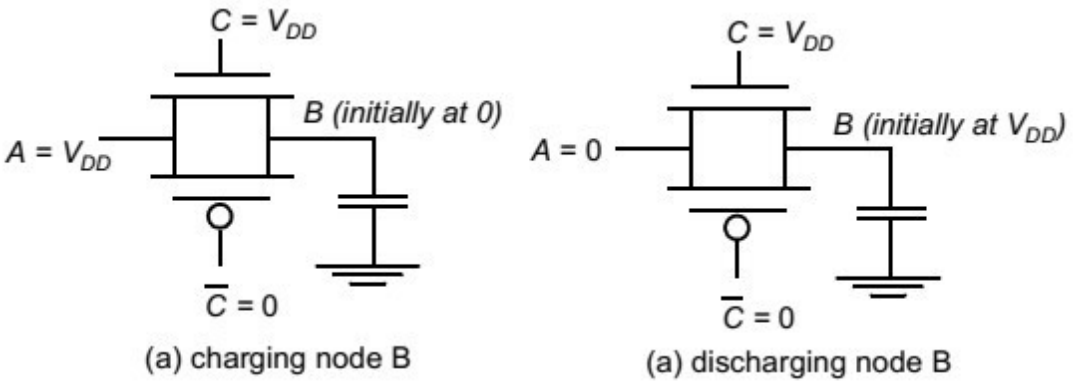
Complementary pass-transistor logic (CPL).

d. Transmission Gate Logic

The most widely-used solution to deal with the voltage-drop problem is the use of transmission gates. It builds on the complementary properties of NMOS and PMOS transistors: NMOS devices pass a strong 0 but a weak 1, while PMOS transistors pass a strong 1 but a weak 0. The ideal approach is to use an NMOS to pull-down and a PMOS to pull-up. The transmission gate combines the best of both device flavors by placing a NMOS device in parallel with a PMOS device .The control signals to the transmission gate (C and C) are complementary.



CMOS transmission gate

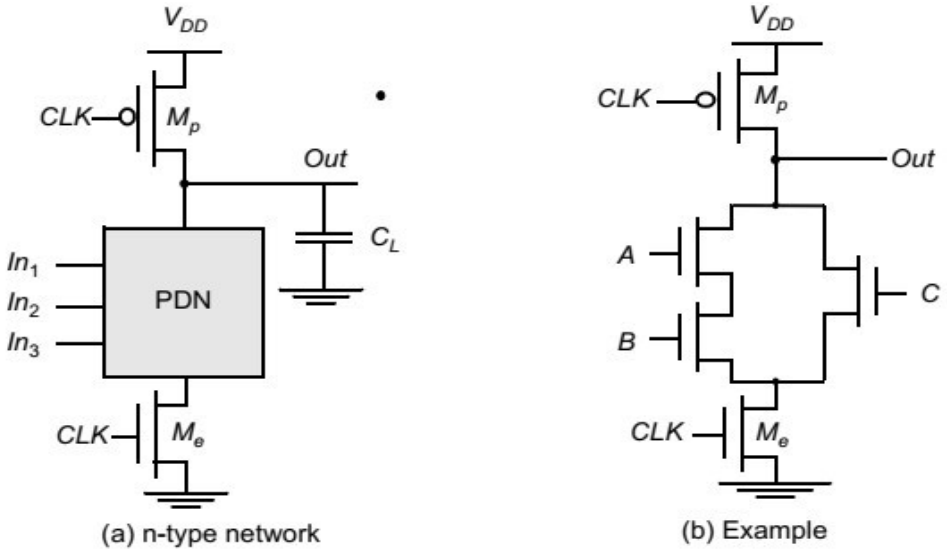


Transmission gates enable rail-to-rail switching

2. Dynamic CMOS Design

Dynamic circuit class, which relies on temporary storage of signal values on the capacitance of high-impedance circuit nodes. In this section, an alternate logic style called dynamic logic is presented that obtains a similar result, while avoiding static power consumption. With the addition of a clock input, it uses a sequence of precharge *a*nd conditional evaluation phases.

The basic construction of an (n-type) dynamic logic gate is shown in Figure. The PDN (pull-down network) is constructed exactly as in complementary CMOS. The operation of this circuit is divided into two major phases: precharge and evaluation, with the mode of operation determined by the clock signal CLK.



Basic concepts of a dynamic gate.