2. Dynamic CMOS Design

Dynamic circuit class, which relies on temporary storage of signal values on the capacitance of high-impedance circuit nodes. In this section, an alternate logic style called dynamic logic is presented that obtains a similar result, while avoiding static power consumption. With the addition of a clock input, it uses a sequence of precharge and conditional evaluation phases.

The basic construction of an (n-type) dynamic logic gate is shown in Figure. The PDN (pull-down network) is constructed exactly as in complementary CMOS. The operation of this circuit is divided into two major phases: precharge and evaluation, with the mode of operation determined by the clock signal CLK.

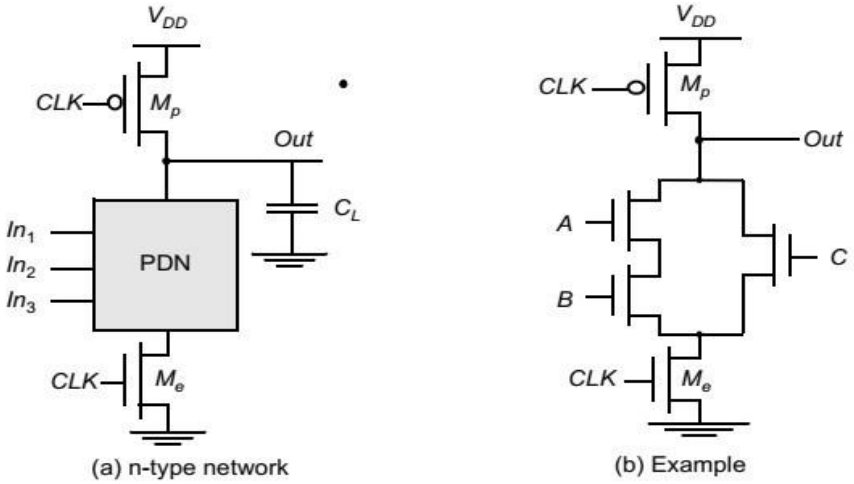


Fig. Basic concepts of a dynamic gate.

Precharge

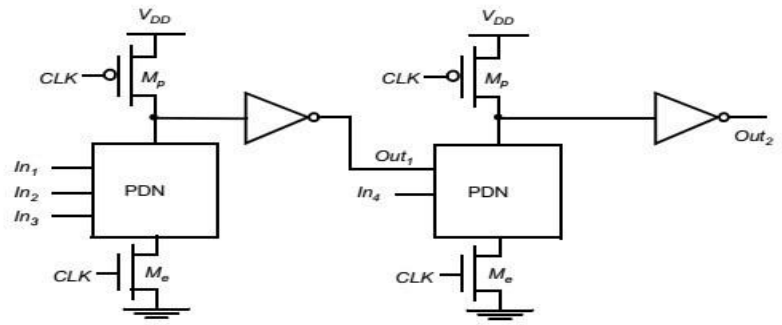
When CLK = 0, the output node Out is precharged to V_{DD} by the PMOS transistor Mp. During that time, the evaluate NMOS transistor Me is off, so that the pull-down path is disabled. The evaluation FET eliminates any static power that would be consumed during the precharge period (this is, static current would flow between the supplies if both the pulldown and the precharge device were turned on simultaneously).

Evaluation

For CLK = 1, the precharge transistor Mp is off, and the evaluation transistor Me is turned on. The output is conditionally discharged based on the input values and the pull-down topology. If the inputs are such that the PDN conducts, then a low resistance path exists between Out and GND and the output is discharged to GND.

a. Domino Logic

A Domino logic module consists of an n-type dynamic logic block followed by a static inverter. During precharge, the output of the n type dynamic gate is charged up to V_{DD}, and the output of the inverter is set to 0. During evaluation, the dynamic gate conditionally discharges, and the output of the inverter makes a conditional transition from 0 to 1.



DOMINO CMOS logic.

Remember that the problem in cascading conventional dynamic CMOS stages occurs when one or more inputs of a stage make a 1to 0 transition during the evaluation phase, as illustrated in Fig bellow.

On the other hand, if we build a system by cascading domino CMOS logic gates as shown in Fig. above, all input transistors in subsequent logic blocks will be turned off during the precharge phase, since all buffer outputs are equal to 0. During the evaluation phase, each buffer output can make at most one transition (from 0 to 1), and thus each input of all subsequent logic stages can also make at most one (0 to 1) transition. In a cascade structure consisting of several such stages, the evaluation of each stage ripples the next stage evaluation, similar to a chain of dominos falling one after the other. The structure is hence called domino CMOS logic.

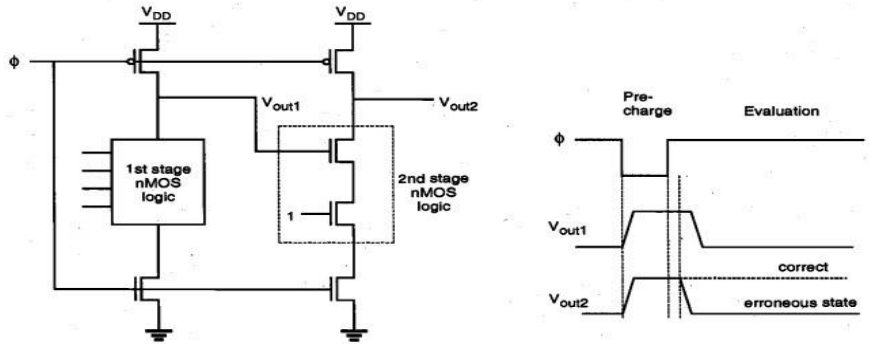
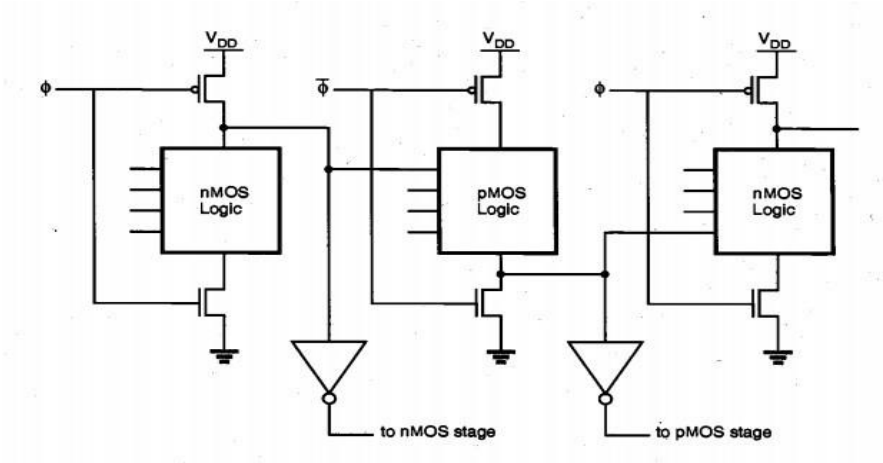


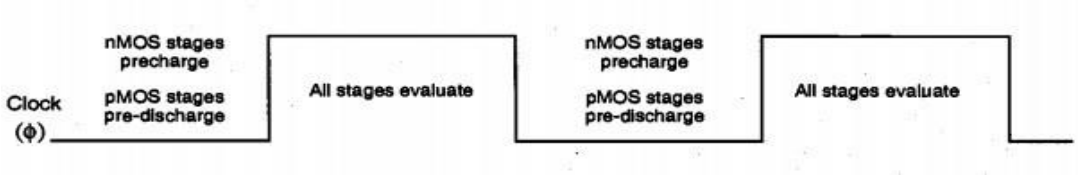
Fig. Illustration of the cascading problem in dynamic CMOS logic.

There are also some other limitations associated with domino CMOS logic gates. First, only noninverting structures can be implemented using domino CMOS. If necessary, inversion must be carried out using conventional CMOS logic. Also, charge sharing between the dynamic stage output node and the intermediate nodes of the n MOS logic block during the evaluation phase.

b. NORA CMOS Logic (NP-Domino Logic)

In domino CMOS logic gates, all logic operations are performed by the NMOS transistors acting as pull-down networks, while the role of PMOS transistors is limited to precharging the dynamic nodes. As an alternative and a complement to NMOS-based domino CMOS logic, we can construct dynamic logic stages using PMOS transistors as well. Consider the circuit shown in Fig., with alternating NMOS and PMOS logic stages.





- The advantage of NORA CMOS logic is that a static CMOS inverter is not required at the output of every dynamic logic stage. Instead, direct coupling of logic blocks is feasible by alternating nMOS and pMOS logic blocks.
- The second important advantage of NORA CMOS logic is that it allows pipelined system architecture.
- As in all dynamic CMOS structures, NORA CMOS logic gates also suffer from charge sharing and leakage. To overcome the dynamic charge sharing and soft- node leakage problems in NORA CMOS structures, a circuit technique called Zipper CMOS can be used.

a. Zipper CMOS Circuits

The basic circuit architecture of Zipper CMOS is essentially identical to NORA CMOS, with the exception of the clock signals. The Zipper CMOS clock scheme requires the generation of slightly different clock signals for the precharge (discharge) transistors and for the pull-down (pull-up) transistors. In particular, the clock signals which drive the PMOS precharge and NMOS discharge transistors allow these transistors to remain in weak conduction or near cut-off during the evaluation phase, thus compensating for the charge leakage and charge-sharing problems.

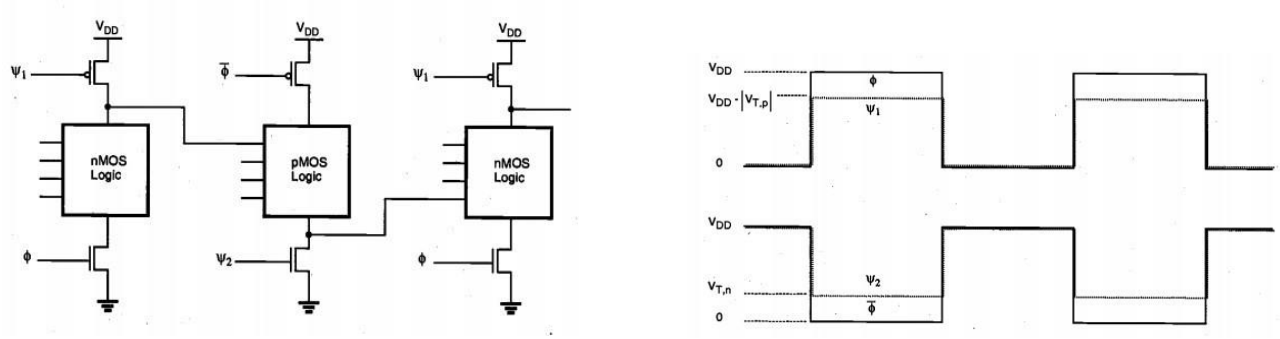


Fig. General circuit structure and the clock signals of Zipper CMOS