Switching improvement techniques in VLSI Circuits for Low Power Applications

In VLSI design flow there are various level of abstraction such that architecture level, Gate level, circuit level etc. So that improvement of switching techniques is possible at every level of abstractions.

The dynamic power of digital chips expressed by Equation is generally the largest portion of power dissipation. The $P = C.V^2.f$ equation consists of three terms: voltage, capacitance and frequency. Due to the quadratic effect of the voltage term, reducing the switching voltage can achieve dramatic savings. The easiest method to achieve this is to reduce the operating voltage of the CMOS circuit.

Reducing parasitic capacitance in digital design has always been a good way to improve performance as well as power. However, a blind reduction of capacitance may not achieve the desired result in power dissipation. The real goal is to reduce the product of capacitance and its switching frequency. Signals with high switching frequency should be routed with minimum parasitic capacitance to conserve power. Conversely, nodes with large parasitic capacitance should not be allowed to switch at high frequency.

For the sake of power dissipation, the techniques for reducing switching frequency have the same effect as reducing capacitance. Again, frequency reduction is best applied to signals with large capacitance. The techniques are often applied to logic level design and above. Those applied at a higher abstraction level generally have greater impact.

Leakage current, whether reverse biased junction or subthreshold current, is generally not very useful in digital design. However, designers often have very little control over the leakage current of the digital circuit. Fortunately, the leakage power dissipation of a CMOS digital circuit is several orders of magnitude smaller than the dynamic power. The leakage power problem mainly appears in very low frequency circuits or ones with "sleep modes" where dynamic activities are suppressed. Most leakage reduction techniques are applied at low-level design abstraction such as process, device and circuit design.

1. Circuits level

The power reduction techniques at the circuit-level are quite limited if compared with the other techniques at higher abstraction levels. At the circuit level, percentage power reduction in the teens is considered good. However, circuit techniques can have major impact because some circuits, especially in cell-based design, are repeated thousands of times on a chip. Therefore, circuit techniques with a small percentage improvement should not be overlooked.

i.) Transistor and Gate Sizing

transistor sizes are the most important factor affecting the quality, i.e., the area, performance and power dissipation, of a circuit. A large gate is required to drive a large load with acceptable delay but requires more power. In many ways, this is similar to the classical delay-area trade-off problem. Therefore, if we are not allowed to restructure the transistor network, the sizing for dynamic power reduction generally has the same goal as the area reduction problem. The basic rule is to use the smallest transistors or gates that satisfy the delay constraints. To reduce dynamic power, the gates that toggle with higher frequency should be made smaller.

This transistor sizing concept is illustrated in Figure for leakage power reduction. The inverter at the top is the reference design, with its transistor sizes, rise/fall delay and leakage power noted in the figure. The output of the inverter has a static probability of 0.99, which means that the leakage current is mainly determined by the N-transistor. Suppose that the output rising delay T_{rise} is critical. If we increase the channel length of the N-transistor, as shown by the bottom-left inverter, the leakage current improves without affecting the critical delay T_{rise} but the non-critical delay T_{fall} worsens. On the other hand, we can decrease the channel length of the P transistor to improve the critical delay without affecting the leakage.

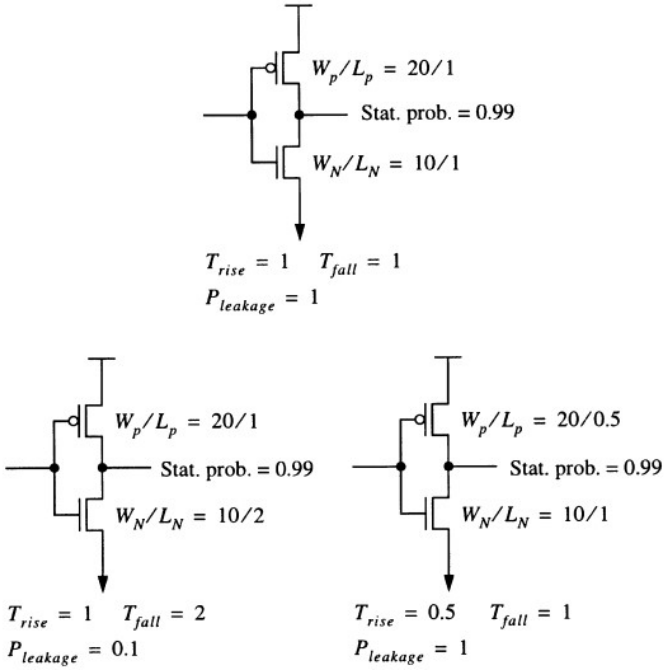
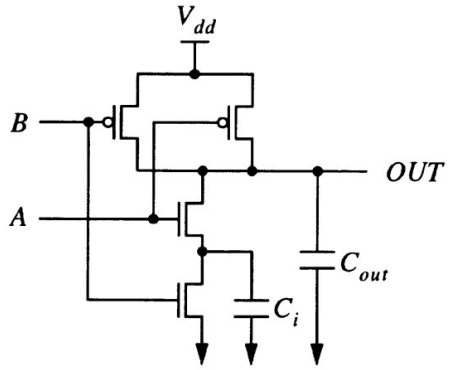


Fig. Transistor sizing for leakage power reduction or speed increase.

ii.) **Equivalent Pin Ordering**

Logically equivalent pins may not have identical circuit characteristics, which means that the pins have different delay or power consumption. Such property can be exploited for low power design. Consider a simple two-input CMOS NAND gate shown in Figure. We examine the condition when the input A is at logic high and the input B switches from logic low to high. Initially, capacitance C_{out} and C_i are charged to V_{dd} because the N transistor of input A is turned on and the output is at high. After the input B switches and all signals have stabilized, C_{out} and C_i are fully discharged to the ground. The charge stored in C_{out} and C_i has to pass through the N-transistor of input B to discharge. Consider another symmetrical situation in which the input B is at logic high and the input A switches from low to high. Before A switches, C_{out} is charged to V_{dd}..



To apply pin reordering, the designer needs to know the signal statistics at the gate inputs such as the switching frequencies and static probabilities. This can be observed from the logic simulation of a gate-level circuit. Without the probability information, the pin ordering technique cannot be applied. When performing pin reordering, the timing constraints of the design should not be violated.

iii.) **Network Restructuring and Reorganization**

For example, to compute the Boolean Function Y = A (B + C), we serialize the connection between the N-transistor of variable A and the network of (B + C), which is a parallel connection of two N-transistors. The P network is similarly constructed with the serial and parallel rule interchanged. The final circuit is shown in Figure.

As a general rule, transitions involving transistors closer to the output node have less delay and consume less energy. Therefore, the transition probabilities of each input need to be known to evaluate the circuits. In figure, a switch level simulation is used to choose the best circuit implementation. Power reduction up to 20% was reported using the transistor network restructuring technique.

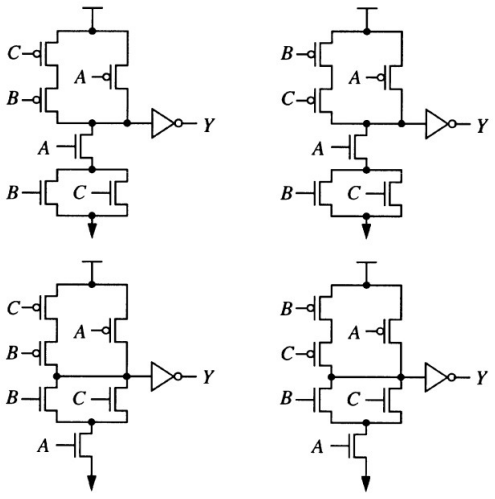


Fig. Four different circuit implementations of Y = A (B + C)