MOS Inverters: Switching Characteristics:

the capacitances C_d and are primarily due to gate overlap with diffusion, while C_{db} and C_{sb} are voltage-dependent junction capacitances. The 'capacitance component C is due to the thin-oxide capacitance over the gate area. In addition, we also consider the lumped interconnect capacitance C_{int}. which represents the parasitic capacitance contribution of the metal or polysilicon connection between the two inverters. It is assumed that a pulse waveform is applied to the input of the first-stage inverter. We wish to analyze the time-domain behavior of the first-stage output, V_{out}.

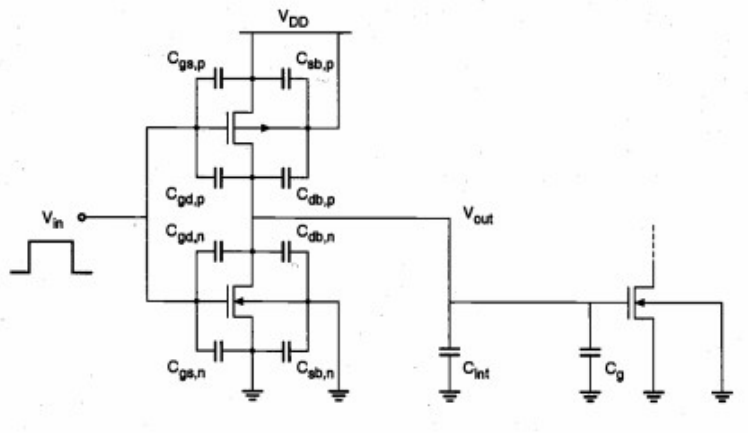


Fig. Cascaded CMOS inverter stages

The problem of analyzing the output voltage waveform is fairly complicated, even for this relatively simple circuit, because a number of nonlinear, voltage-dependent capacitances are involved. To simplify the problem, we first combine the capacitances seen in Fig. into an equivalent lumped linear capacitance, connected between the output node of the inverter and the ground. This combined capacitance at the output node will be called the load capacitance, C_{load}

$$C_{load} = C_{gd,n} + C_{gd,p} + C_{db,n} + C_{db,p} + C_{int} + C_g$$

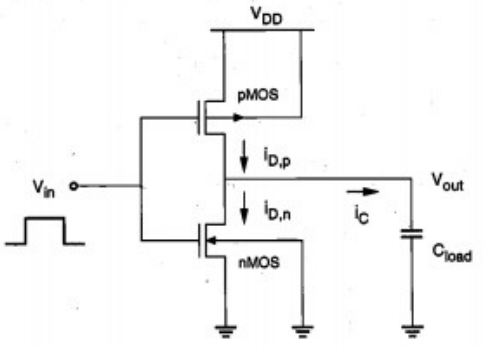
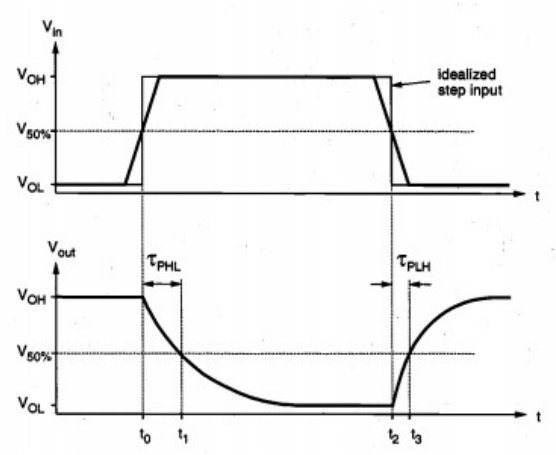


Fig. First-stage CMOS inverter with lumped output load capacitance.

Delay-Time Definitions:

The propagation delay times T_{PHL} and T_{pLH} determine the input-to-output signal delay during the high-to-low and low-to-high transitions of the output, respectively. By definition, T_{PHL} is the time delay between the $V_{50\%}$-transition of the rising input voltage and the V_{50} -transition of the falling output voltage. Similarly, T_{PLH} is defined as the time delay between the V_{50} -transition of the falling input voltage and the $V_{50\%}$-transition of the rising output voltage.



$$T_{PHL} = t_1 - t_0$$

$$T_{PLH} = t_3 - t_2$$

$$\tau_{PHL} = \frac{C_{load}}{k_n\left(V_{DD} - V_{T,n}\right)}\left[\frac{2V_{T,n}}{V_{DD} - V_{T,n}} + \ln\left(\frac{4\left(V_{DD} - V_{T,n}\right)}{V_{DD}} - 1\right)\right]$$

$$\tau_{PLH} = \frac{C_{load}}{k_p\left(V_{DD} - |V_{T,p}|\right)}\left[\frac{2|V_{T,p}|}{V_{DD} - |V_{T,p}|} + \ln\left(\frac{4\left(V_{DD} - |V_{T,p}|\right)}{V_{DD}} - 1\right)\right]$$

Calculation of Delay Times:

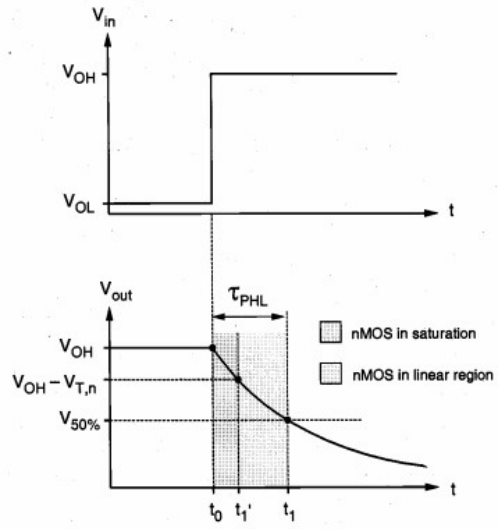


Fig. Input and output voltage waveforms during high-to-low transition.

$$C_{load}\frac{dV_{out}}{dt} = i_C = i_{D,p} - i_{D,n}$$

First, we consider the rising-input case for a CMOS inverter. Initially, the output Voltage is assumed to be equal to V_{OH}. When the input voltage switches from low (V_{OL}) to high (V_{OH}), the NMOS transistor is turned on and it starts to discharge the load 0 capacitance. At the same time, the PMOS transistor is switched off; thus,

$$C_{load}\frac{dV_{out}}{dt}=-i_{D,n}$$

$$i_{D,n}=\frac{k_n}{2}\left(V_{in}-V_{T,n}\right)^2$$
$$=\frac{k_n}{2}\left(V_{OH}-V_{T,n}\right)^2,\qquad for\quad V_{OH}-V_{T,n}<V_{out}\le V_{OH}$$

$$\int_{t=t_0}^{t=t_1'}dt=-C_{load}\int_{V_{out}=V_{OH}}^{V_{out}=V_{OH}-V_{T,n}}\left(\frac{1}{i_{D,n}}\right)dV_{out}$$

$$=-\frac{2\,C_{load}}{k_n\left(V_{OH}-V_{T,n}\right)^2}\int_{V_{out}=V_{OH}}^{V_{out}=V_{OH}-V_{T,n}}dV_{out}$$

$$t_1'-t_0=\frac{2\,C_{load}\,V_{T,n}}{k_n\left(V_{OH}-V_{T,n}\right)^2}$$

At t = t'$_1$, the output voltage will be equal to (V_{DD}-V_{Tn}) and the transistor will be at the saturation-linear region boundary. Next, consider the NMOS transistor operating in the linear region.

$$i_{D,n}=\frac{k_n}{2}\left[2\left(V_{in}-V_{T,n}\right)V_{out}-{V_{out}}^2\right]$$
$$=\frac{k_n}{2}\left[2\left(V_{OH}-V_{T,n}\right)V_{out}-{V_{out}}^2\right],\qquad for\quad V_{out}\le V_{OH}-V_{T,n}$$

$$\int_{t=t_1'}^{t=t_1}dt=-C_{load}\int_{V_{out}=V_{OH}-V_{T,n}}^{V_{out}=V_{50\%}}\left(\frac{1}{i_{D,n}}\right)dV_{out}$$

$$=-2\,C_{load}\int_{V_{out}=V_{OH}-V_{T,n}}^{V_{out}=V_{50\%}}\left(\frac{1}{k_n\left[2\left(V_{OH}-V_{T,n}\right)V_{out}-V_{out}^2\right]}\right)dV_{out}$$

$$t_1-t_1'=-\frac{2\,C_{load}}{k_n}\frac{1}{2\left(V_{OH}-V_{T,n}\right)}\ln\left(\frac{V_{out}}{2\left(V_{OH}-V_{T,n}\right)-V_{out}}\right)\Bigg|_{V_{out}=V_{OH}-V_{T,n}}^{V_{out}=V_{50\%}}$$

$$t_1-t_1'=\frac{C_{load}}{k_n\left(V_{OH}-V_{T,n}\right)}\ln\left(\frac{2\left(V_{OH}-V_{T,n}\right)-V_{50\%}}{V_{50\%}}\right)$$

$$\tau_{PHL}=\frac{C_{load}}{k_n\left(V_{OH}-V_{T,n}\right)}\left[\frac{2\,V_{T,n}}{V_{OH}-V_{T,n}}+\ln\left(\frac{4\left(V_{OH}-V_{T,n}\right)}{V_{OH}+V_{OL}}-1\right)\right]$$

For V_{OH} = V_{DD} and V_{OL}= 0, as is the case for the CMOS inverter

$$\tau_{PHL}=\frac{C_{load}}{k_n\left(V_{DD}-V_{T,n}\right)}\left[\frac{2\,V_{T,n}}{V_{DD}-V_{T,n}}+\ln\left(\frac{4\left(V_{DD}-V_{T,n}\right)}{V_{DD}}-1\right)\right]$$

In a CMOS inverter, the charge-up event of the output load capacitance for falling input transition is completely analogous to the charge-down event for rising input. When the input voltage switches from high (V_{OH}) to low (V_{OL}) the NMOS transistor is cut off, and the load capacitance is being charged up through the PMOS transistor. Following a very similar derivation procedure, the propagation delay time τ_{PLH} can be found as

$$\tau_{PLH}=\frac{C_{load}}{k_p\left(V_{OH}-V_{OL}-\left|V_{T,p}\right|\right)}\left[\frac{2\left|V_{T,p}\right|}{V_{OH}-V_{OL}-\left|V_{T,p}\right|}+\ln\left(\frac{2\left(V_{OH}-V_{OL}-\left|V_{T,p}\right|\right)}{V_{OH}-V_{50\%}}-1\right)\right]$$

For V_{OH} =V_{DD} and V_{OL}=0:

$$\tau_{PLH}=\frac{C_{load}}{k_p\left(V_{DD}-\left|V_{T,p}\right|\right)}\left[\frac{2\left|V_{T,p}\right|}{V_{DD}-\left|V_{T,p}\right|}+\ln\left(\frac{4\left(V_{DD}-\left|V_{T,p}\right|\right)}{V_{DD}}-1\right)\right]$$