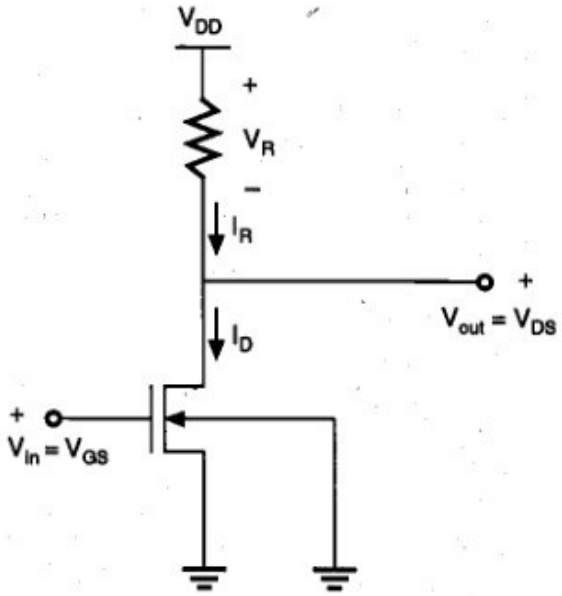
Inverters with different types of load:

1. **Resistive-Load Inverter:**

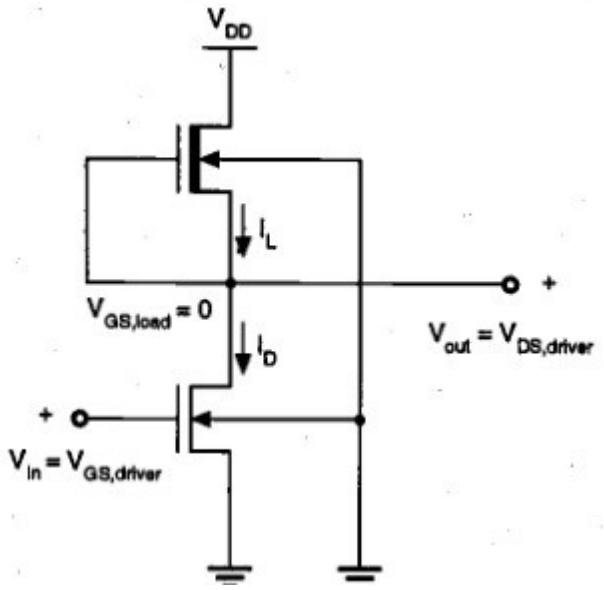


The average DC power consumption of the resistive-load inverter circuit is found by considering two cases, $V_{in} = V_{OL}$ (Low) and Vi. = V_{OH} (high). When the input voltage is equal to VOL, the driver transistor is in cut-off. Consequently, there is no steady-state current flow in the circuit ($I_D = I_R = 0$), and the DC power dissipation is equal to zero. When the input voltage is equal to VOW on the other hand, both the driver MOSFET and the load resistor conduct a nonzero current. Since the output voltage in this case is equal to VOL' the current drawn from the power supply can be found as:

$$I_D = I_R = \frac{V_{DD} - V_{OL}}{R_L}$$

The chip area occupied by the resistive-load inverter circuit depends on two parameters, the (W/L) ratio of the driver transistor and the value of the resistor RL. The area of the driver transistor can be approximated by the gate area, (WxL).

2. Depletion-load NMOS Inverter:



Several of the disadvantages of the enhancement-type load inverter can be avoided by using a depletion-type nMOS transistor as the load device.-The fabrication process for producing an inverter with an enhancement-type nMOS driver and a depletion-type nMOS load is slightly more complicated and requires additional processing steps, especially for the channel implant to adjust the threshold voltage of the load device.

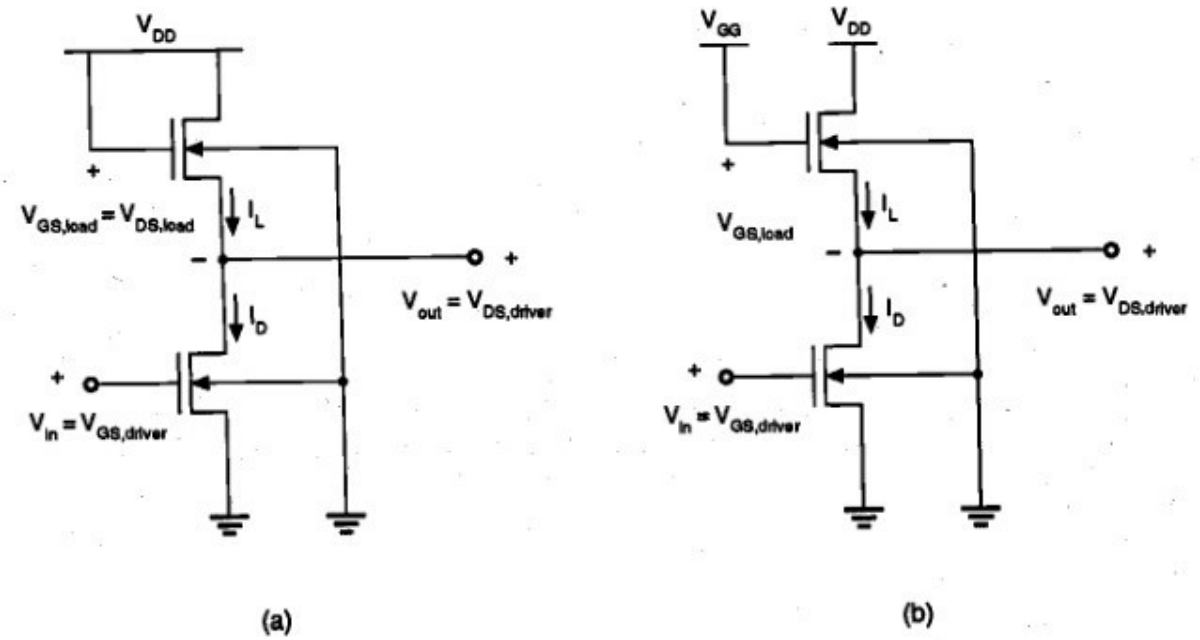
The resulting improvement of circuit performance and integration possibilities, however, easily justify the additional processing effort required for the fabrication of depletion-load inverters. The immediate advantages of implementing this circuit configuration are:

(i) sharp VTC transition and better noise margins,

(ii) (ii) single power supply, and

(iii) (iii) smaller overall layout area.

3. Enhancement-load NMOS Inverter:



(a) Inverter circuit with saturated enhancement-type nMOS load. (b) Inverter with linear enhancement-type load.

The circuit configurations of two inverters with enhancement-type load devices are depending on the bias voltage applied to its gate terminal, the load transistor can be operated either in the saturation region or in the linear region.

Both types of inverters have some distinct advantages and disadvantages from the circuit design point of view. The saturated enhancement-load inverter shown in Fig.(a) requires a single voltage supply and a relatively simple fabrication process, yet the V_{OH} level is limited to VDD - V_{TIoad}'

The load device of the inverter circuit shown in Fig. (b), on the other hand, is always biased in the linear region. Thus, the V_{OH} level is equal to V_{DD}, resulting in higher noise margins compared to saturated enhancement-load inverter. The most significant drawback of this configuration is the use of two separate power supply voltages. In addition, both types of inverter circuits suffer from relatively high stand-by (DC) power dissipation; hence, enhancement-load nMOS inverters are not used in any large-scale digital applications.