Power Consumption in CMOS Logic Gates:

Characterization of Logic Signals:

A logic signal only consists a waveform with zero-one voltage levels. The most precise way to describe a logic signal is to record all transitions of the signal at the exact times the transitions occur. if we only wish to know the frequency of the signal, there is no need to know the initial state and the exact switching times; the number of switches should be sufficient.

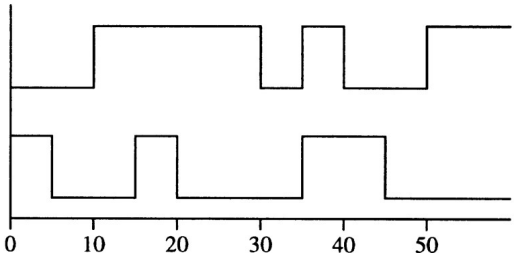

Fig. Two different logic signals with identical frequency.

Probability and Frequency:

The notion of switching frequency implies an observation period because it is meaningless to talk about the switching frequency of a signal without knowing the observation period. Regardless of the continuous or discrete signal model, the switching frequency f of a digital signal is defined as half the number of transitions per unit time, i.e.,

$$f = \frac{N(T)}{2T}$$

where N(T) is the number of logic transitions observed in the period T.

The static probability of a digital signal is the ratio of the time it spends in logic 1 (t_1) to the total observation time $t_0 + t_1$ expressed in a probability value between zero and one, i.e.,

$$p = \frac{t_1}{t_0 + t_1}$$

Propagation of Static Probability in Logic Circuits:

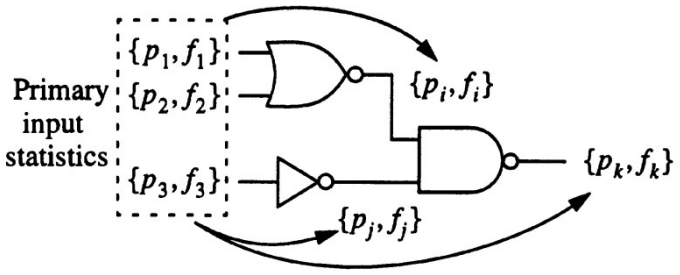

Fig. Propagation of statistical quantities in probabilistic power analysis.

We now derive the general formula for the propagation of static probability through an arbitrary Boolean function. Let y =f (x_1, ..., x_n) be an n-input Boolean function. Applying Shannon's decomposition with respect to x_i we have.

$$y = x_i f_{x_i} + \overline{x_i} f_{\overline{x_i}}$$

in which fx, ($f\overline{x}$) is the new Boolean function obtained by setting $x_i = 1$ ($x_i = 0$) in F(x_1 ,..., x_n). Let the static probabilities of the input variables be P(x_1),……, P(x_n). Since the two sum terms in the decomposition cannot be at logic 1 simultaneously, they are mutually exclusive. We can simply add their probabilities

$$P(y) = P(x_i f_{x_i}) + P(\overline{x_i} f_{\overline{x_i}}) = P(x_i)P(f_{x_i}) + P(\overline{x_i})P(f_{\overline{x_i}})$$

Example:

Let P(a), P(b) and P(c) be the input static probabilities. Find the output static probability of $y = ab + c$ by using the Shannon's decomposition method.

$$\begin{aligned} P(y) &= P(a)P(b+c) + P(\overline{a})P(c) \\ &= P(a)\,[P(b) + P(\overline{b})P(c)] + P(\overline{a})P(c) \\ &= P(a)P(b) + P(a)P(c) - P(a)P(b)P(c) + P(c) - P(a)P(c) \\ &= P(a)P(b) + P(c) - P(a)P(b)P(c) \end{aligned}$$

Logic Function: The transition activity is a strong function of the logic function being implemented. For static CMOS gates with statistically independent inputs, the static transition probability is the probability p_0 that the output will be in the zero state in one cycle, multiplied by the probability p_1 that the output will be in the one state in the next cycle:

$$\alpha_{0\to 1} = p_0 \bullet p_1 = p_0 \bullet (1 - p_0)$$

Signal Statistics: The switching activity of a logic gate is a strong function of the input signal statistics. Using a uniform input distribution to compute activity is not a good one since the propagation through logic gates can significantly modify the signal statistics. For example, consider once again a 2-input static NOR gate, and let pa and p_b be the probabilities that the inputs A and B are one. Assume further that the inputs are not correlated. The probability that the output node equals one is given by

$$P_1 = (1\text{-}P_a)\,(1\text{-}P_b)$$

Therefore, the probability of a transition from 0 to 1 is:

$$\alpha_{0\text{->}1} = p_0\, p_1 = (1\text{-}(1\text{-}p_a)\,(1\text{-}p_b))\,(1\text{-}p_a)\,(1\text{-}p_b)$$

	$\alpha_{0\to 1}$
AND	$(1 - p_A p_B)p_A p_B$
OR	$(1 - p_A)(1 - p_B)[1 - (1 - p_A)(1 - p_B)]$
XOR	$[1 - (p_A + p_B - 2p_A p_B)](p_A + p_B - 2p_A p_B)$

Output transition probabilities for static logic gates

Gate Level Power Analysis Using Transition Density:

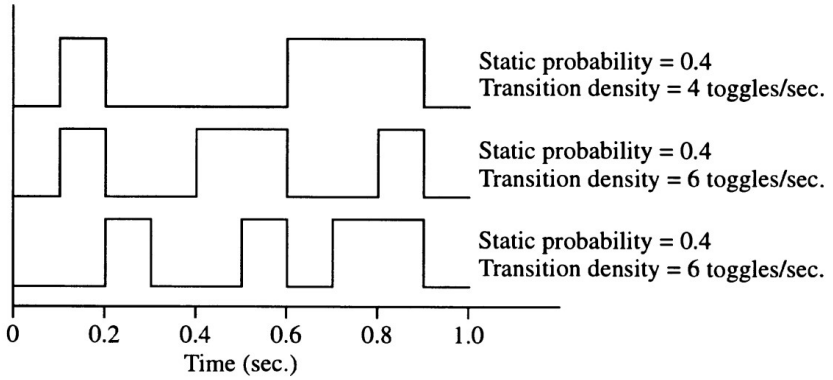

Fig. Static probabilities and transition densities of logic signals.

let's assume that Xi makes a transition from 1 to 0. According to the Shannon's decomposition equation, when $X_i = 1$, the output of y is f_{xi} Similarly when $X_i = 0$, the output is $f_{\bar{x}i}$. If a 1-to-0 or 0-to-1 transition in X_i, were to trigger a logic change in y, the Boolean functions. f_{xi} and $f_{\bar{x}i}$ must have different values. There are only two possible scenarios where this can happen:

1. $f_{x_i} = 1, f_{\bar{x}_i} = 0$; or
2. $f_{x_i} = 0, f_{\bar{x}_i} = 1.$

In other words, the exclusive-OR of the two functions has to be 1, i.e.,

$$f_{x_i} \oplus f_{\bar{x}_i} = 1$$

The exclusive-OR of the two functions is called the Boolean difference of y with respect to X_i denoted as

$$\frac{dy}{dx_i} = f_{x_i} \oplus f_{\bar{x}_i}$$

From the above discussion, it is clear that an input transition at xi propagates to the output y if and only if $dy/dx_i = 1$. Let P (dy/ dx) be the static probability that the Boolean function dy/dx_i evaluates to logic 1, and let $D(x_i)$ be the transition density of x_i Because of the uncorrelated inputs assumption, the output will have transition density of

$$P(\frac{dy}{dx_i}) D(x_i)$$

$$D(y) = \sum_{i=1}^{n} P(\frac{dy}{dx_i}) D(x_i)$$

1. For each internal node y of the circuit, find the Boolean function of the node with respect to the primary inputs.

2. Find the transition density D(y) of each node $y = f(x_1, \ldots, x_n)$ using Equation

3. Compute the total power with the formula

$$P = \sum_{\text{all nodes } y} 0.5 C_y V^2 D(y).$$

The power dissipation is a strong function of transistor sizing (which affects physical capacitance), input and output rise/fall times (which affects the short-circuit power), device thresholds and temperature (which affect leakage power), and switching activity. The dynamic power dissipation is given by $a_{0\text{-}1} C_L V_{DD}^2 f$. Making a gate more complex mostly affects the **switching activity** $a_{0\text{-}1}$, which has two components: a static component that is only a function of the topology of the logic network, and a dynamic one that results from the timing behavior of the circuit-the latter factor is also called glitching.