VLSI Design (BEC-41)
(Unit-2, Lecture-6)

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Power Dissipation of CMOS Inverters

- There are two types of power dissipation in CMOS circuits: dynamic and static:

Static power dissipation

Due to conduction of following currents:

- Subthreshold current
- Reverse biased PN-junction current
- Tunneling current

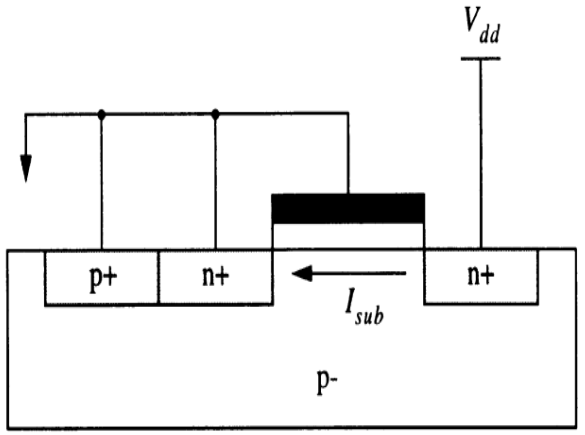
Dynamic power dissipation

- Due to charging and discharging of load capacitance
- Due to short circuit current

Static power dissipation

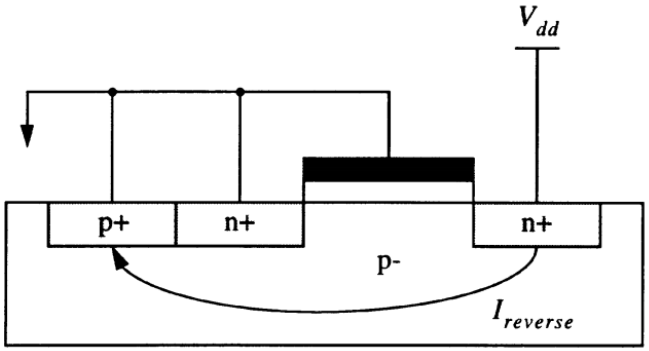
Subthreshold current

Even though a transistor is logically turned off, there is a non-zero leakage current through the channel at the microscopic level, as illustrated in Figure. This current is known as the subthreshold leakage because it occurs when the gate voltage is below its threshold voltage.



Reverse biased PN-junction current

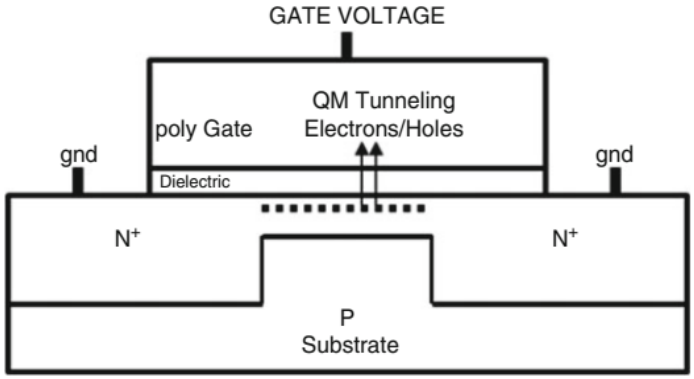
PN-junctions are formed at the source or drain of transistors because of a parasitic effect of the bulk CMOS device structure. The junction current at the source or drain of the transistor is picked up through the bulk or well contact. The magnitude of the current depends on the temperature, process, bias voltage and the area of the PN-junction.



Static power dissipation

Tunneling current

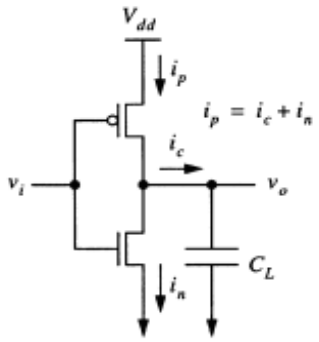
For MOSFETs with heavily doped channels and ultrathin oxide layers, the field in the oxide can reach very high values of MV/cm. The ultrathin oxide layer reduces the width of the energy barrier that separates the gate from the channel, thus making it easier for electrons/ holes to tunnel through the insulator layer as shown in Figure.

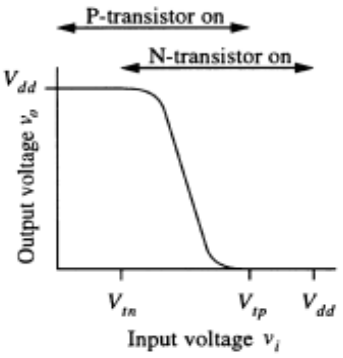


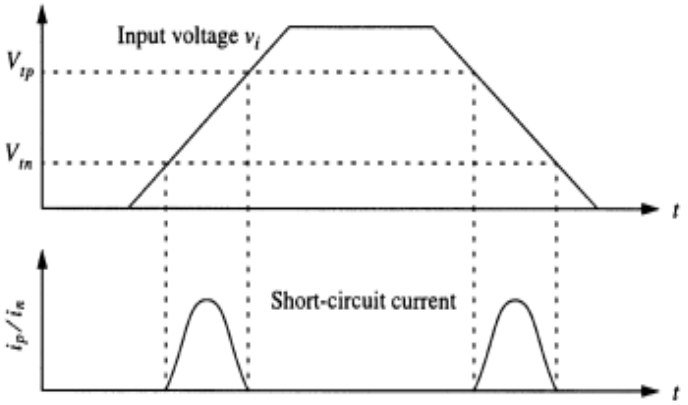
Dynamic power dissipation

Short circuit current

- CMOS inverter operating at V_{DD} with the transistor threshold voltages of V_{tn} and V_{tp} as marked on the transfer curve.
- When the input signal level is above V_{tn} the NMOS is turned on.
- Similarly, when the signal level is below V_{tp} the PMOS is turned on.
- When the input signal V_i switches, there is a short duration in which the input level is between V_{tn} and V_{tp} and both transistors are turned on.
- This causes a short-circuit current from V_{DD} to ground and dissipates power.







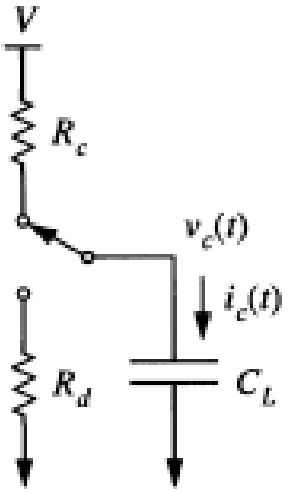
Dynamic power dissipation

Charging and discharging of load capacitance

- The most significant source of dynamic power dissipation in CMOS circuits is the charging and discharging of capacitance.
- Sometimes, capacitors are intentionally fabricated to achieve certain non-digital operations such as charge sharing and signal delay.
- However, most digital CMOS circuits do not require capacitors for their intended operations.
- The capacitance forms due to parasitic effects of interconnection wires and transistors. Such
- parasitic capacitance cannot be avoided and it has a significant impact on the power dissipation of the circuits.

Dynamic power dissipation

Charging and discharging of load capacitance (Continued..)



$$i_c(t) = C_L \frac{dv_c(t)}{dt}$$

- During the charging cycle from time t_0 to t_1 the energy E_s drawn from the voltage source is

$$E_s = \int_{t_0}^{t_1} V\, i_c(t)\, dt$$

- Initially the capacitor contains no charge and the voltage across its terminals is zero, i.e., $V_c(t_o) = 0$. Assume that the capacitor is fully charged at the end of the charging cycle, we have $V_c(t_1) = V$.

$$E_s = C_L V \int_{t_0}^{t_1} \frac{dv_c(t)}{dt}\, dt = C_L V \int_0^V dv_c = C_L V^2$$

- Part of the electrical energy E_s drawn from the voltage source is stored in the capacitor and the rest is dissipated as heat energy in the resistor Re. The energy E_{cap} stored in the capacitor at the end of the charging cycle is:

Dynamic power dissipation

Charging and discharging of load capacitance (Continued..)

$$E_{cap} = \int_{t_0}^{t_1} v_c(t)\, i_c(t)\, dt = C_L \int_{t_0}^{t_1} v_c(t) \frac{dv_c(t)}{dt} dt$$

$$= C_L \int_0^V v_c\, dv_c = \frac{1}{2} C_L V^2$$

- The energy *Ec* dissipated at *Rc* during charging is therefore

$$E_c = E_s - E_{cap} = \frac{1}{2} C_L V^2$$

- Now consider the discharging cycle from t_1 to t_2, we assume that the capacitor is fully discharged, i.e., $V_c(t1) = V$ and $V_c(t2) = 0$. The energy Ed dissipated in the discharge resistor R_d is

$$E_d = -\int_{t_1}^{t_2} v_c(t)\, i_c(t)\, dt = -C_L \int_V^0 v_c(t)\, dv_c = \frac{1}{2} C_L V^2$$

- Ed is exactly equal to the energy stored in the capacitance at the beginning of the discharging cycle. *If* we charge and discharge the capacitance at the frequency of f cycles per seconds, the power dissipation of the system is

$$P = E_s f = C_L V^2 f$$