UNIT-1

MOS INVERTER

Introduction:

Inverter is fundamental logic gate uses single input.

Basic principles employing in design and analysis of inverter can be directly applied on complex gates.

Therefore, inverter design forms basis for digital circuits.

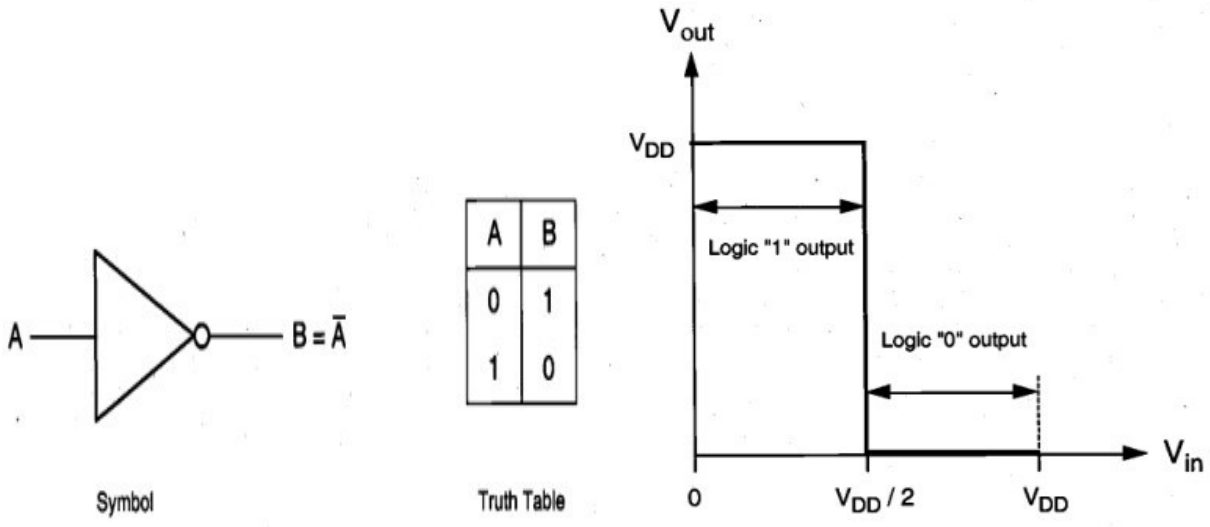
First we start with DC Characteristics.

The DC response is Ultra Low Frequency response of the Circuit.

When you are at a logic low or high before switching, it is a DC condition.

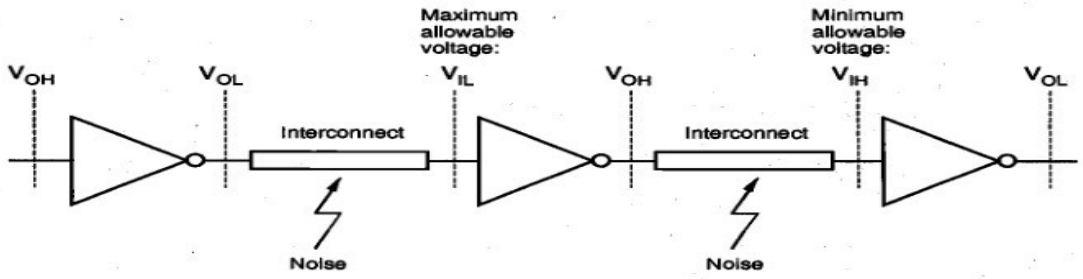
The transient can be thought of as a perturbation of the DC

Since valid logic levels are a range of voltages, it is a tolerant system.



Voltage transfer characteristic (VTC) of the ideal inverter

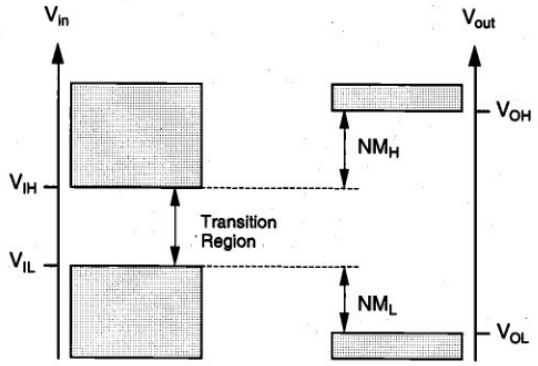
Noise Immunity and Noise Margins:



- Output signal is transmitted through interconnect to next inverter.
- Interconnects are prone to noise. Suppose output of 1st inverter is perturbed to a level higher than V_{IL}. Then this can not predict correct output of 2nd inverter.

- Thus, V_{IL} is maximum allowable input voltage which is low enough to ensure '1' output.
- Similarly argument for V_{IH}.

- Noise tolerance or Noise Margins and denoted by NM. Two noise margins will be defined for low signal level as NM_L and high signal level as NM_H :



$$N_{ML} = V_{IL} - V_{OL}$$

$$N_{MH} = V_{OH} - V_{IH}$$

Justification for V_{IL} and V_{IH}:

$$V_{out} = f(V_{in});\ V'_{out} = f(V_{in} + \Delta V_{noise})$$

$$V'_{out} = f(v_{in}) + \frac{dV_{out}}{dV_{in}} \Delta V_{noise}$$

Critical Parameters for Inverter design:

V_{OH}: Maximum output voltage when the output level is logic " 1"

V_{OL}: Minimum output voltage when the output level is logic "0"

V_{IL}: Maximum input voltage which can be interpreted as logic "0"

V_{IH}: Minimum input voltage which can be interpreted as logic " 1"

Power and Area Consideration:

- The DC power dissipation of an inverter is defined as

$$\mathbf{P_{DC} = V_{DD}.\ I_{DC}}$$

- Current depends upon input and output voltage levels. Assume input voltage level 50% is at logic '0' and 50% at logic '1'.

$$P_{DC} = \frac{V_{DD}}{2} \cdot \left[I_{DC}(V_{in} = low) + I_{DC}(V_{in} = high) \right]$$

- To reduce chip area, one has to reduce the size of transistor i.e. gate area (W x L). Thus keep W/L ratio close to unity.