VLSI Design (BEC-41)
(Unit-2, Lecture-2)

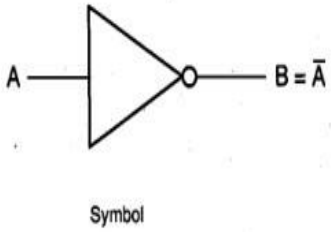
Presented By:

Prof. R. K. Chauhan

Department of Electronics and Communication Engineering

MOS INVERTER

- Inverter is fundamental logic gate uses single input.
- Basic principles employing in design and analysis of inverter can be directly applied on complex gates.
- Therefore, inverter design forms basis for digital circuits.
- First we start with DC Characteristics. The DC response is Ultra Low Frequency response of the Circuit.
- When you are at a logic low or high before switching, it is a DC condition.
- The transient can be thought of as a perturbation of the DC Since valid logic levels are a range of voltages, it is a tolerant system.



Symbol

A	B
0	1
1	0

Truth Table

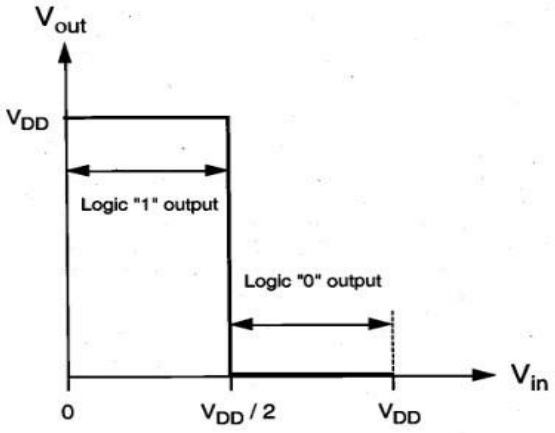
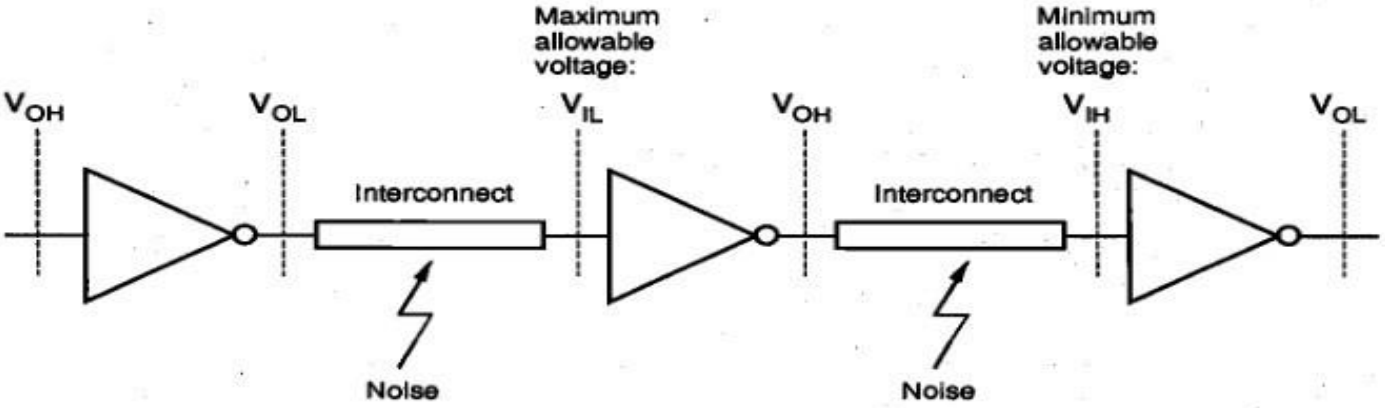


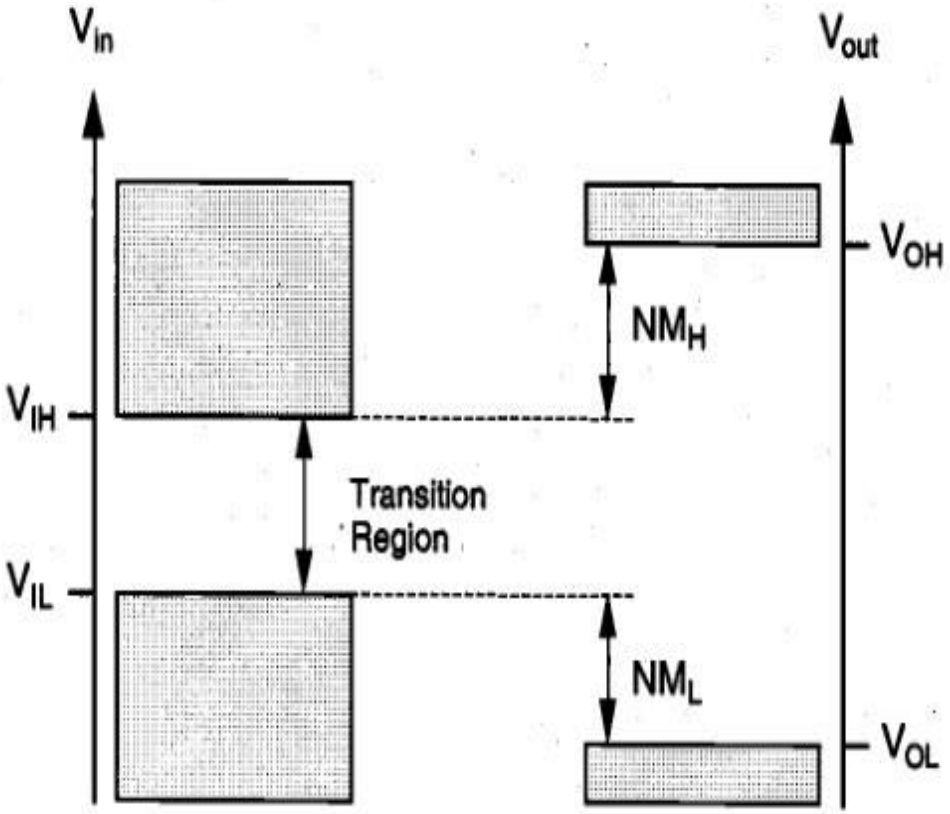
Fig. Voltage transfer characteristic (VTC) of the ideal inverter

Noise Immunity and Noise Margins



- Output signal is transmitted through interconnect to next inverter.
- Interconnects are prone to noise. Suppose output of 1st inverter is perturbed to a level higher than V_{IL}. Then this can not predict correct output of 2nd inverter.
- Thus, V_{IL} is maximum allowable input voltage which is low enough to ensure '1' output.
- Similarly argument for V_{IH}.
- Noise tolerance or Noise Margins and denoted by NM. Two noise margins will be defined for low signal level as NM_L and high signal level as NM_H

Noise Immunity and Noise Margins



$$N_{ML} = V_{IL} - V_{OL}$$

$$N_{MH} = V_{OH} - V_{IH}$$

- Noise tolerance or Noise Margins and denoted by NM.
- Two noise margins will be defined for low signal level as NM_L and high signal level as NM_H

Noise Immunity and Noise Margins

- If the input signal is perturbed from its nominal value because of external influences, such as noise:

$$V_{out}' = f\left(V_{in} + \Delta V_{noise}\right)$$

$$V_{out}' = f\left(V_{in}\right) + \frac{dV_{out}}{dV_{in}} \cdot \Delta V_{noise} + higher\ order\ terms\ (neglected)$$

Perturbed Output = Nominal Output + Gain x External Perturbation

- If the magnitude of the voltage gain at the nominal input voltage V_{in} is smaller than unity, then the input perturbation is not amplified and, consequently, the output perturbation remains relatively small.
- Otherwise, with the voltage gain larger than unity, a small perturbation in the input voltage level will cause a rather large perturbation in the output voltage.
- Hence, we define the boundaries of the valid input signal regions as the voltage points where the magnitude of the inverter voltage gain is equal to unity.

Noise Immunity and Noise Margins

Critical Parameters for Inverter design:

V_{OH}: Maximum output voltage when the output level is logic " 1"

V_{OL}: Minimum output voltage when the output level is logic "0"

V_{IL}: Maximum input voltage which can be interpreted as logic "0"

V_{IH}: Minimum input voltage which can be interpreted as logic " 1"

Power and Area Consideration

- The DC power dissipation of an inverter is defined as

$$P_{DC} = V_{DD} \cdot I_{DC}$$

- Current depends upon input and output voltage levels. Assume input voltage level 50% is at logic '0' and 50% at logic '1'.

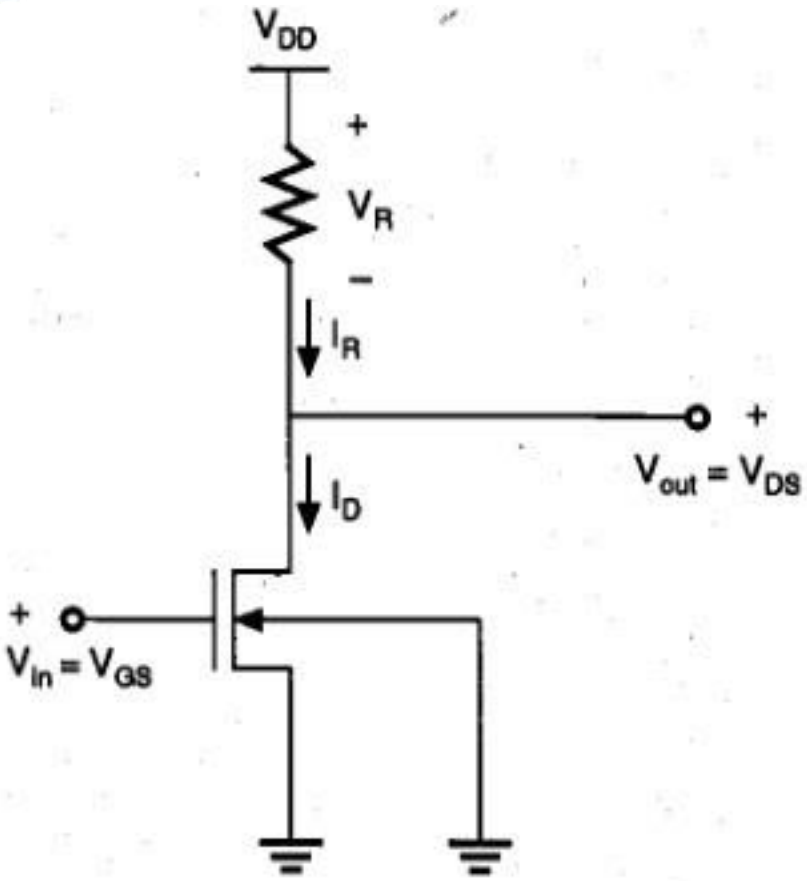
$$P_{DC} = \frac{V_{DD}}{2} \cdot \left[I_{DC}(V_{in} = low) + I_{DC}(V_{in} = high) \right]$$

- To reduce chip area, one has to reduce the size of transistor i.e. gate area (W x L). Thus keep W/L ratio close to unity.

Inverters with different types of load

1. **Resistive-Load Inverter**
2. **Depletion-load NMOS Inverter**
3. **Enhancement-load NMOS Inverter**
4. **CMOS Inverter**

Resistive-Load Inverter



- The average DC power consumption of the resistive-load inverter circuit is found by considering two cases, $V_{in} = V_{OL}$ (Low) and $V_{in} = V_{OH}$ (high).
- When the input voltage is equal to VOL, the driver transistor is in cut-off. Consequently, there is no steady-state current flow in the circuit ($I_D = I_R = 0$), and the DC power dissipation is equal to zero.
- When the input voltage is equal to VOW on the other hand, both the driver MOSFET and the load resistor conduct a nonzero current. Since the output voltage in this case is equal to V_{OL}'
- The current drawn from the power supply can be found as:

$$I_D = I_R = \frac{V_{DD} - V_{OL}}{R_L}$$

- The chip area occupied by the resistive-load inverter circuit depends on two parameters, the (W/L) ratio of the driver transistor and the value of the resistor RL. The area of the driver transistor can be approximated by the gate area, (WxL).

Resistive-Load Inverter

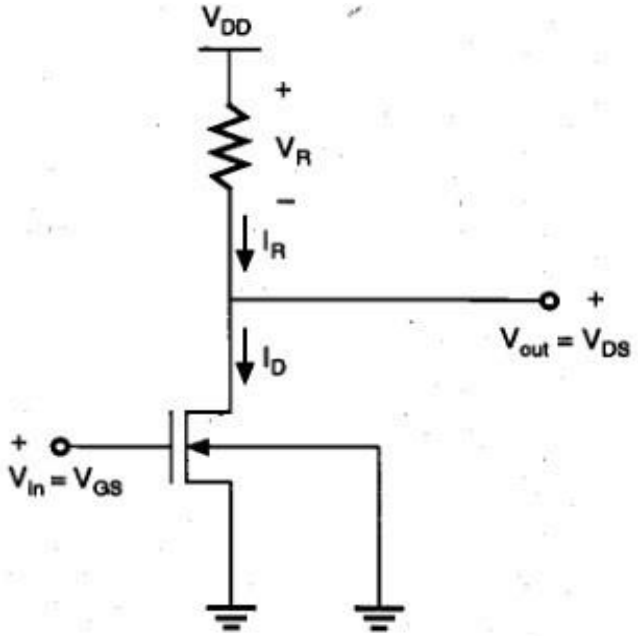


Table: Operating regions of the driver transistor in the resistive-load inverter.

Input Voltage Range	Operating Mode
$V_{in} < V_{T0}$	cut-off
$V_{T0} \leq V_{in} < V_{out} + V_{T0}$	saturation
$V_{in} \geq V_{out} + V_{T0}$	linear

Resistive-Load Inverter

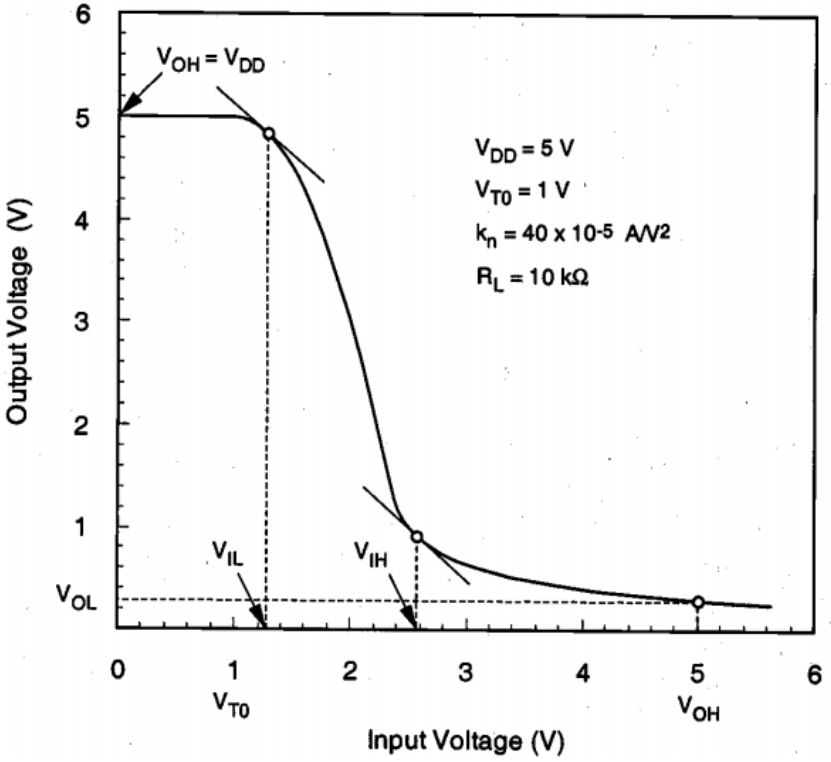


Fig. Typical VTC of a resistive-load inverter circuit.

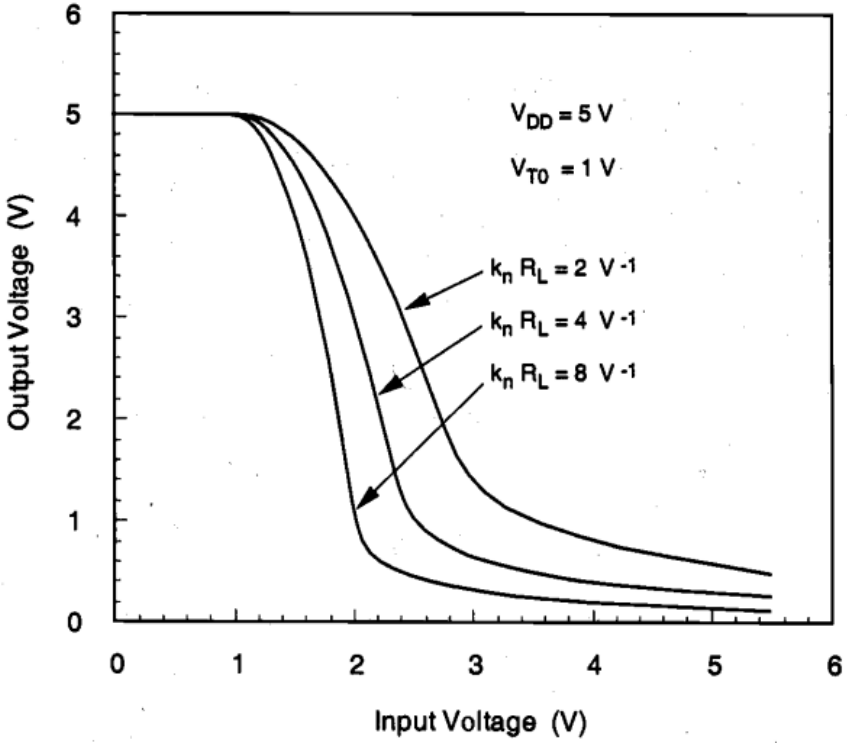
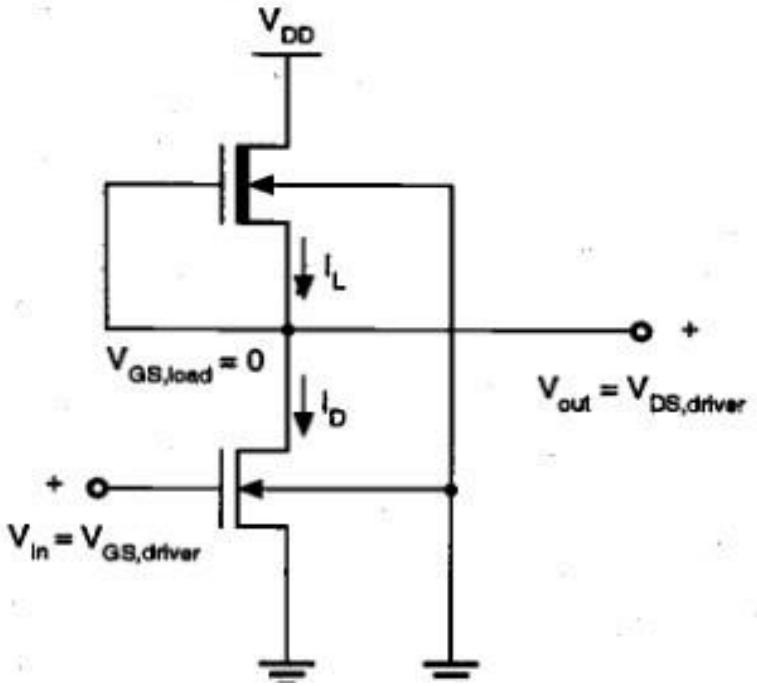


Fig. Voltage transfer characteristics of the resistive-load inverter, for different value of the parameter (k_n, $\mathbf{R_L}$)

Depletion-load NMOS Inverter



- Several disadvantages of the enhancement-type load inverter can be avoided by using a depletion-type nMOS transistor as the load device.-
- The fabrication process for producing an inverter with an enhancement-type nMOS driver and a depletion-type nMOS load is slightly more complicated and requires additional processing steps, especially for the channel implant to adjust the threshold voltage of the load device.

- The resulting improvement of circuit performance and integration possibilities, however, easily justify the additional processing effort required for the fabrication of depletion-load inverters.
- The immediate advantages of implementing this circuit configuration are:

(i) Sharp VTC transition and better noise margins,
(ii) single power supply, and
(iii) smaller overall layout area.

Depletion-load NMOS Inverter

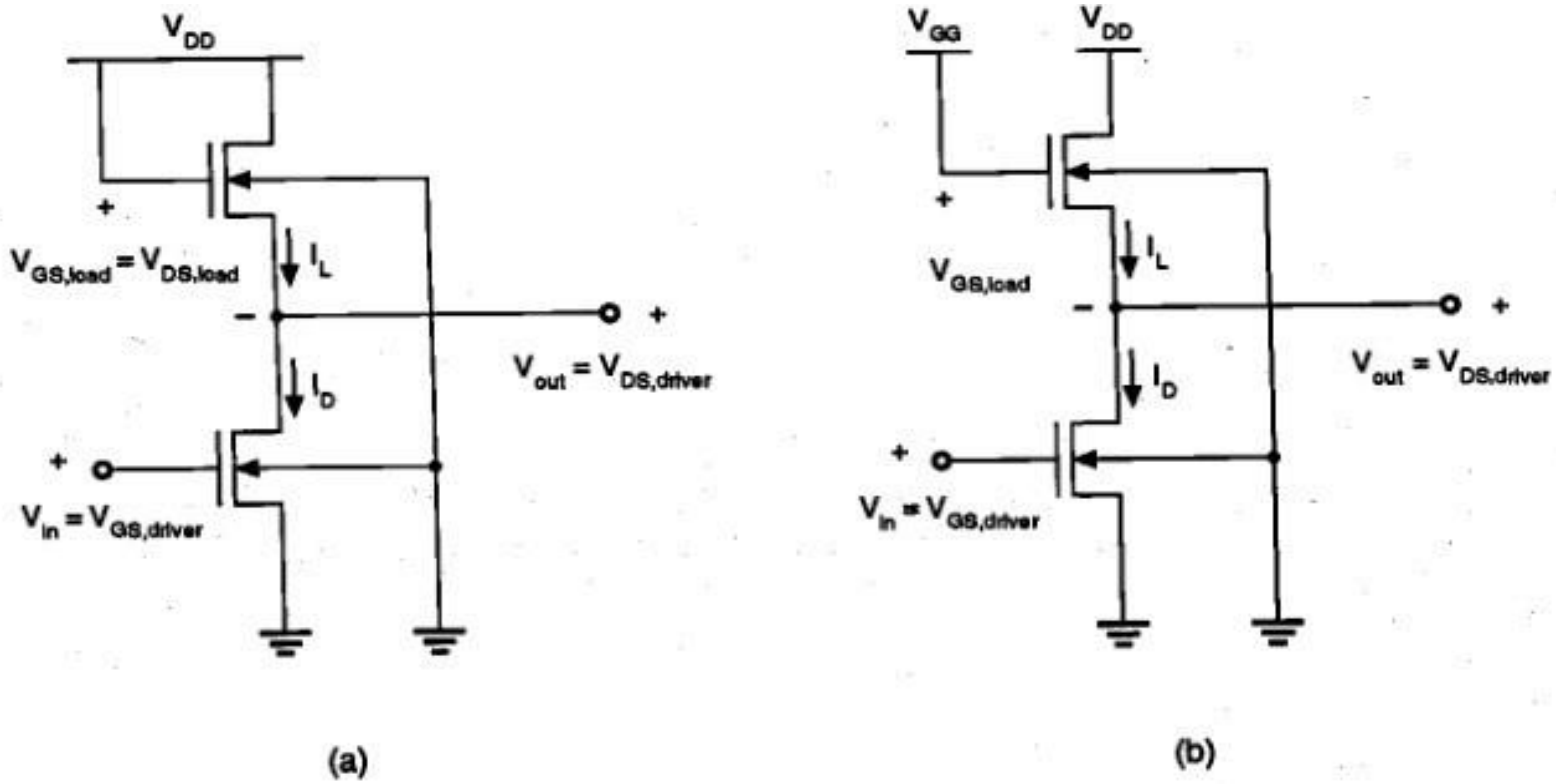


Fig.(a) Inverter circuit with saturated enhancement-type nMOS load. **(b)** Inverter with linear enhancement-type load.

- The circuit configurations of two inverters with enhancement-type load devices are depending on the bias voltage applied to its gate terminal, the load transistor can be operated either in the saturation region or in the linear region.

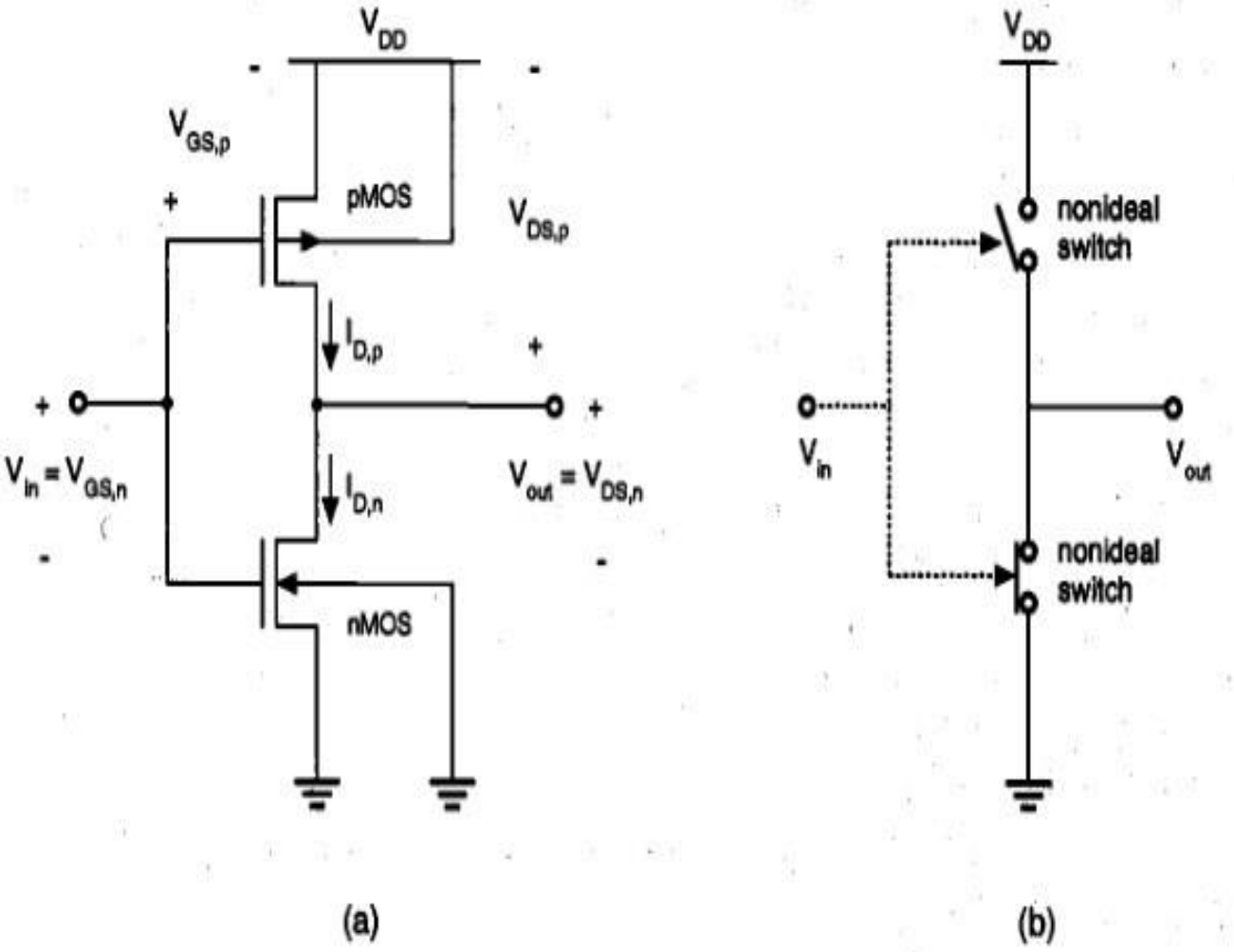
Depletion-load NMOS Inverter (Continued..)

- Both types of inverters have some distinct advantages and disadvantages from the circuit design point of view.
- The saturated enhancement-load inverter shown in Fig.(a) requires a single voltage supply and a relatively simple fabrication process, yet the V_{OH} level is limited to (V_{DD} – V_{TIload})
- The load device of the inverter circuit shown in Fig. (b), on the other hand, is always biased in the linear region. Thus, the V_{OH} level is equal to V_{DD}, resulting in higher noise margins compared to saturated enhancement-load inverter.
- The most significant drawback of this configuration is the use of two separate power supply voltages.
- In addition, both types of inverter circuits suffer from relatively high stand-by (DC) power dissipation
- Hence, enhancement-load nMOS inverters are not used in any large-scale digital applications.

CMOS Inverter

- The CMOS inverter has two important advantages over the other inverter configurations:
- The first and perhaps the most important advantage is that the steady-state power dissipation of the CMOS inverter circuit is virtually negligible, except for small power dissipation due to leakage currents. In all other inverter structures examined so far, a nonzero steady-state current is drawn from the power source when the driver transistor is turned on, which results in a significant DC power consumption.
- The other advantages of the CMOS configuration are that the voltage transfer characteristic (VTC) exhibits a full output voltage swing between 0 V and V_{DD}, and that the VTC transition is usually very sharp. Thus, the VTC of the CMOS inverter resembles that of an ideal inverter.

CMOS Inverter



CMOS Inverter

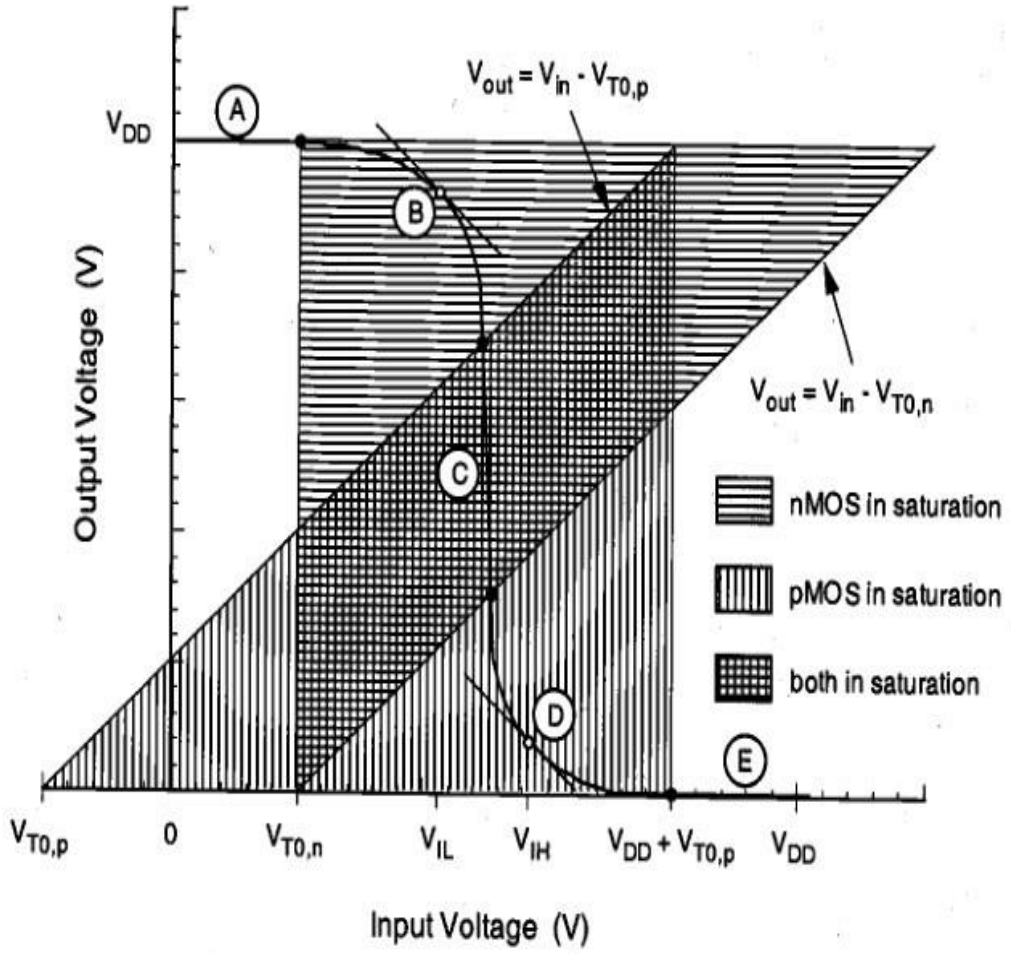


Fig. VTC Characteristic

A: P Linear N Cut-off

B: P Linear N Saturation

C: P saturation N Saturation

D: P Saturation N Linear

E: P Cut-off N Linear

$$\frac{k_n}{k_p} = \frac{\mu_n C_{ox} \cdot \left(\frac{W}{L}\right)_n}{\mu_p C_{ox} \cdot \left(\frac{W}{L}\right)_p} = \frac{\mu_n \cdot \left(\frac{W}{L}\right)_n}{\mu_p \cdot \left(\frac{W}{L}\right)_p}$$

For Symmetric Inverter:

$V_{T0}=V_{T0n}=-V_{T0p}$ and $K_R=1$

$$\frac{\left(\frac{W}{L}\right)_n}{\left(\frac{W}{L}\right)_p} = \frac{\mu_p}{\mu_n} \approx \frac{230\ \text{cm}^2/\text{V}\cdot\text{s}}{580\ \text{cm}^2/\text{V}\cdot\text{s}}$$

$$\left(\frac{W}{L}\right)_p \approx 2.5\left(\frac{W}{L}\right)_n$$