Analog Integrated Circuits (BEC-27)

…Study of Op-Amp based Circuits and why they are useful to us

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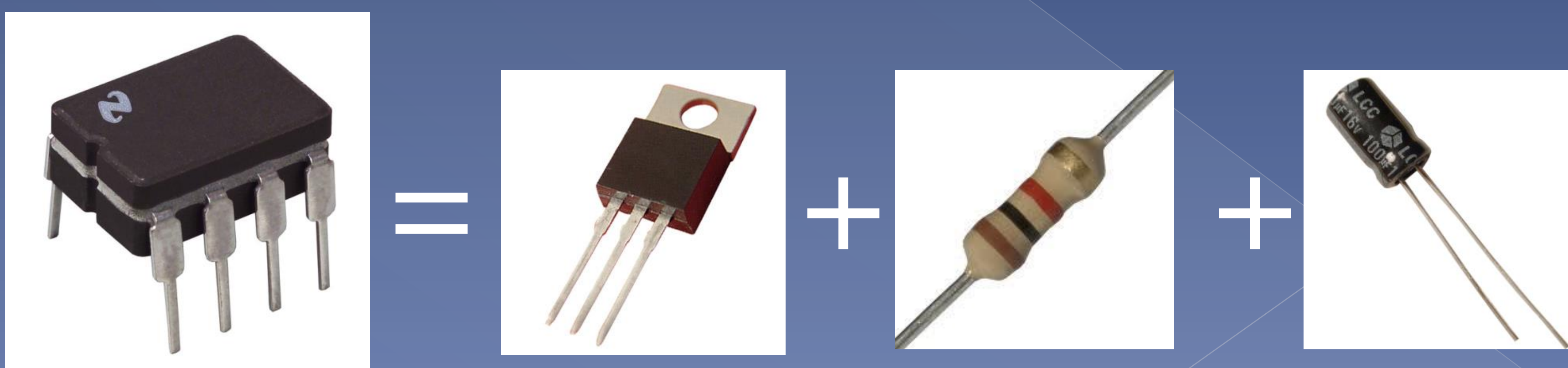
Outline of Presentation

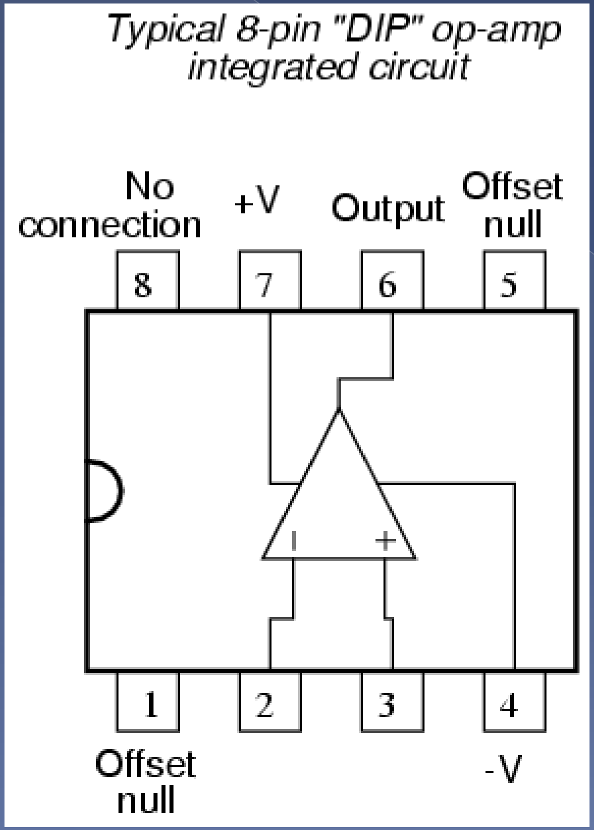
- What is an Analog IC and Op-Amp?
- Characteristics of Ideal and Real Op-Amps
- Common Op-Amp Circuits
- Applications of Op-Amps
- References

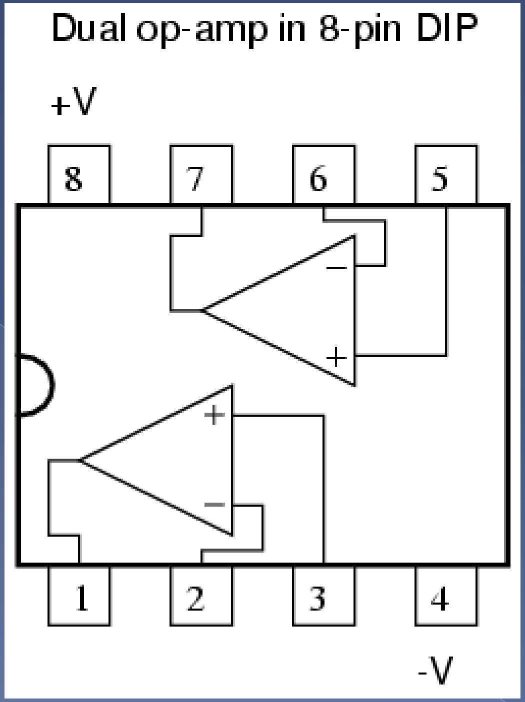
What is an Op-Amp?

- An *Operational Amplifier* (known as an "Op-Amp") is a device that is used to amplify a signal using an external power source
- Op-Amps are generally composed of:
  - Transistors, Resistors, Capacitors



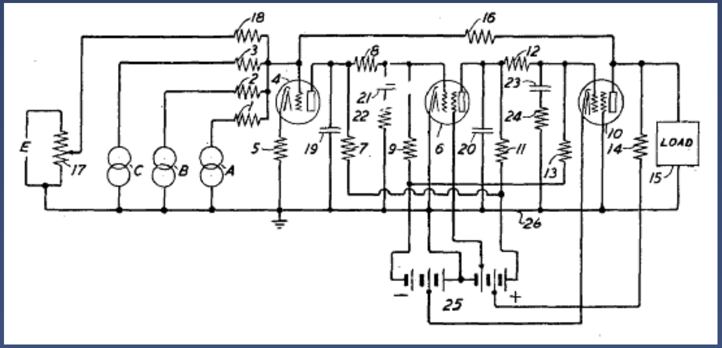
What do they really look like?





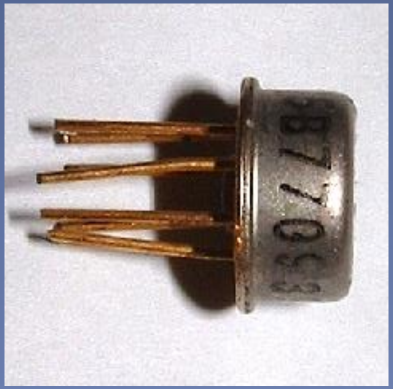
Brief History

- First patent for Vacuum Tube Op-Amp (1946)



- First Commercial Op-Amp available (1953)

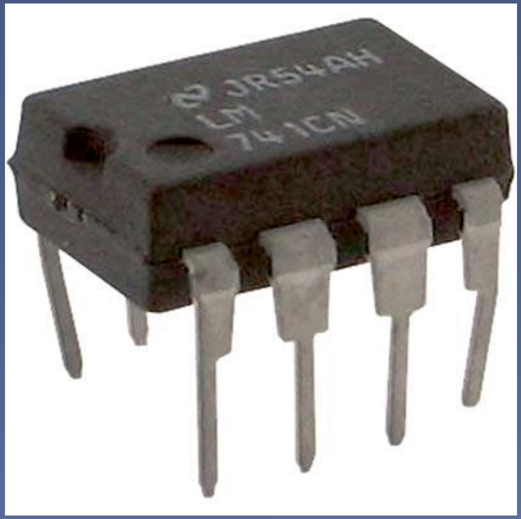
- First discrete IC Op-Amps (1961)



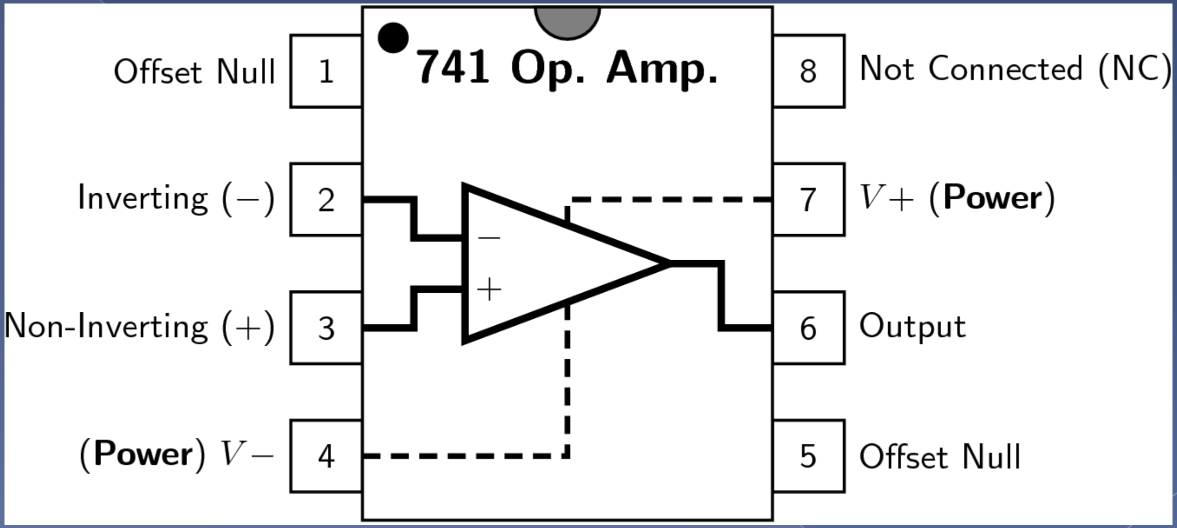
- First commercially successful Monolithic Op-Amps (1965)

History Continued…

- Leading to the advent of the modern Analog IC which is still used even today (1967 – present)



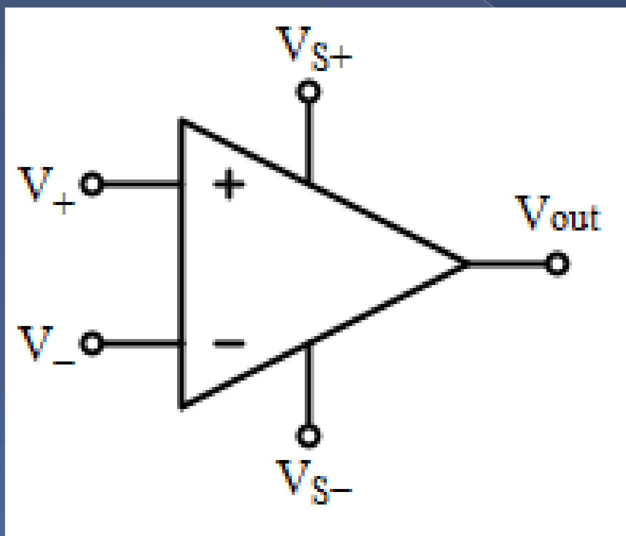
Fairchild µA741



Electrical Schematic of µA741

Op-Amps and their Math

A traditional Op-Amp:



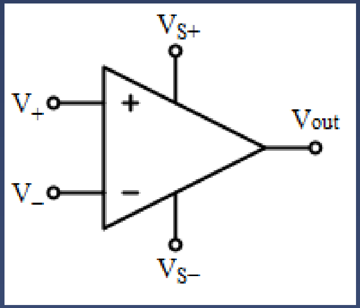
V_+ : non-inverting input
V_- : inverting input
V_{out} : output
V_{S+} : positive power supply
V_{S-} : negative power supply

$$V_{out} = K\,(V_+ - V_-)$$

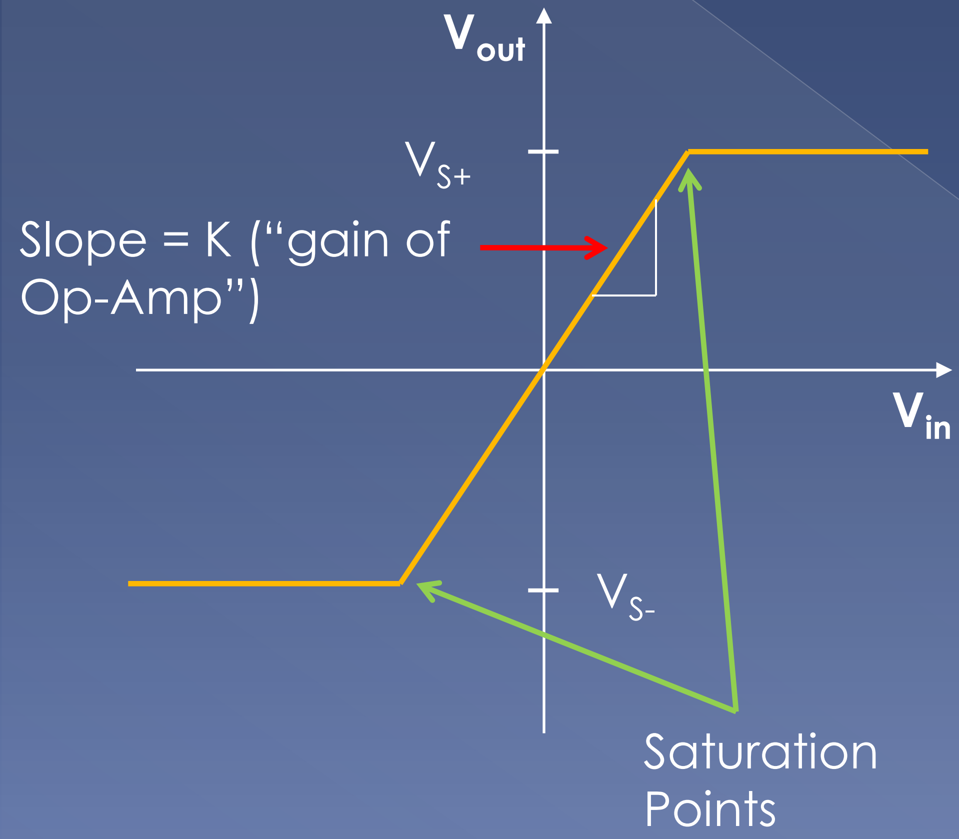
- The difference between the two inputs voltages (V_+ and V_-) multiplied by the gain (K, “amplification factor”) of the Op-Amp gives you the output voltage

- The output voltage can only be as high as the <u>difference</u> between the power supply (V_{S+} / V_{S-})and ground (0 Volts)

Saturation



Saturation is caused by increasing/decreasing the input voltage to cause the output voltage to equal the power supply's voltage*



The slope is normally much steeper than it is shown here. Potentially just a few milli-volts (mV) of change in the difference between V_+ and V_- could cause the op-amp to reach the saturation level

* Note that saturation level of traditional Op-Amp is 80% of supply voltage with exception of CMOS op-amp which has a saturation at the power supply's voltage

Important Parameters for Op-Amps

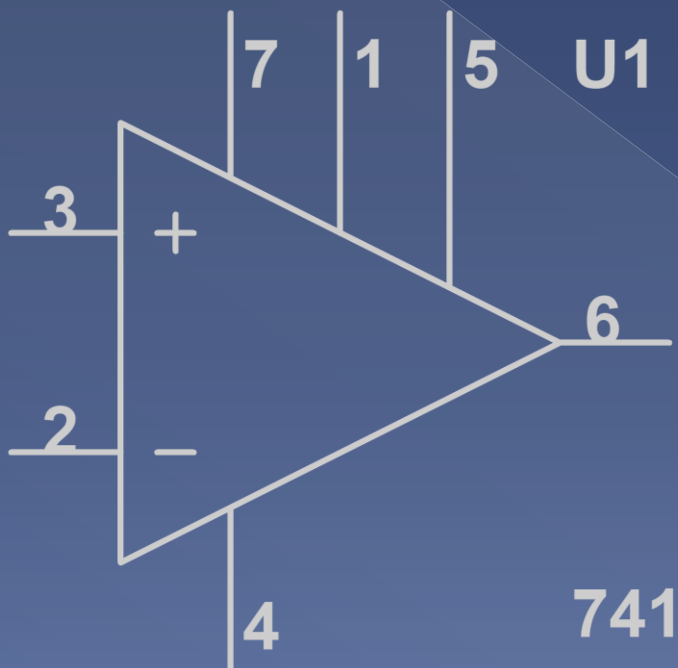
- Input Parameters
  - Voltage (Vicm)
  - Offset voltage
  - Bias current
  - Input Impedance
- Output Parameters
  - Short circuit current
  - Voltage Swing
  - Open Loop Gain
  - Slew Rate

An Ideal Op-Amp

- Infinite voltage gain
- Infinite input impedance
- Zero output impedance
- Infinite bandwidth
- Zero input offset voltage (i.e., exactly zero out if zero in).

http://hyperphysics.phy-astr.gsu.edu/hbase/electronic/opamp.html#c4

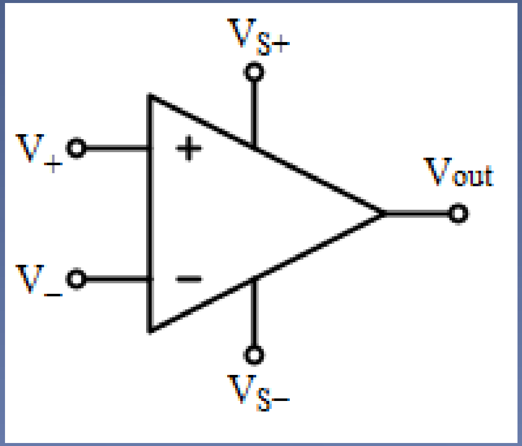
Circuit Symbol and Pin Identification



- 2 Inverting Input
- 3 Non-Inverting Input
- 6 Output
- 7 + Voltage Supply V_{CC}
- 4 – Voltage Supply V_{EE}
- 1 and 5 -- Offset Null

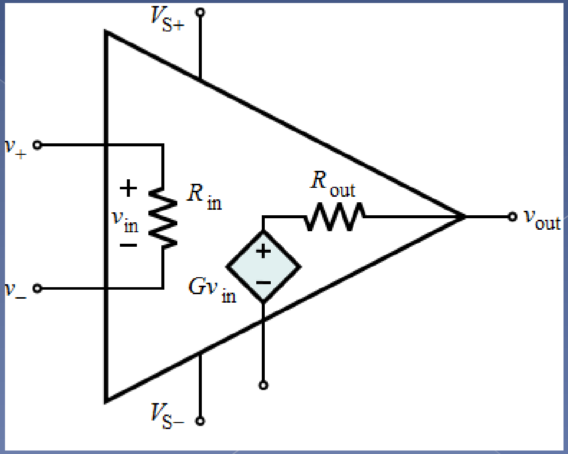
Ideal versus Real Op-Amps

Parameter	Ideal Op-Amp	Real Op-Amp
Differential Voltage Gain	∞	10^5 - 10^9
Gain Bandwidth Product (Hz)	∞	1-20 MHz
Input Resistance (R)	∞	10^6 - 10^{12} Ω
Output Resistance (R)	0	100 - 1000 Ω



Ideal

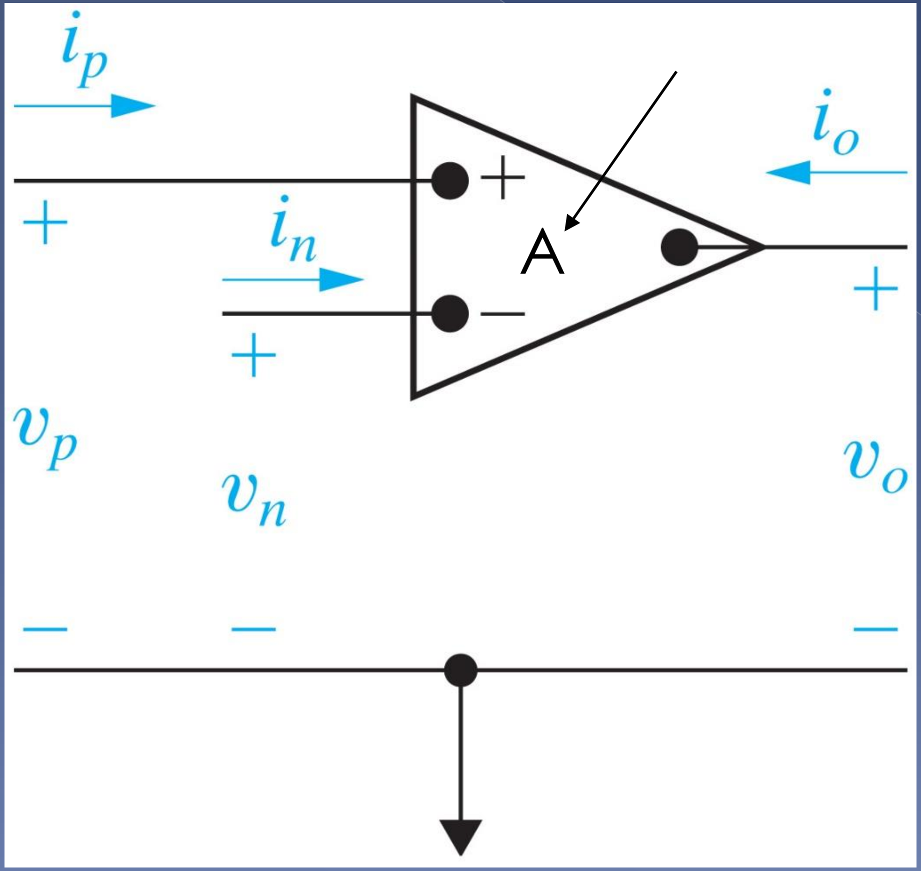
Real



http://hyperphysics.phy-astr.gsu.edu/hbase/electronic/opamp.html#c4

Ideal OP AMP (Open Loop)

A = "open-loop" gain



$$v_o = A(v_p - v_n)$$

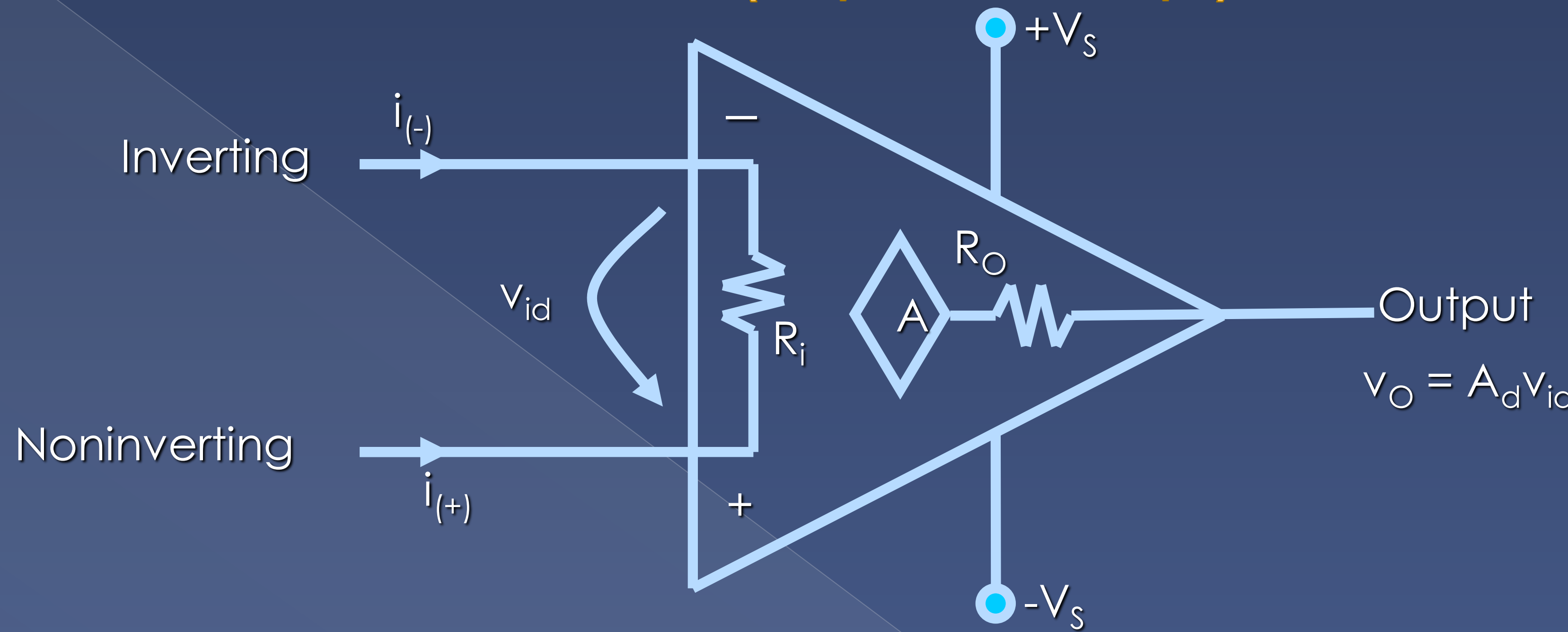
$$R_{in} \to \infty$$

$$A \to \infty$$

$$v_p = v_n$$

$$i_p = i_n = 0$$

Practical OP AMP (Open Loop)



- $i_{(+)}$, $i_{(-)}$: Currents into the amplifier on the inverting and noninverting lines respectively
- v_{id} : The input voltage from inverting to non-inverting inputs
- $+V_S$, $-V_S$: DC source voltages, usually +15V and –15V
- R_i : The input resistance, ideally infinity
- A : The gain of the amplifier. Ideally very high, in the $1x10^{10}$ range.
- R_O: The output resistance, ideally zero
- v_O: The output voltage; $v_O = A_{OL}v_{id}$ where A_{OL} is the open-loop voltage gain

POWER BW

The maximum frequency at which a sinusoidal output signal can be produced without causing distortion in the signal.

The power bandwidth, BW_p is determined using the desired output signal amplitude and the the slew rate (*see next slide*) specifications of the op amp.

$$BW_p = \frac{SR}{2\pi V_{o(max)}}$$

$SR = 2\pi f V_{o(max)}$ where SR is the slew rate

Example:

Given: $V_{o(max)} = 12$ V and SR = 500 kV/s

Find: BW_p

Solution: $$BW_p = \frac{500 \text{ kV/s}}{2\pi * 12 \text{ V}} = 6.63 \text{ kHz}$$

SLEW RATE

A limitation of the maximum possible rate of change of the output of an operational amplifier.

As seen on the previous slide, this is derived from:

$SR = 2\pi f V_{o(max)}$

$SR = (\partial v_o / \partial t)|_{max}$

Slew Rate is independent of the closed-loop gain of the op amp.

Example:

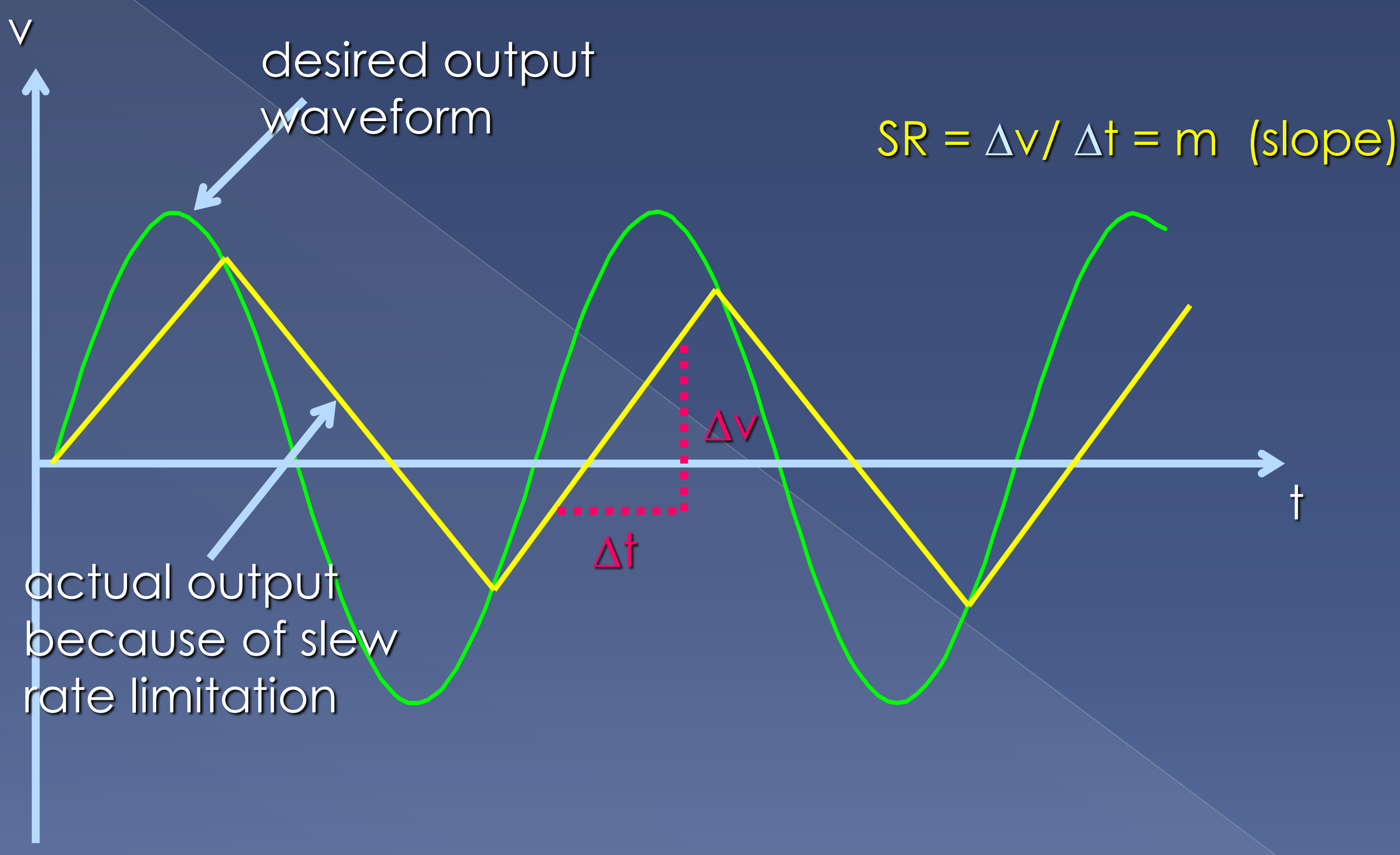
Given: SR = 500 kV/s and Δv_o = 10 V ($V_{o(max)}$ = 12V)

Find: The Δt and f.

Solution: $\Delta t = \Delta v_o / SR = (10\ V) / (5\times10^5\ V/s) = 2\times10^{-5}\ s$

$f = SR / 2\pi V_{o(max)} = (5\times10^5\ V/s) / (2\pi * 12) = 6{,}630\ Hz$

SLEW RATE DISTORTION

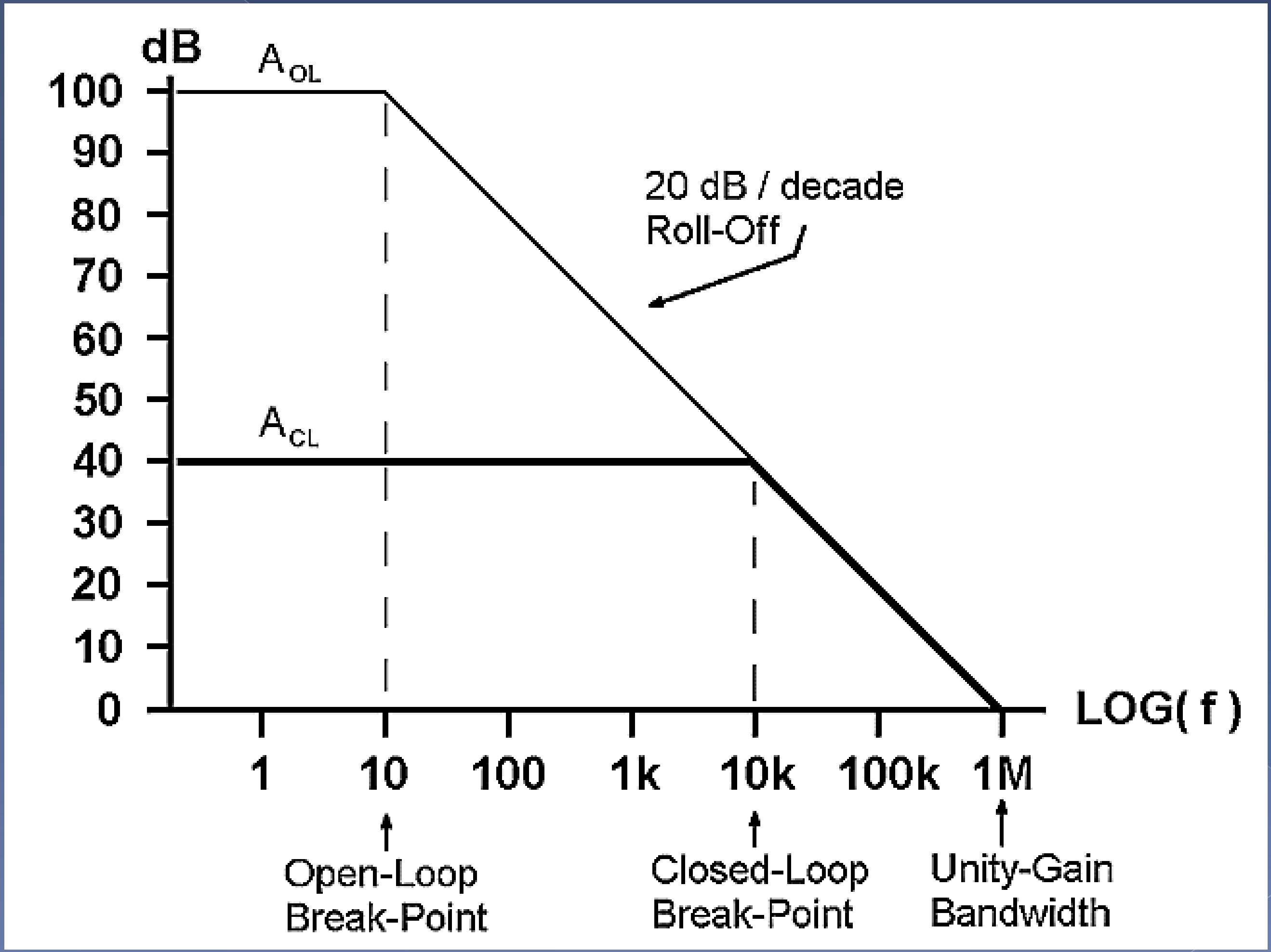


The picture above shows exactly what happens when the slew rate limitations are not met and the output of the operational amplifier is distorted.

Gain-Bandwidth Product

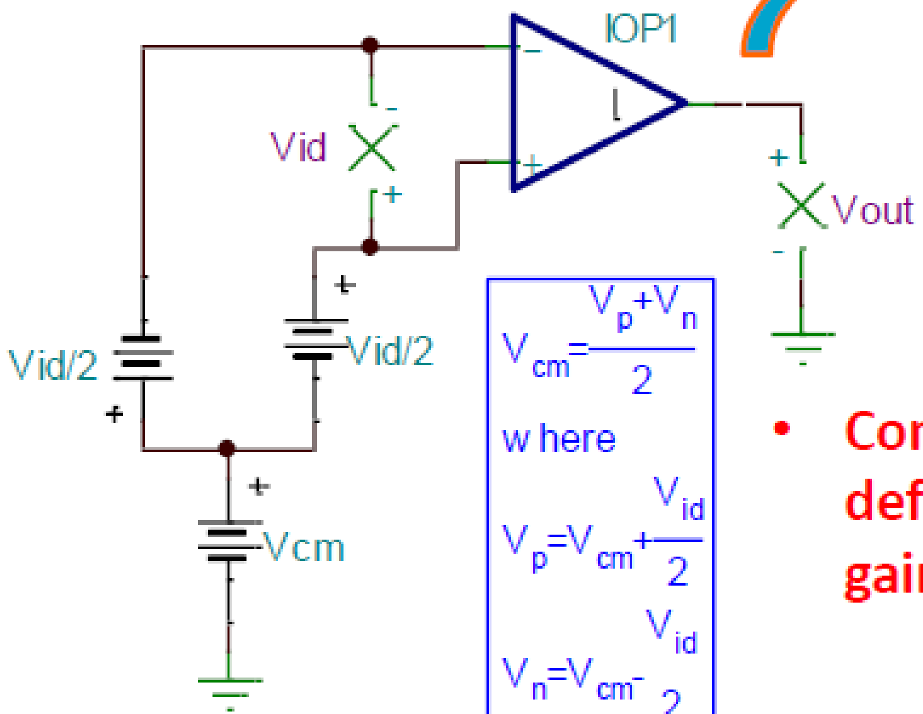
- **Gain Bandwidth Product (GBP)-** is the product of the open-loop gain and the bandwidth at that gain.
- For practical purposes the actual gain should only be 1/10 to 1/20 of the open loop gain at a given frequency to ensure that the op-amp will operate without distortion.

Open and Closed Loop Response



Common Mode Rejection Ratio (CMRR) (contd.)

- For a differential amplifier, common-mode voltage is defined as the average of the two input voltages.



$$V_{cm} = \frac{V_p + V_n}{2}$$

where

$$V_p = V_{cm} + \frac{V_{id}}{2}$$

$$V_n = V_{cm} - \frac{V_{id}}{2}$$

$$V_{out} = A_{dm}(V_{id}) + A_{cm}(V_{cm})$$

where

A_{dm} = Differential-mode gain

A_{cm} = Common-mode gain

- Common-Mode Rejection Ratio is defined as the ratio of the differential gain to the common-mode gain.

$$CMRR = \left|\frac{A_{dm}}{A_{cm}}\right|$$

- CMR is defined as: $CMR(dB) = 20\log_{10}(CMRR)$

PSRR

One of the reasons op amps are so useful, is that they can be operated from a wide variety of power supply voltages.

The 741 op amp can be operated from bipolar supplies ranging from ±5V to ±18V with out too many changes to the parameters of the op amp.

The power supply rejection ratio (SVRR) refers to the slight change in output voltage that occurs when the power supply of the op amp changes during operation.

$SVRR = 20 \log (V_s / V_o)$

The SVRR value is given for a specified op amp. For the 741 op amp, SVRR = 96 dB over the range ± 5V to ± 18V.

Basics of an Op-Amp Circuit

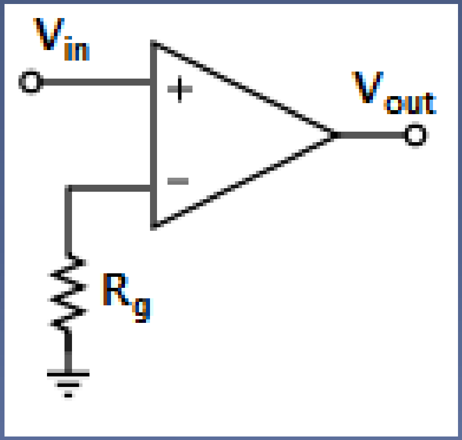
- An op-amp amplifies the difference of the inputs V_+ and V_- (known as the differential input voltage)
- This is the equation for an *open loop* gain amplifier:

$$V_{out}=K(V_+-V_-)$$

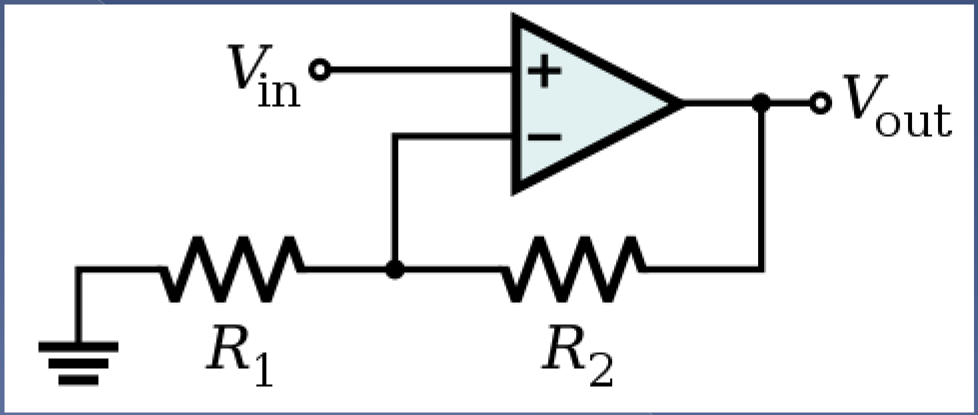
- K is typically very large – at around 10,000 or more for IC Op-Amps
- This equation is the basis for all the types of amps we will be discussing

Open Loop vs Closed Loop

- A closed loop op-amp has feedback from the output to the input, an open loop op-amp does not



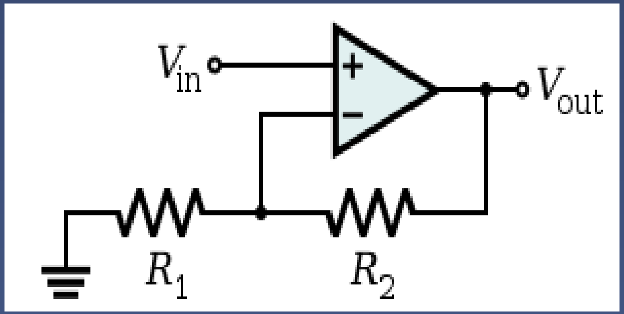
Open Loop



Closed Loop

Non-Inverting Op-Amp

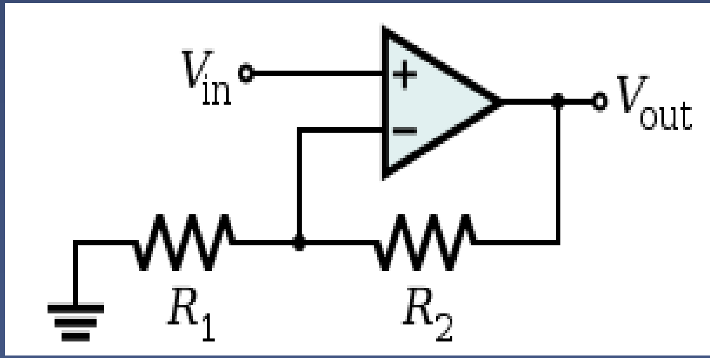
- Amplifies the input voltage by a constant
- Closed loop op-amp
- Voltage input connected to non-inverting input
- Voltage output connected to inverting input through a feedback resistor
- Inverting input is also connected to ground
- Non-inverting input is only determined by voltage output



Non-Inverting Op-Amp

$V_{out}=K(V_+-V_-)$

$R_1/(R_1+R_2)$ ← Voltage Divider



$V_-=V_{out}\ (R_1/(R_1+R_2)\ )$

$V_{out}=[V_{in}-V_{out}\ (R_1/(R_1+R_2))]\ K$

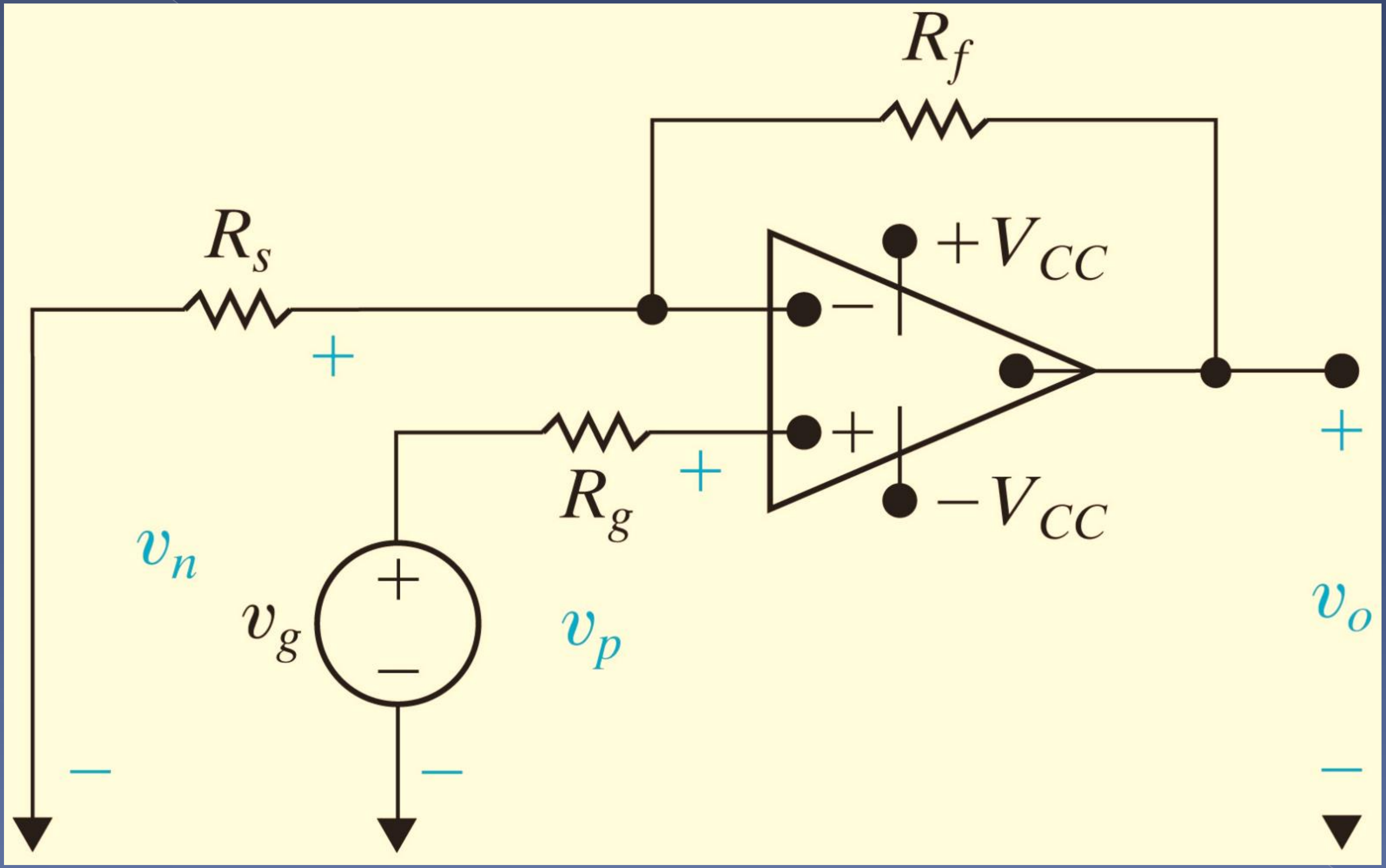
$V_{out}=V_{in}/[(1/K)+\ (R_1/(R_1+R_2))]$

As discussed previously assuming, K is very large, we have:

$V_{out}=V_{in}/(R_1/(R_1+R_2))$

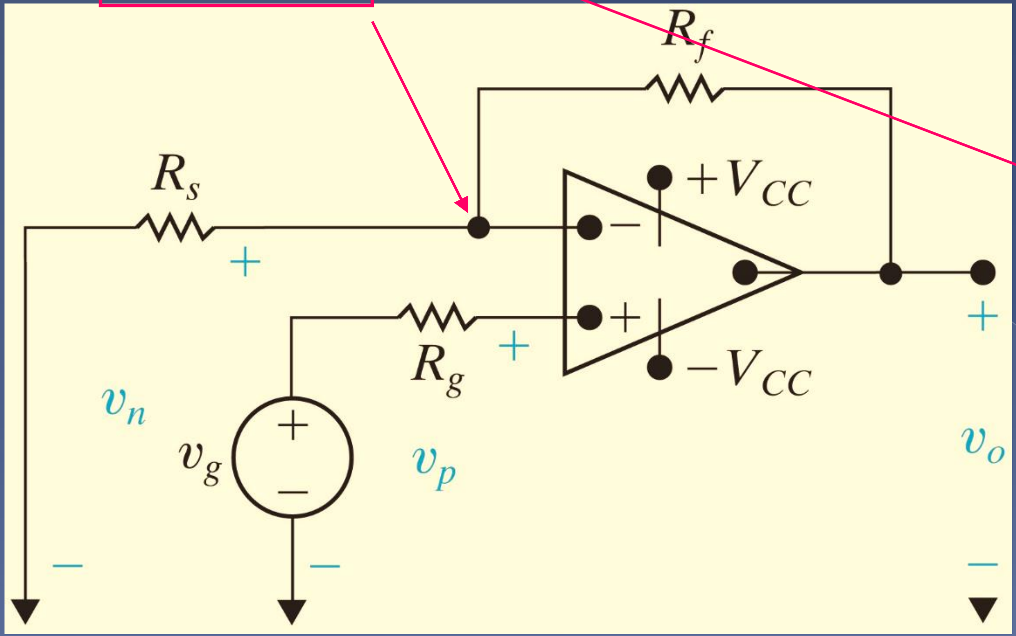
$V_{out}=V_{in}\ (1+(R_2/R_1))$

Non-Inverting Amplifier(Alternate)



Analysis Using the Ideal OP AMP

"Virtual Short



$$v_p = v_g$$

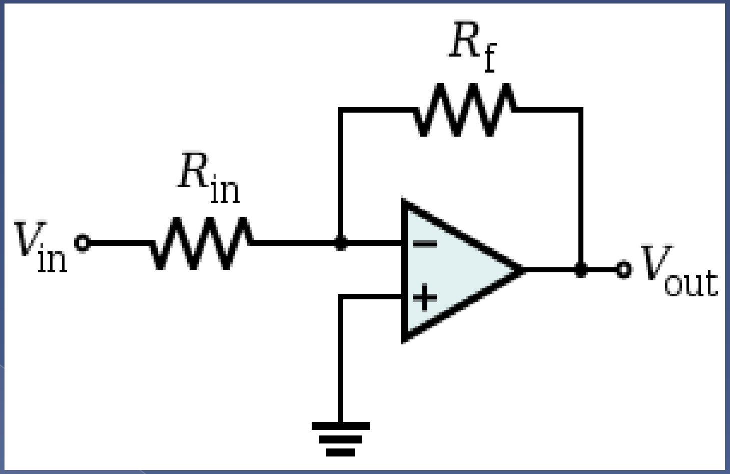
$$v_n = v_p = v_g = v_o \frac{R_s}{R_s + R_f}$$

$$v_o = \frac{R_s + R_f}{R_s} v_g$$

$$v_o = \left(1 + \frac{R_f}{R_s}\right) v_g$$

Inverting Op-Amp

- Amplifies and inverts the input voltage
- Closed loop op-amp
- Non-inverting input is determined by *both* voltage input and output
- The polarity of the output voltage is opposite to that of the input voltage
- Voltage input is connected to inverting input
- Voltage output is connected to inverting input through a feedback resistor
- Non-inverting input is grounded

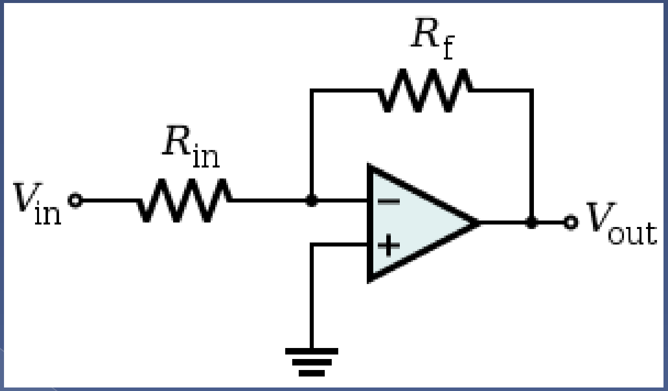


Inverting Op-Amp

$$V_{out}=K(V_+-V_-)$$

$$V_-=V_{out}(R_{in}/(R_{in}+R_f))+V_{in}(R_f/(R_{in}+R_f))$$

$$V_-=(V_{out}R_{in}+V_{in}R_f)/(R_{in}+R_f)$$

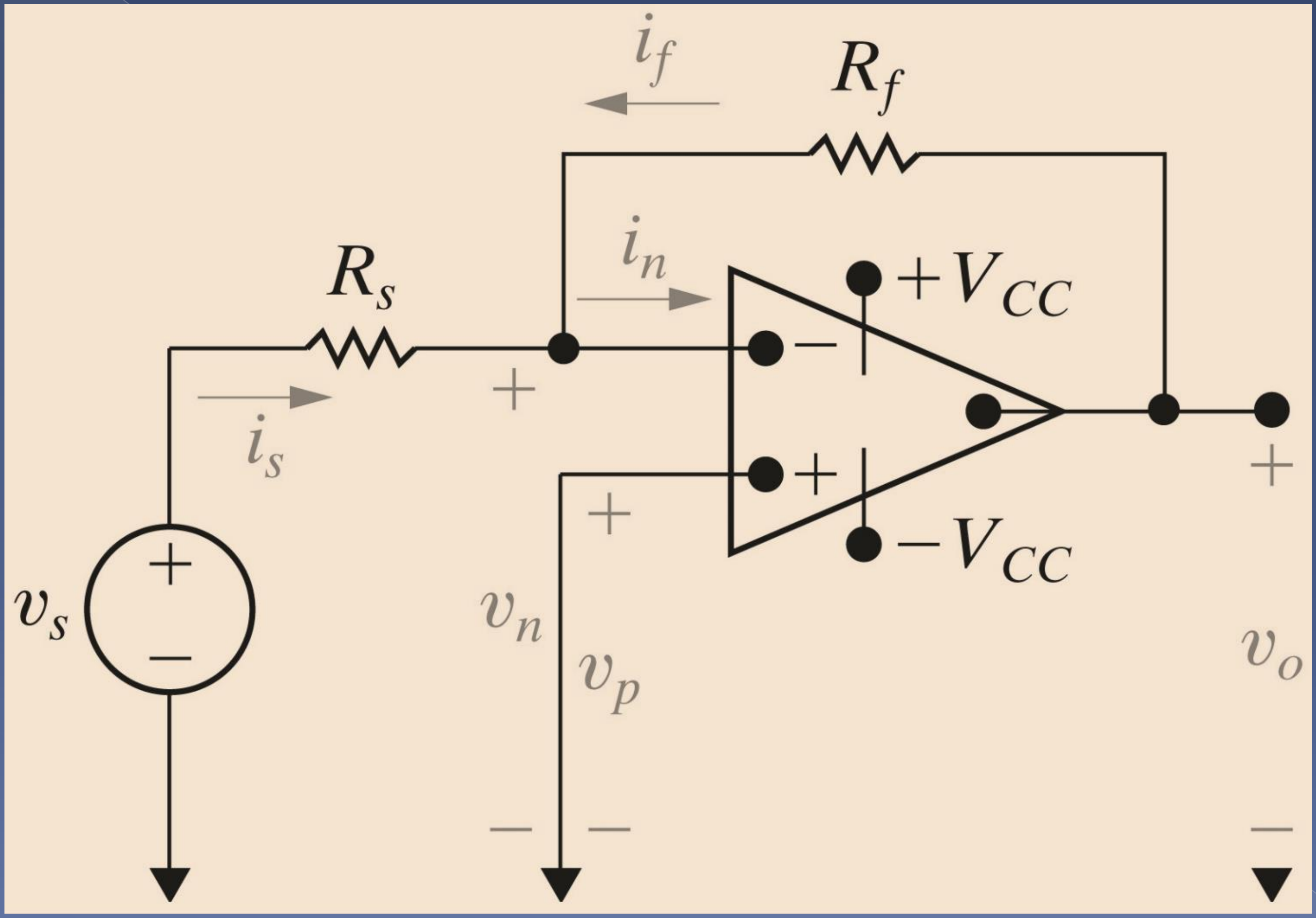


$$V_{out}=K(0-V_-)$$

$$V_{out}=-V_{in}R_f/[(R_{in}+R_f)/K+(R_{in})]$$

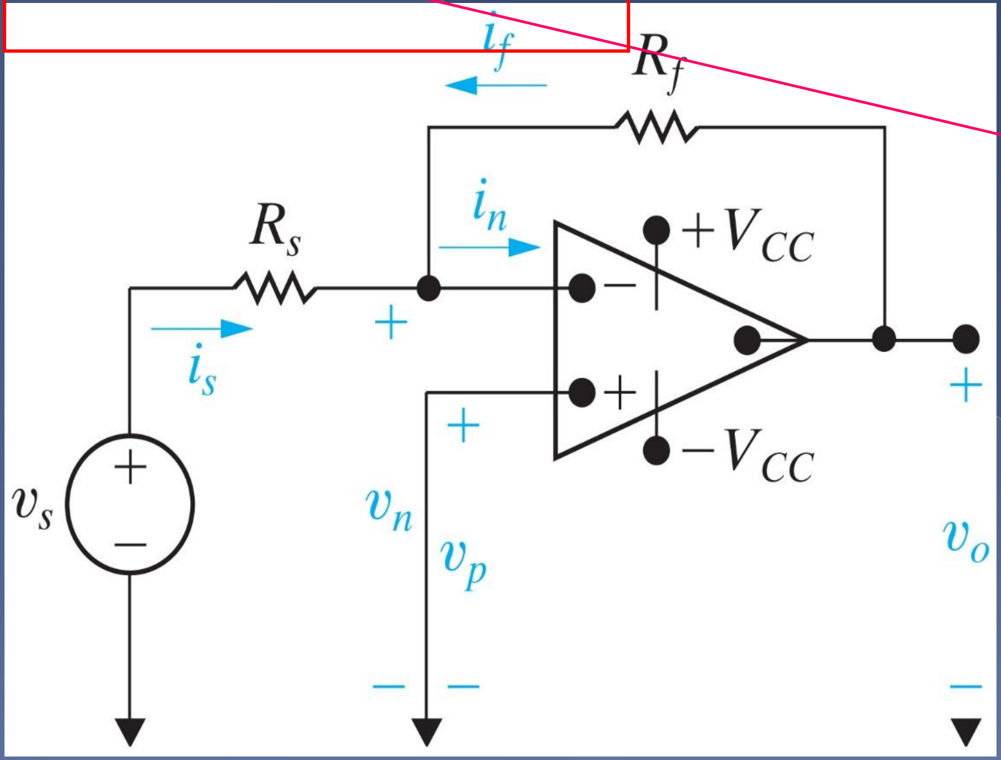
$$V_{out}=-V_{in}R_f/R_{in}$$

Inverting Amplifier



Analysis Using the Ideal OP AMP

"Virtual" ground



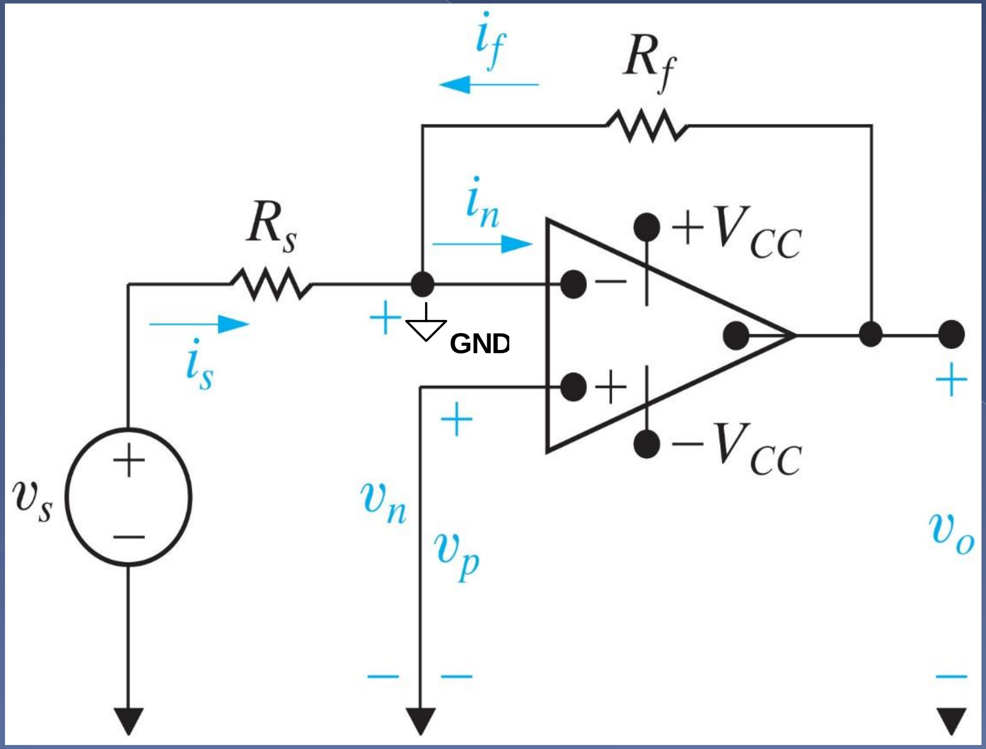
$$i_s + i_f = i_n$$

$$v_n = v_p = 0$$

$$i_s = \frac{v_s}{R_s}$$

$$i_f = \frac{v_o}{R_f}$$

Analysis continued



$$i_n = 0$$

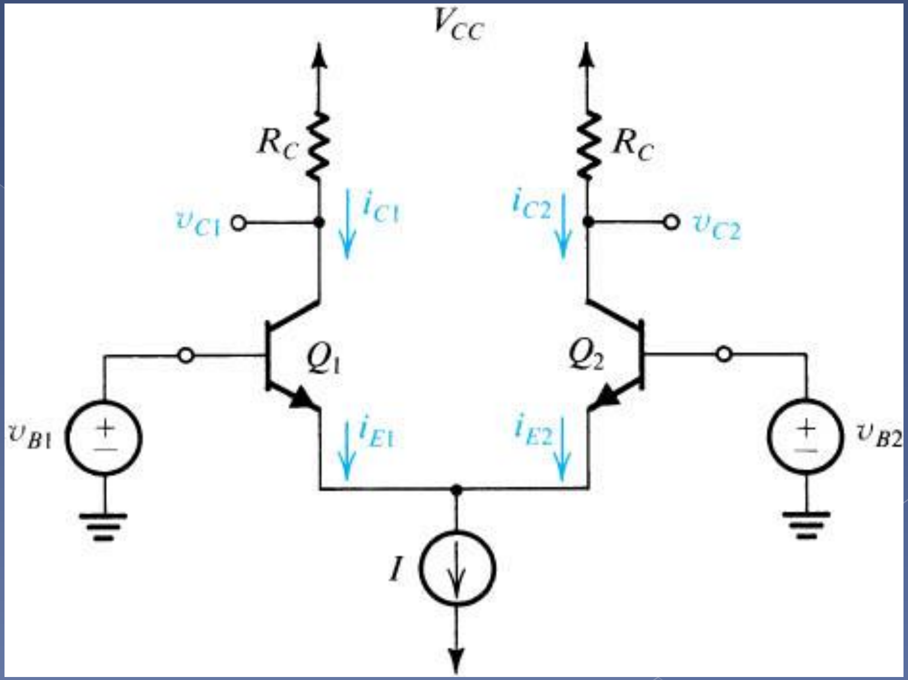
$$i_f = -i_s$$

$$\frac{v_o}{R_f} = -\frac{v_s}{R_s}$$

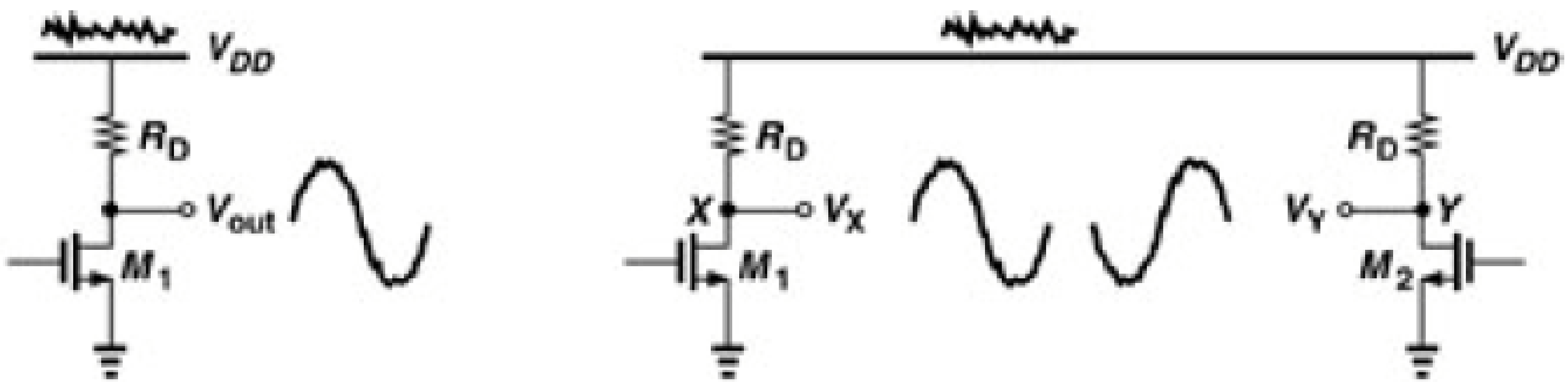
$$v_o = -\frac{R_f}{R_s} v_s$$

The basic BJT differential-pair configuration.

- Differential amplifiers are pervasive in analog electronics
  - Low frequency amplifiers
  - High frequency amplifiers
  - Operational amplifiers – the first stage is a differential amplifier
  - Analog modulators
  - Logic gates
- Advantages
  - Large input resistance
  - High gain
  - Differential input
  - Good bias stability
  - Excellent device parameter tracking in IC implementation
- Examples
  - Bipolar 741 op-amp (mature, well-practiced, cheap)
  - CMOS or BiCMOS op-amp designs (more recent, popular)



Rejection of Power Supply Noise



(a) (b)

- **Maximum Output Swing:**

$$V_{out\max} = V_{DD} - (V_{GS} - V_{TH})$$

- **Maximum Output Swing:**

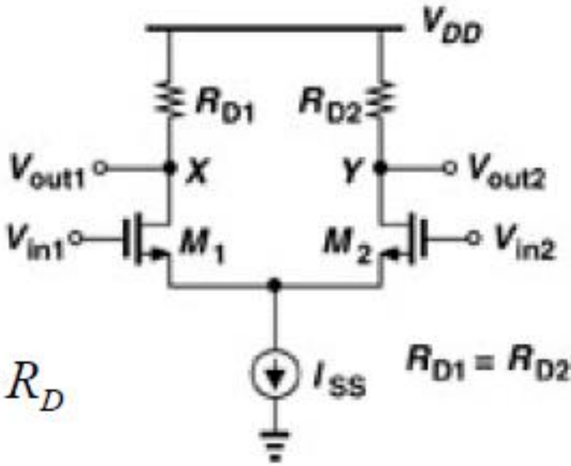
$$V_{X\max} - V_{Y\max} = 2\left[V_{DD} - (V_{GS} - V_{TH})\right]$$

Differential Pair: Qualitative Analysis

$V_{in1} << V_{in2}$ ➡ **M1 OFF, M2 ON**

$I_{D2} = I_{SS}$ ➡ $V_{out1} = V_{DD}$

$V_{out2} = V_{DD} - I_{SS} R_D$



$R_{D1} = R_{D2} = R_D$

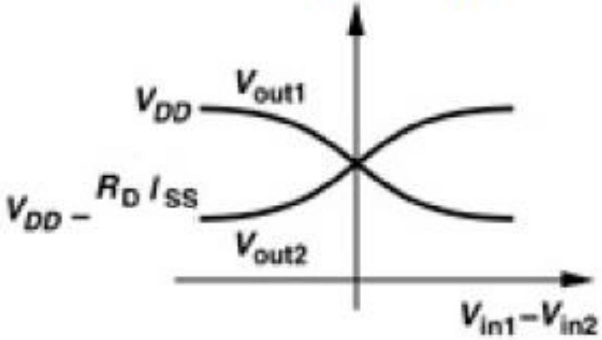
$V_{in1} = V_{in2}$ ➡ **M1 ON, M2 ON**

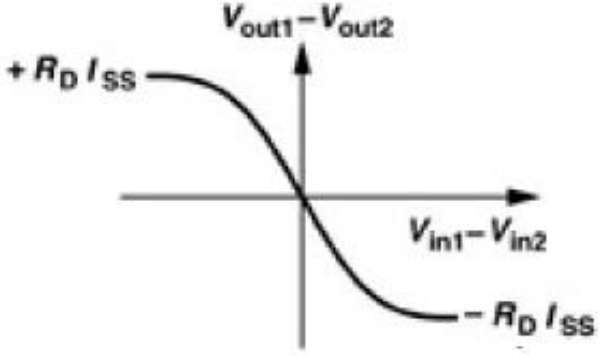
$$I_{D1} = I_{D2} = \frac{I_{SS}}{2} \Rightarrow V_{out1} = V_{out2} = V_{DD} - \frac{I_{SS}}{2} R_D$$

$V_{in1} >> V_{in2}$ ➡ **M1 ON, M2 OFF**

$I_{D1} = I_{SS}$ ➡ $V_{out1} = V_{DD} - I_{SS} R_D$

$V_{out2} = V_{DD}$

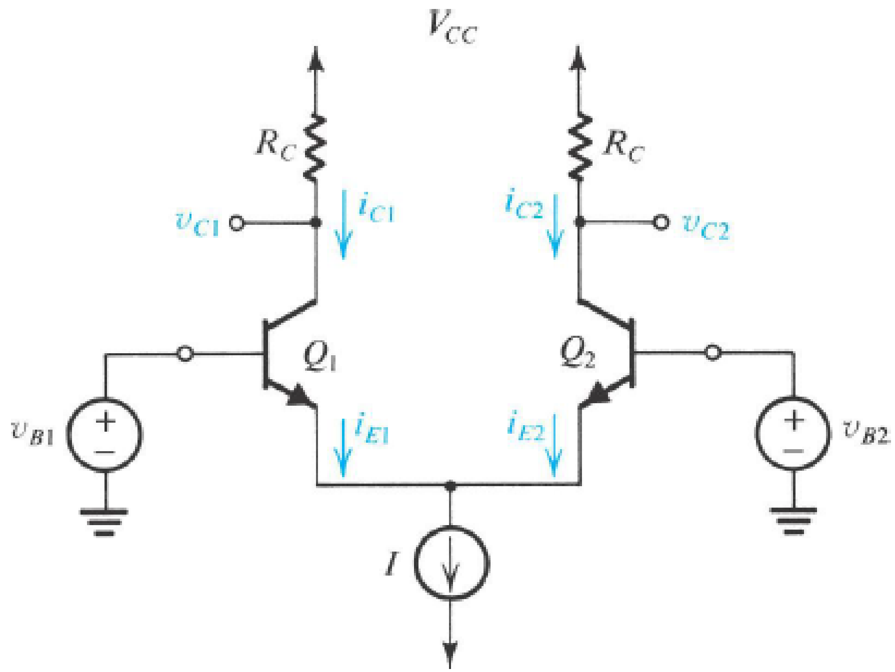




The BJT Differential Pair

- Figure 8.15 shows the basic BJT differential-pair configuration

- – composed of two matched transistors biased by a constant-current source – and is modeled by similar expressions.



Input Common-Mode Range

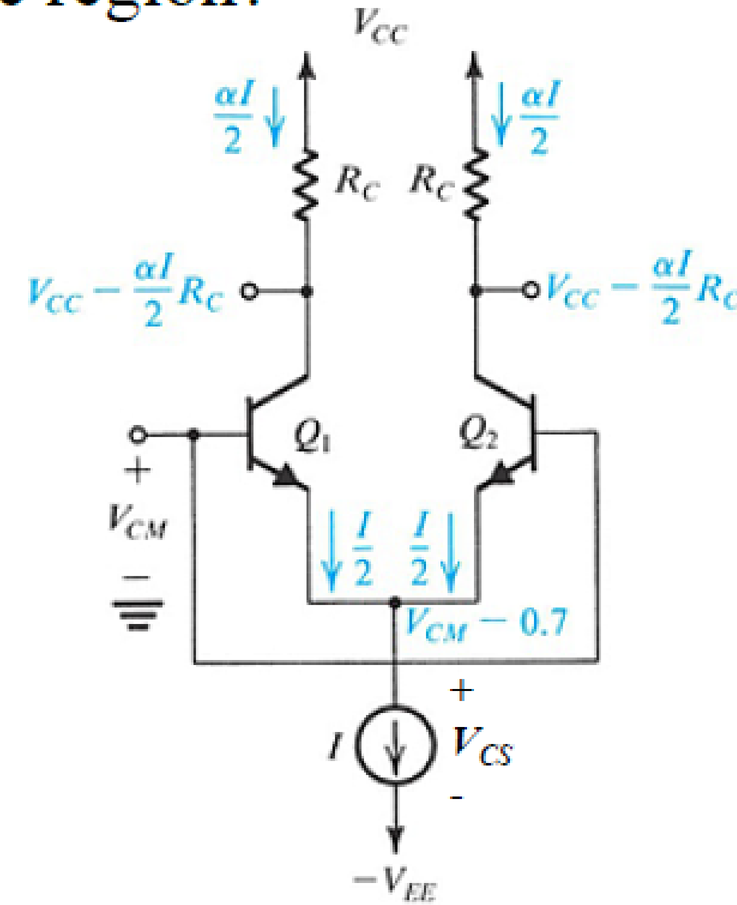
DC Common-mode voltage (V_{CM})

- What is the range of input voltage within which the transistors will stay in active region?

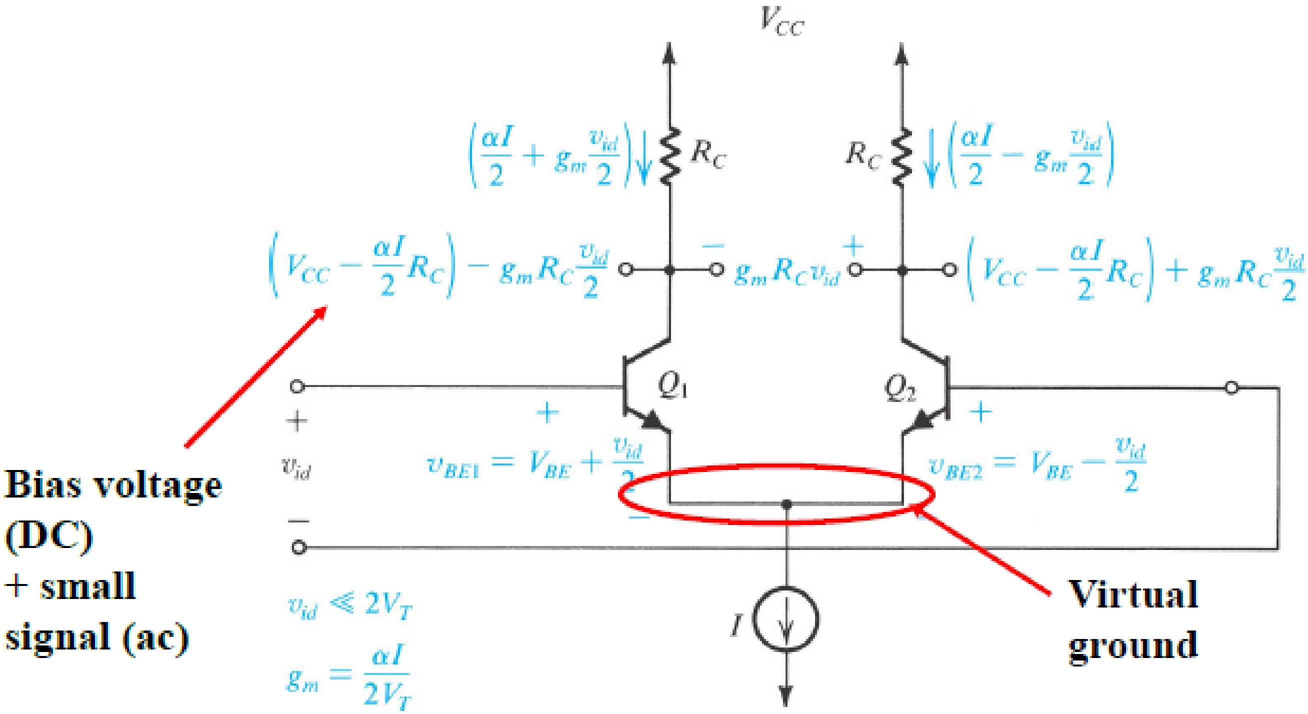
- $V_{CM\_max} = 0.4 + \underbrace{V_{CC} - 0.5\alpha I R_C}_{V_C}$

- $V_{CM\_min} = -V_{EE} + V_{CS} + V_{BE}$

Min voltage need to keep the current mirror in active region



Small Signal Operation



$$g_m = \frac{I_C}{V_T} = \frac{\alpha I}{2V_T}$$

$$i_c = \frac{\alpha I}{2V_T}\frac{v_{id}}{2}$$

$$i_c = g_m \frac{v_{id}}{2}$$

$$i_c = \alpha i_e = \alpha \frac{v_{id}}{2r_e}$$

Differential Gain=2 x single stage gain A_d

If the input differential voltage = $v_{id}/2$ - $(-v_{id}/2)=v_{id}$

then **Differential gain=A_d= $|v_{od}/ v_{id}|$= $g_m(R_C||r_o)$**

Common-Mode Rejection Ratio (CMRR)

CMRR: Figure-of-merit for noise rejection

$$CMRR(dB) = 20log_{10}\left|\frac{A_d}{A_{cm}}\right|$$

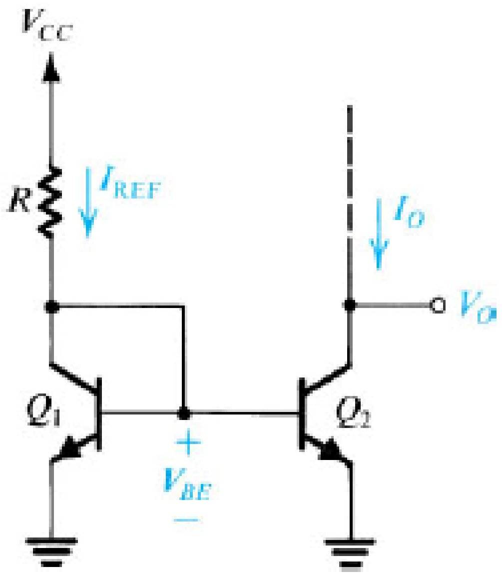
$$A_d = -gmRc$$

$$A_{cm} = -\frac{\alpha \Delta R_C}{2R_{EE} + r_e} = -\left(\frac{R_C}{2R_{EE}}\right)\left(\frac{\Delta R_C}{R_C}\right)$$

$$CMRR = \left|\frac{A_d}{A_{cm}}\right| = (2g_m R_{EE}) \Big/ \left(\frac{\Delta R_C}{R_C}\right)$$

CMRR is the ratio of differential gain over common-mode gain

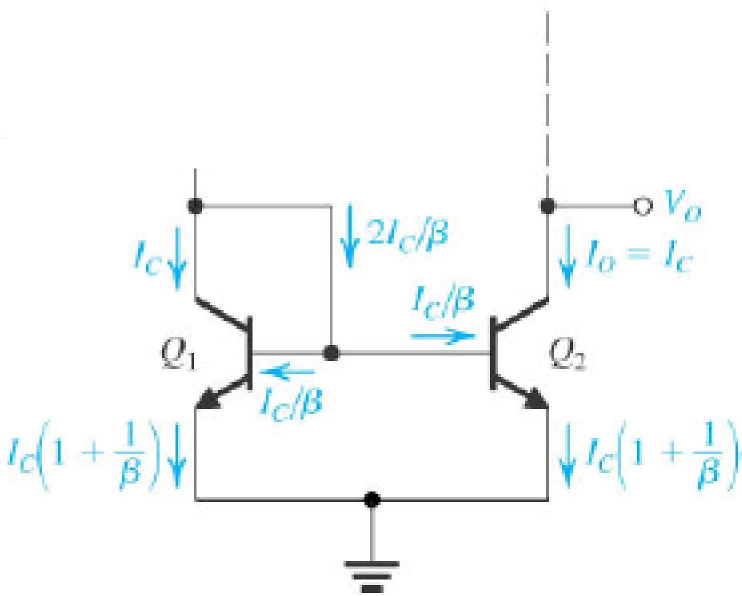
BJT CURRENT MIRRORS



$$I_{REF} = \frac{V_{CC} - V_{BE}}{R}$$

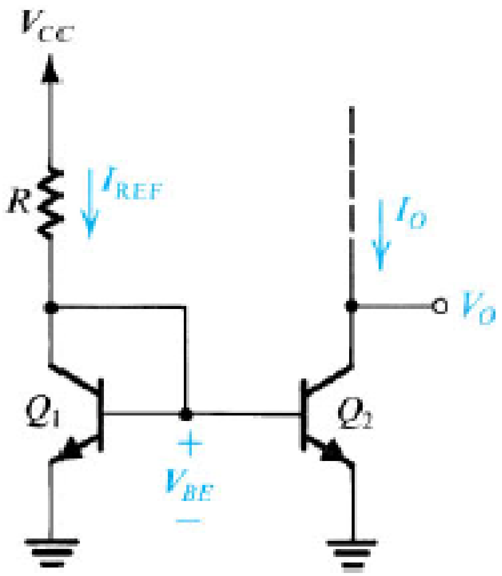
$$I_{REF} = I_C + 2I_C / \beta = I_C\left(1 + \frac{2}{\beta}\right)$$

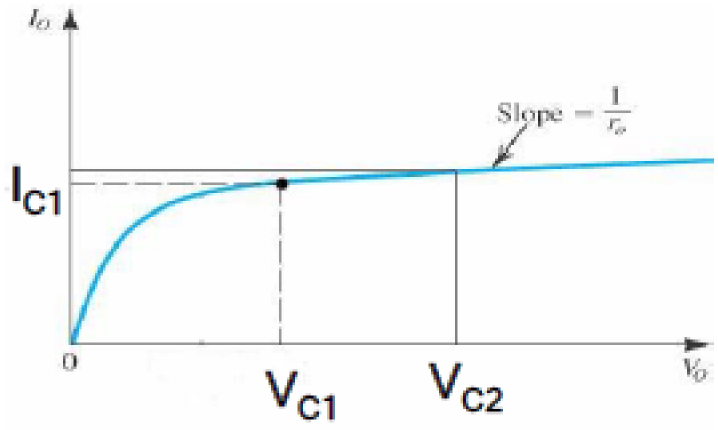
$$\therefore I_o = I_C = I_{REF} \cdot \frac{1}{1 + \frac{2}{\beta}}$$



BJT CURRENT MIRRORS

How does V_O affect I_O?





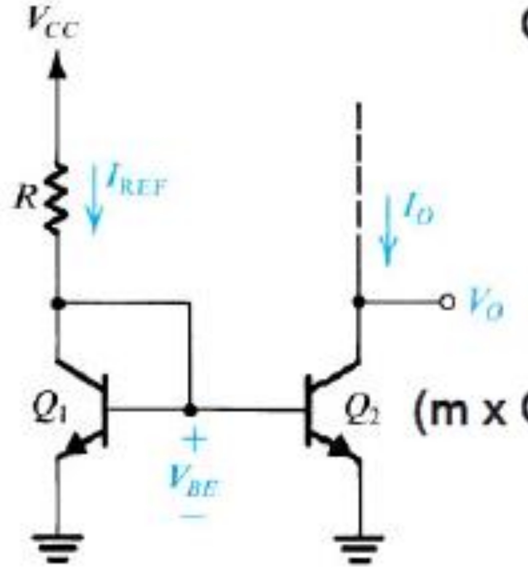
$$I_O = I_{C1} + \frac{V_O - V_{C1}}{r_O}$$

Since $r_O = \frac{V_A}{I_C}$,

$$I_O = I_{C1} + \frac{I_C}{V_A}(V_O - V_{C1}) \simeq I_{C1}(1 + \frac{V_O}{V_A})$$

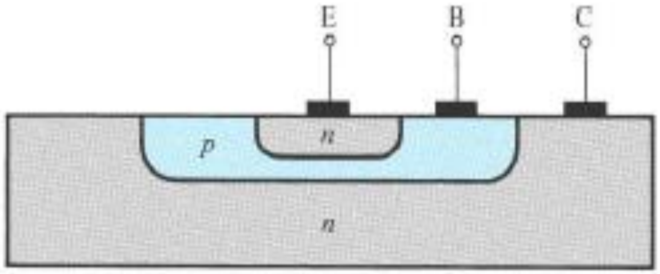
$$= \frac{I_{REF}}{1 + (2/\beta)} \cdot (1 + \frac{V_O}{V_A})$$

BJT CURRENT MIRRORS



(m x Q_1)

Q_2 can have m times larger E-B junction than Q_1



$$I_{REF} = I_{C1} + I_{B1} + I_{B2}$$

$$= I_{C1} + \frac{I_{C1}}{\beta} + m \cdot \frac{I_{C1}}{\beta}$$

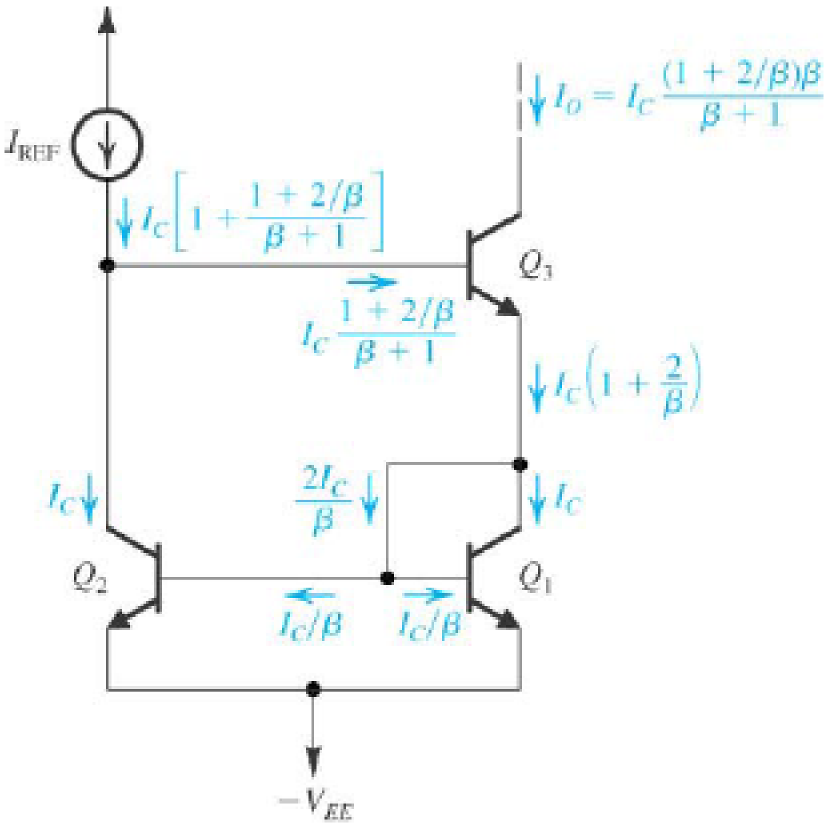
$$= I_{C1}\left(1 + \frac{1+m}{\beta}\right)$$

Since $I_O = m \cdot I_{C1}(1 + \frac{V_O}{V_A})$

$$I_O = \frac{m \cdot I_{REF}}{\left(1 + \frac{1+m}{\beta}\right)}(1 + \frac{V_O}{V_A})$$

WILSON CURRENT MIRROR

Reduce β dependence



Wilson current mirror

$$I_O = I_C \frac{(1 + 2/\beta)\beta}{\beta + 1}$$

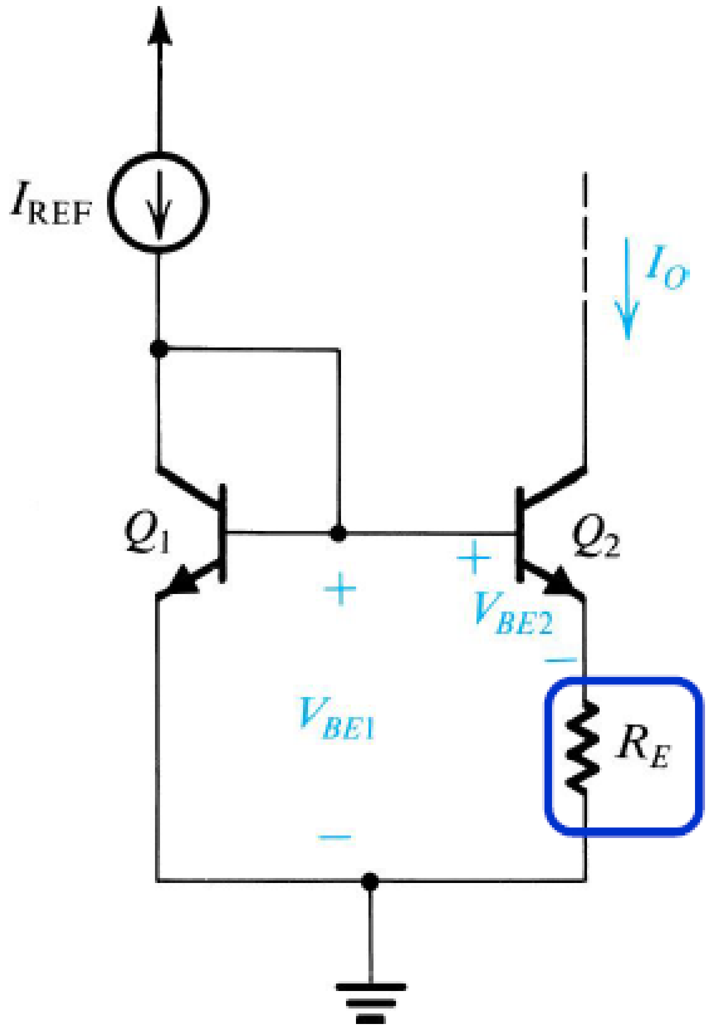
$$I_{REF} = I_C\left[1 + \frac{1 + 2/\beta}{\beta + 1}\right]$$

$$\frac{I_O}{I_{REF}} = \frac{\beta + 2}{\beta + 1 + 1 + 2/\beta} = \frac{1}{1 + \frac{2}{\beta(\beta + 2)}}$$

$$\cong \frac{1}{1 + 2/\beta^2}$$

Widlar Current Mirror

- A resistor R_E is included in the emitter of Q_2



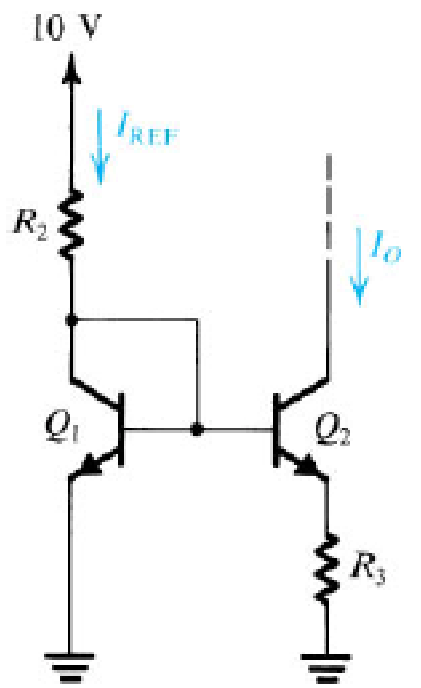
1) This CM can provide very small ***Io***
2) The output resistance can be very high (an ideal current source has infinite resistance)

Design Equations?

WIDLAR CURRENT SOURCE

Example 6.14

Determine R_1 for I_O= 10µA. Q_1, Q_2 have V_{BE}=0.7V for I_C=1mA.



Widlar current source

$$V_{BE1} = V_T \ln\left(\frac{I_{E1}}{I_S}\right) \simeq V_T \ln\left(\frac{I_{REF}}{I_S}\right), \; V_{BE2} = V_T \ln\left(\frac{I_O}{I_S}\right)$$

$$V_{BE1} - V_{BE2} = V_T \ln\left(\frac{I_{REF}}{I_O}\right)$$

$$V_{BE1} = V_{BE2} + I_O R_E$$

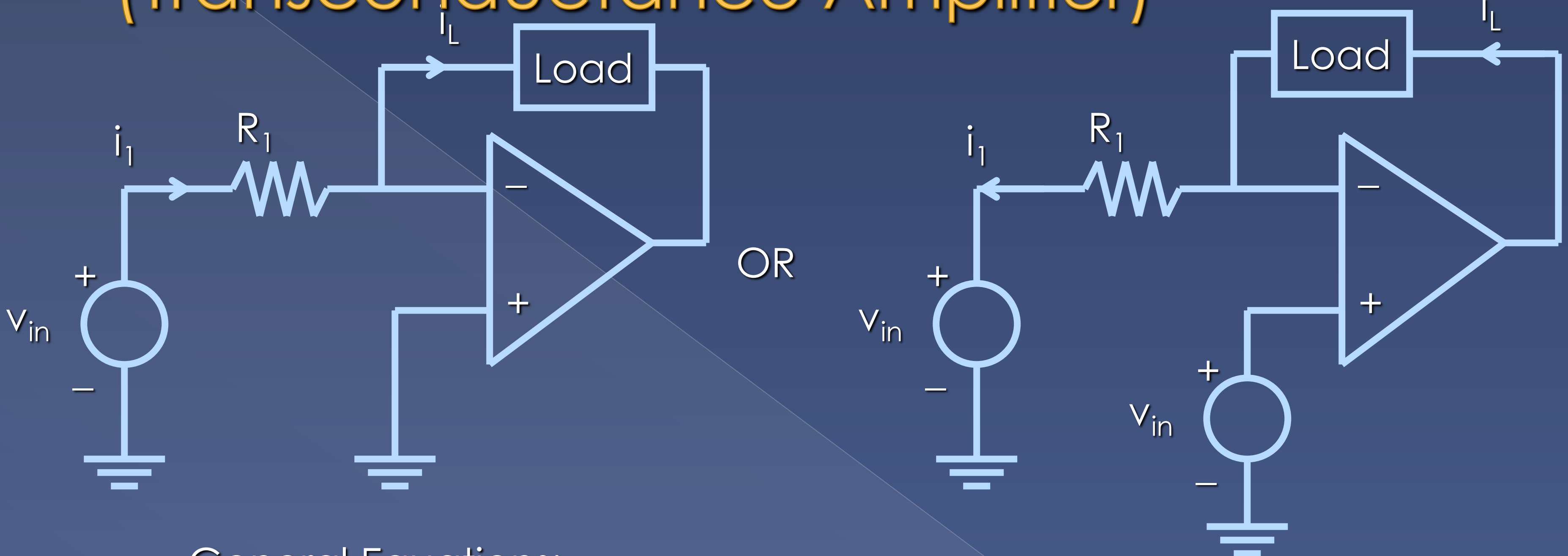
$$\therefore I_O R_3 = V_T \ln\left(\frac{I_{REF}}{I_O}\right)$$

$$\text{For } I_{REF} = 1\text{mA}, \; R_2 = \frac{10 - 0.7}{1} = 9.3\text{k}\Omega$$

$$10 \times 10^{-6} R_3 = 0.025 \ln\left(\frac{1\text{mA}}{10\mu\text{A}}\right)$$

$$R_3 = 11.5\text{k}\Omega$$

Voltage to Current Converter (Transconductance Amplifier)



General Equations:

$i_L = i_1 = v_1/R_1$

$v_1 = v_{in}$

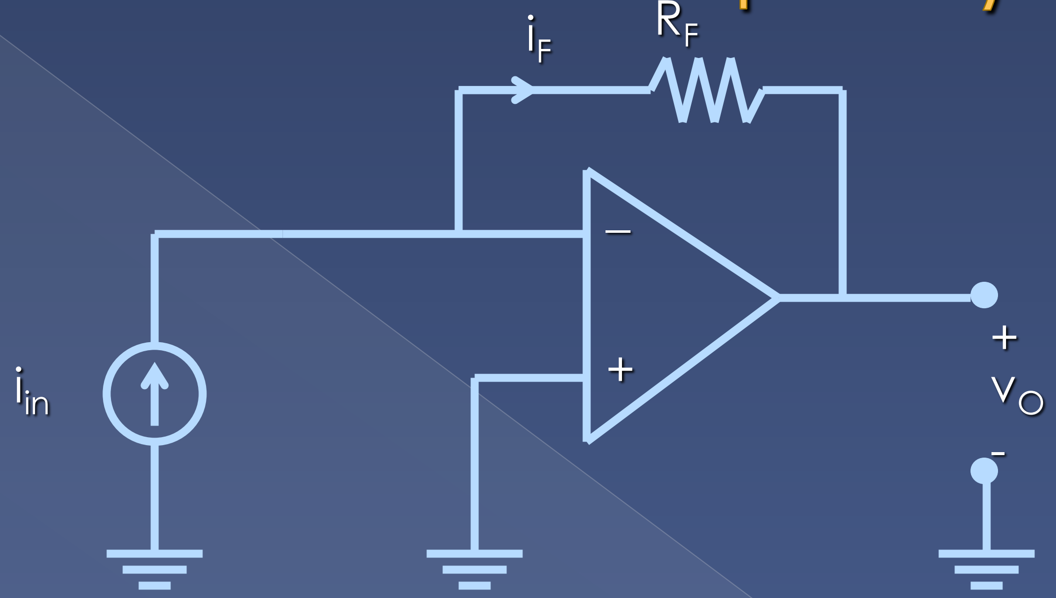
The transconductance, $g_m = i_o/v_{in} = 1/R_1$

Therefore, $i_L = i_1 = v_{in}/R_1 = g_m v_{in}$

The maximum load resistance is determined by:

$R_{L(max)} = v_{o(max)}/i_L$

Current to Voltage Converter (Transresistance Amplifier)



<u>General Equations:</u>

$i_F = i_{in}$

$v_o = -i_F R_F$

$r_m = v_o/i_{in} = R_F$

Nonlinear Op-Amp Circuits

- Most typical applications require op amp and its components to act linearly
  - I-V characteristics of passive devices such as resistors, capacitors should be described by linear equation (Ohm's Law)
  - For op amp, linear operation means input and output voltages are related by a constant proportionality (A_v should be constant)
- Some application require op amps to behave in nonlinear manner (logarithmic and antilogarithmic amplifiers)

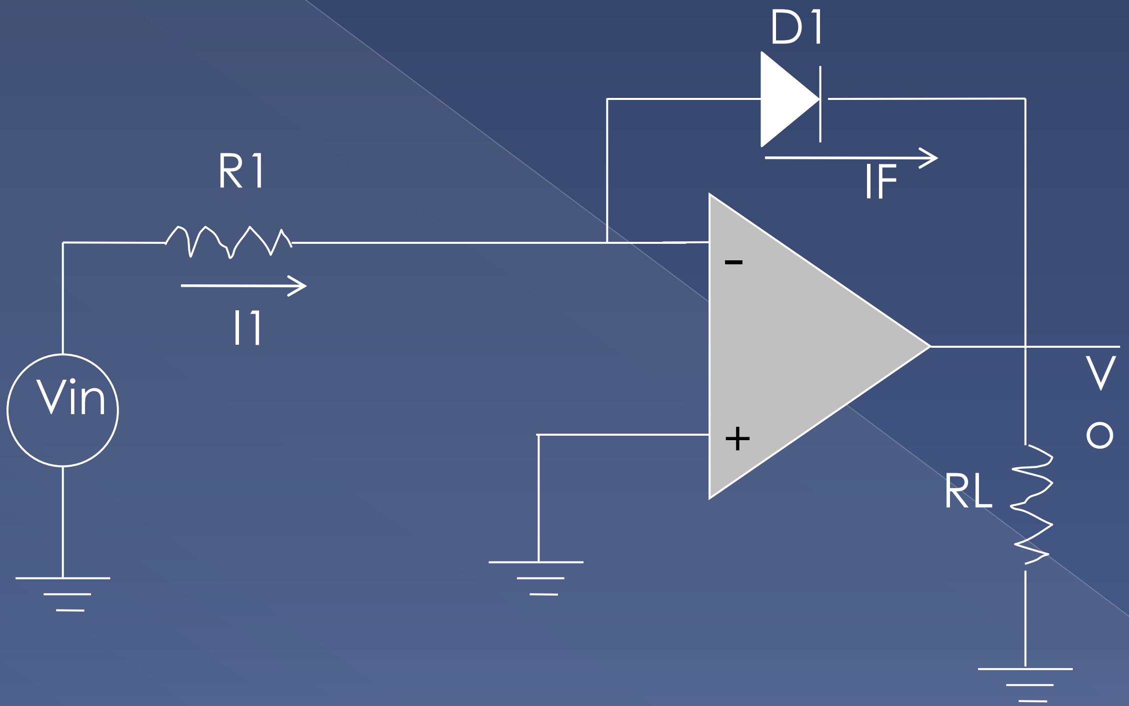
Logarithmic Amplifier

- Output voltage is proportional to the logarithm of input voltage
- A device that behaves nonlinearly (logarithmically) should be used to control gain of op amp
  - Semiconductor diode
- Forward transfer characteristics of silicon diodes are closely described by Shockley's equation

  $$I_F = I_S\, e^{(V_F/\eta V_T)}$$

  - I_S is diode saturation (leakage) current
  - e is base of natural logarithms (e = 2.71828)
  - V_F is forward voltage drop across diode
  - V_T is thermal equivalent voltage for diode (26 mV at 20°C)
  - η is emission coefficient or ideality factor (2 for currents of same magnitude as I_S to 1 for higher values of I_F)

Basic Log Amp operation

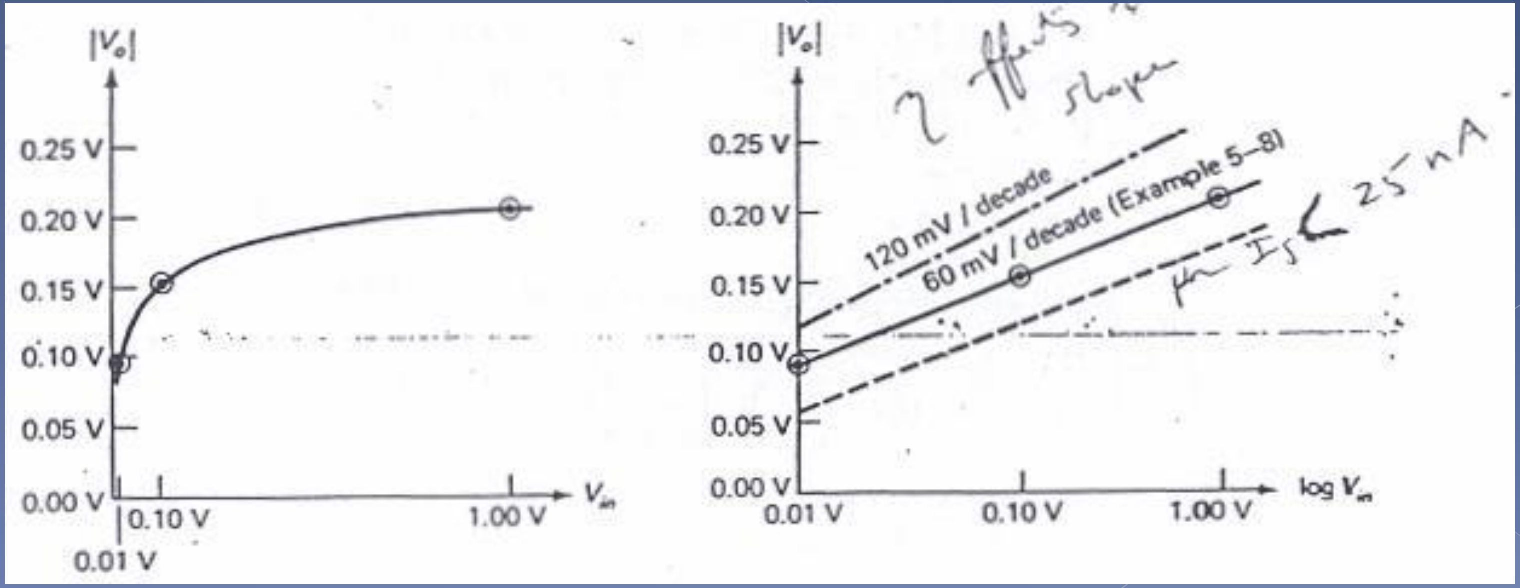


- $I_1 = V_{in}/R_1$
- $I_F = - I_1$
- $I_F = - V_{in}/R_1$
- $V_0 = -V_F = -\eta V_T \ln(I_F/I_S)$
- $V_0 = -\eta V_T \ln[V_{in}/(R_1 I_S)]$
- $r_D = 26 \text{ mV} / I_F$
- $I_F < 1$ mA (log amps)

- At higher current levels ($I_F > 1$ mA) diodes begin to behave somewhat linearly

Logarithmic Amplifier…

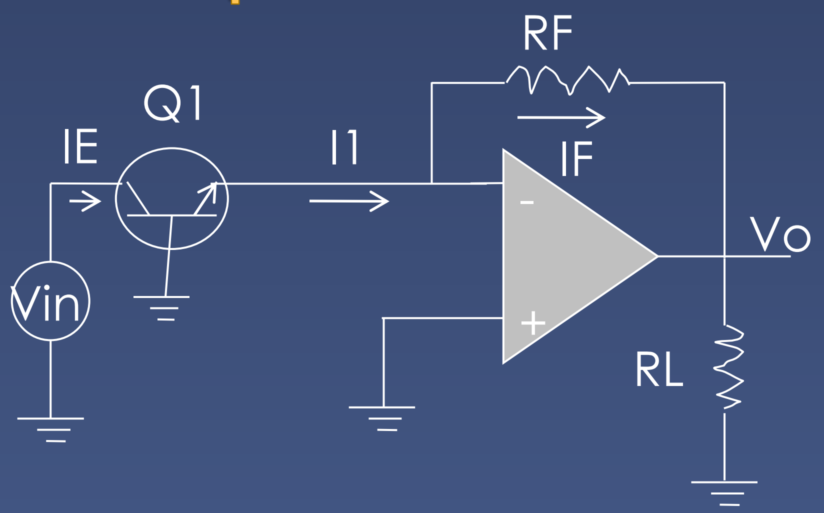
- Linear graph: voltage gain is very high for low input voltages and very low for high input voltages
- Semilogarithmic graph: straight line proves logarithmic nature of amplifier's transfer characteristic
- Transfer characteristics of log amps are usually expressed in terms of slope of V_0 versus V_{in} plot in milivolts per decade
- η affects slope of transfer curve; I_S determines the y intercept



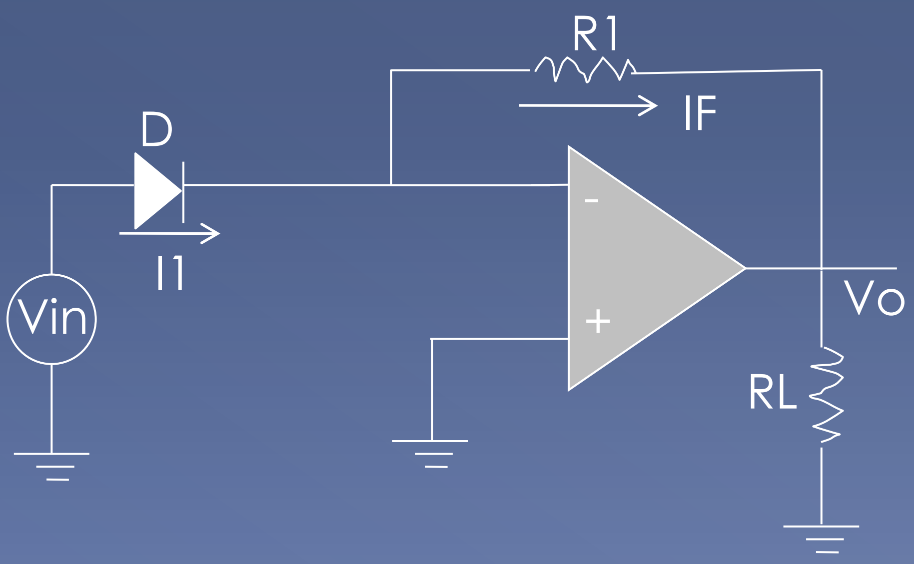
Antilogarithmic Amplifier

- Output of an antilog amp is proportional to the antilog of the input voltage
- with diode logging element
  - $V_0 = -R_F I_S e^{(V_{in}/V_T)}$
- With transdiode logging element
  - $V_0 = -R_F I_{ES} e^{(V_{in}/V_T)}$
- As with log amp, it is necessary to know saturation currents and to tightly control junction temperature

Antilogarithmic Amplifier…



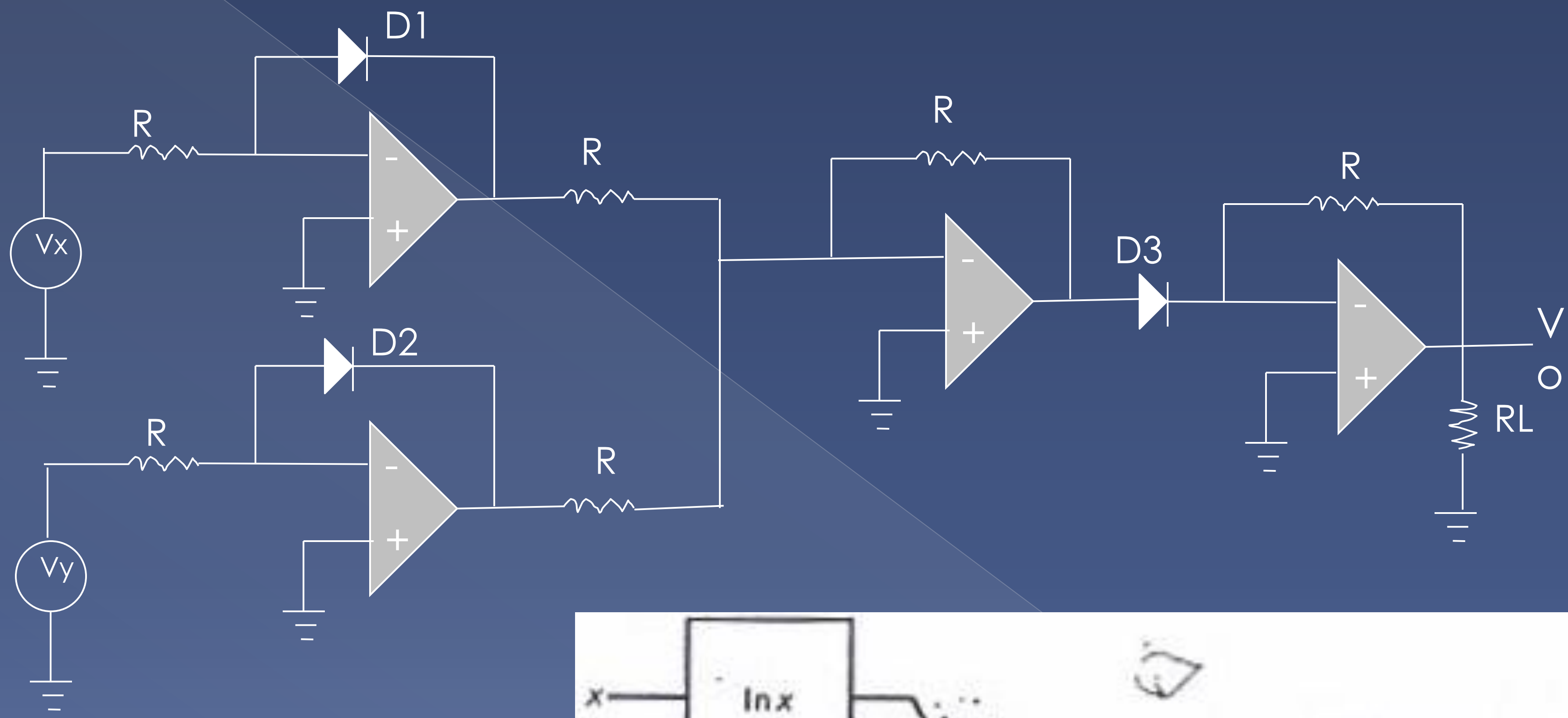
(a = 1) I1 = IC = IE

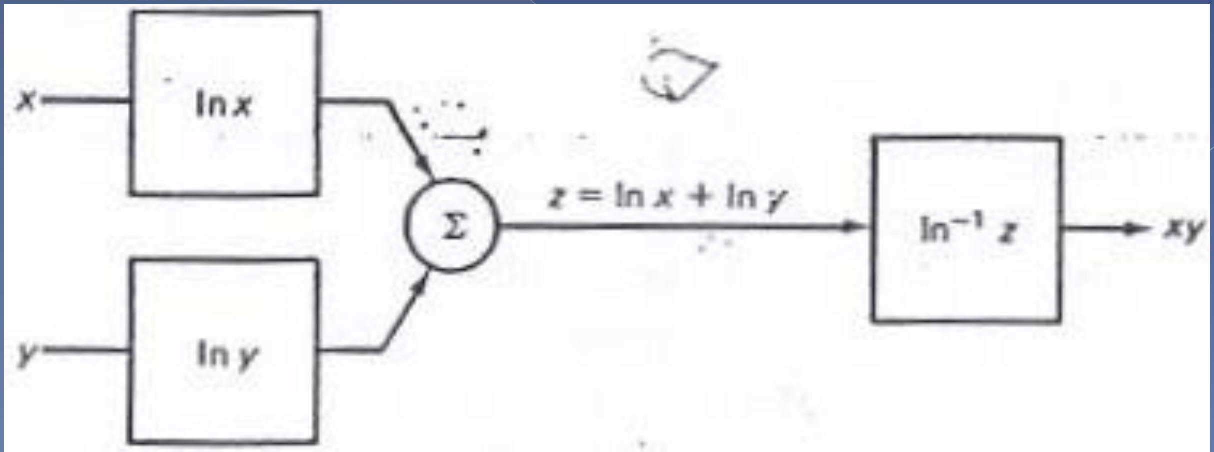


Logarithmic Amplifier Applications

- Logarithmic amplifiers are used in several areas
  - Log and antilog amps to form analog multipliers
  - Analog signal processing
- Analog Multipliers
  - $\ln xy = \ln x + \ln y$
  - $\ln (x/y) = \ln x - \ln y$

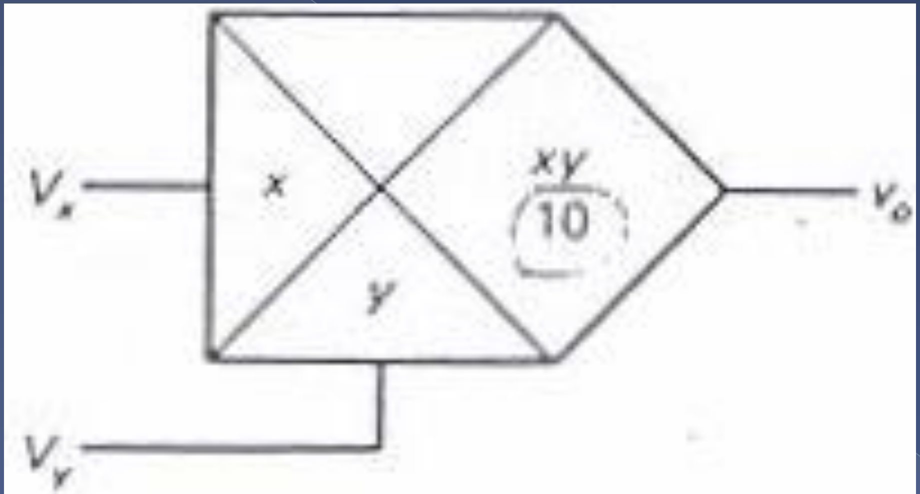
Analog Multipliers





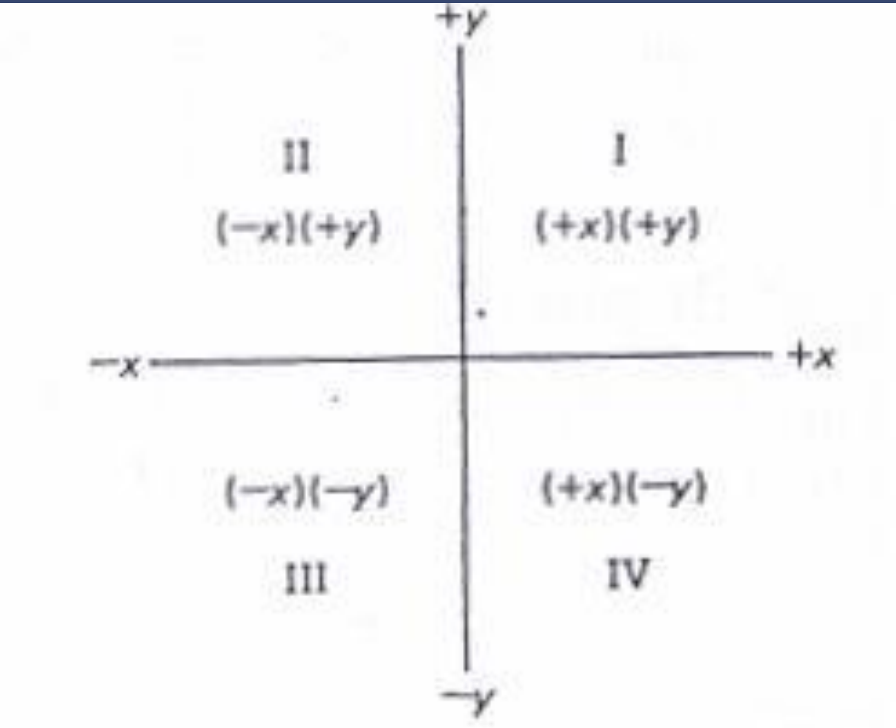
One-quadrant multiplier: inputs must both be of same polarity

Analog Multipliers…



General symbol

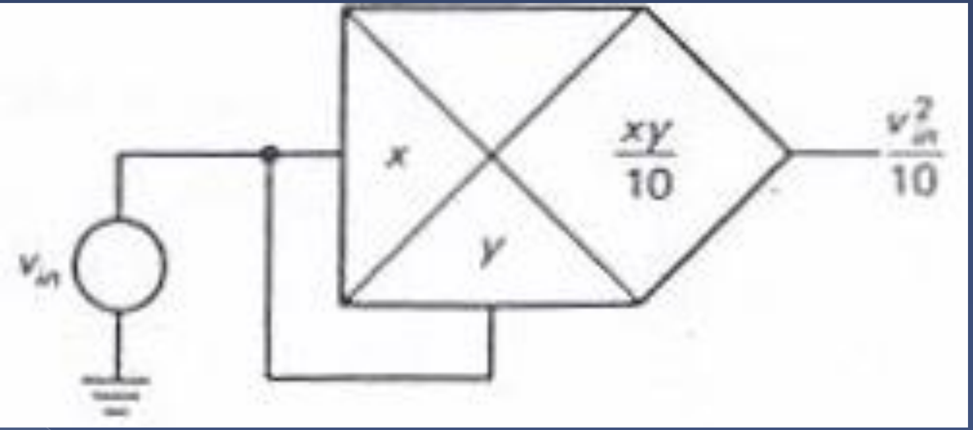
Four quadrants of operation



Two-quadrant multiplier: one input should have positive voltages, other input could have positive or negative voltages
Four-quadrant multiplier: any combinations of polarities on their inputs

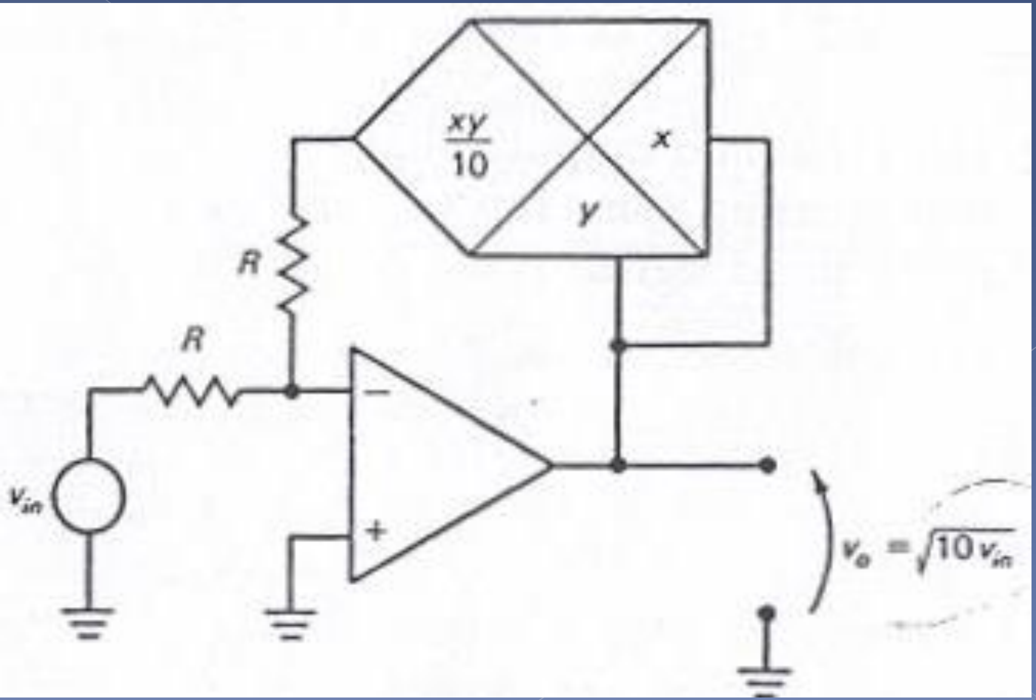
Analog Multipliers…

Squaring Circuit



Implementation of mathematical operations

Square root Circuit



OP-AMP COMPARATORS

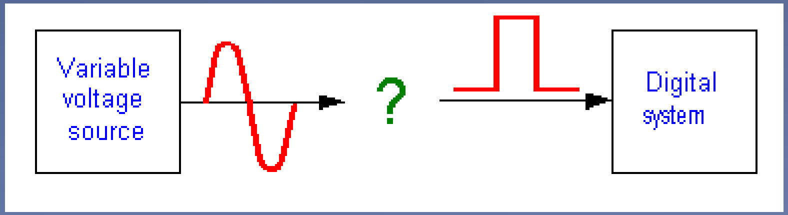
- Function:

Compares two input voltages and produces an output in either of two states indicating the greater than or less than relationship of the inputs.

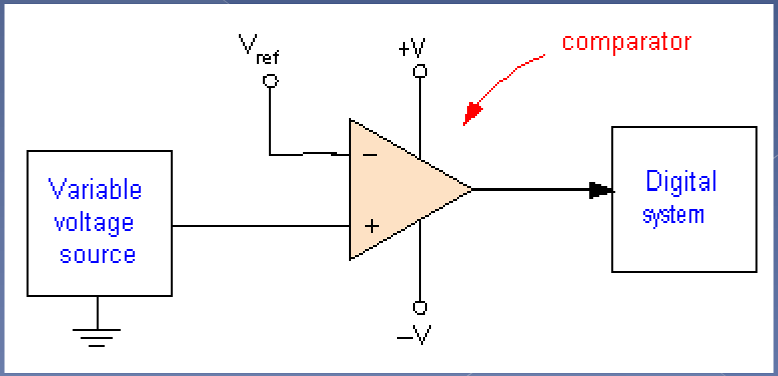
What is a Comparator ?

- The comparator is an op-amp circuit that compares two input voltages and produces an output indicating the relationship between them. The inputs can be two signals (such as two sine waves) or a signal and a fixed dc reference voltage.
- Often used as an interface between digital and analog signals.

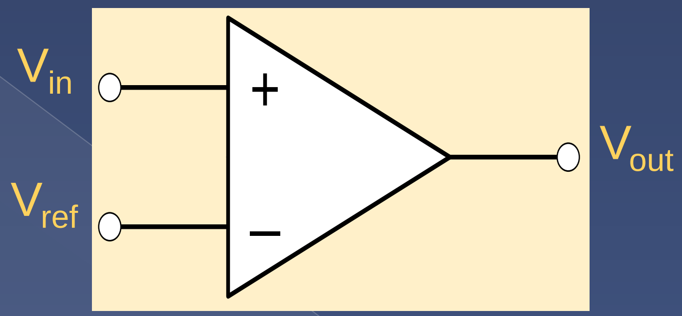
Problem

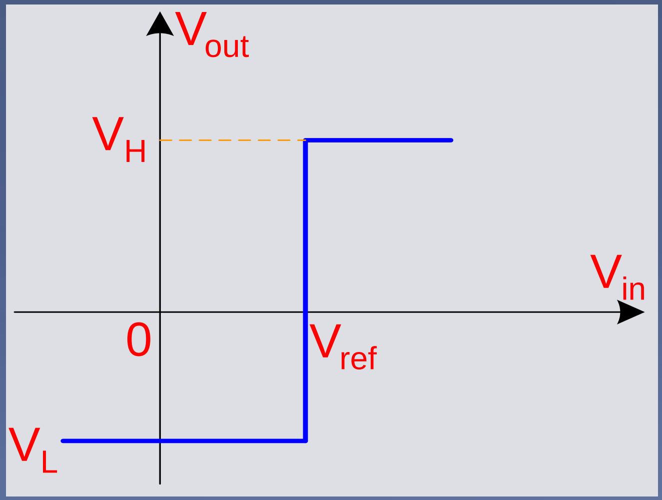


Solution

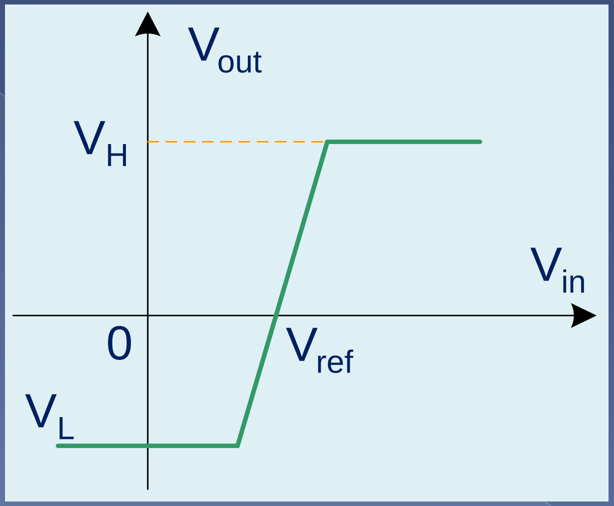


Symbol & Transfer Characteristics





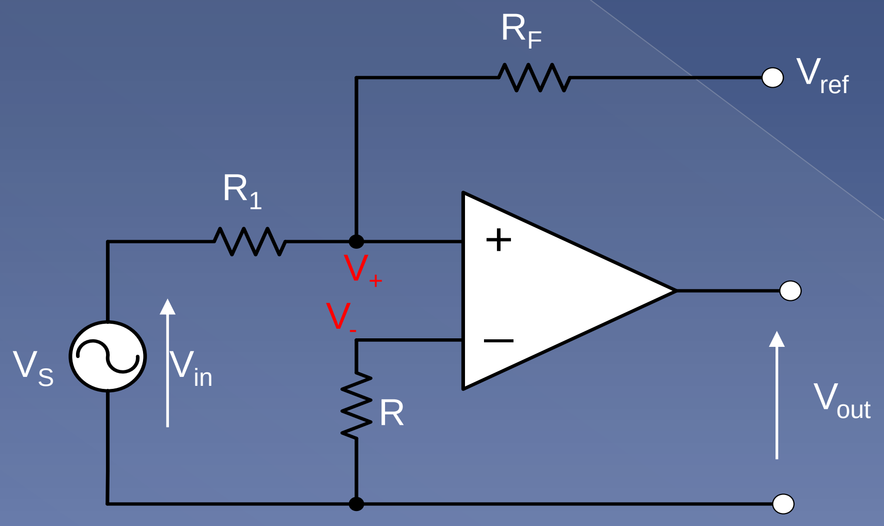
Ideal transfer characteristic



Practical transfer characteristic

Threshold Comparators

- The voltage at which a comparator changes from one level to another is called the *crossover* (or *threshold*) voltage.
- Its value can be adjusted by adding resistors, as shown in the non-inverting comparator.



From the superposition theorem, the voltage at V_+ is given by

$$V_+ = \frac{R_1}{R_1 + R_F} V_{ref} + \frac{R_F}{R_1 + R_F} V_{in}$$

Ideally, the *crossover* will occur when $V_+ = 0$.
That is

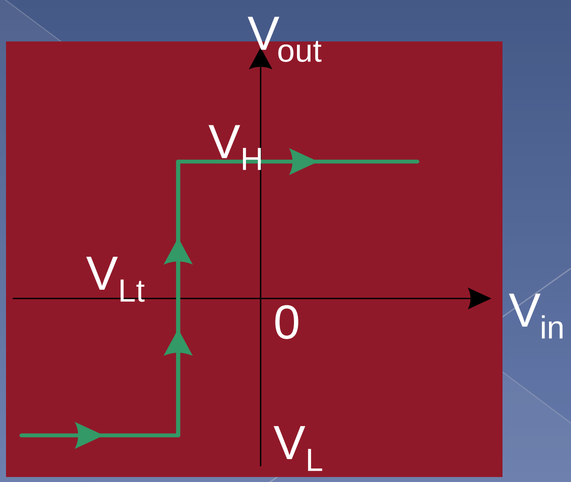
$$R_1 V_{ref} + R_F V_{in} = 0$$

which gives the low threshold voltage $V_{Lt} = V_{in}$ as

$$V_{Lt} = -\frac{R_1}{R_F} V_{ref}$$

Thus, the output voltage becomes high (V_H) at the positive saturation voltage.

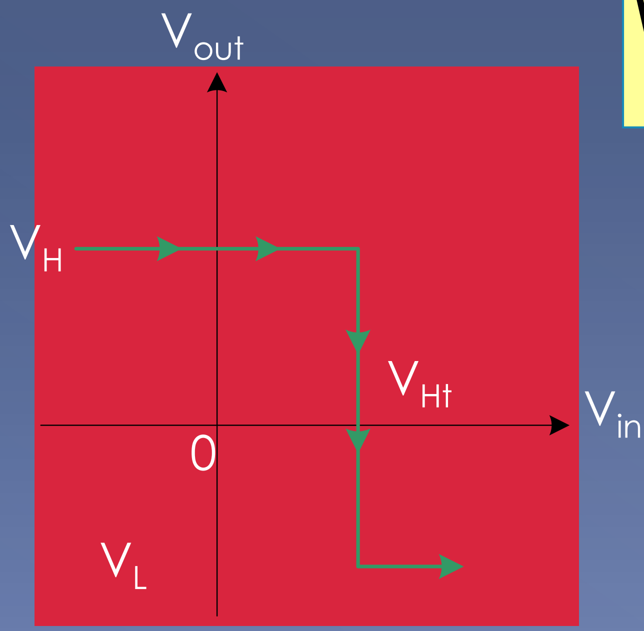
($+V_{sat}$) when $V_+ > 0$ (i.e. $V_{in} > V_{Lt}$)



- If the input signal is connected to the inverting terminal, the output will change from high (V_H) to low (V_L).

The high threshold voltage $V_{Ht} = V_{in}$ is given by

$$V_{Ht} = \frac{R_1}{R_1 + R_F} V_{ref}$$



Thus, the output voltage becomes low (V_L) at the negative saturation voltage :-

($-V_{sat}$) when $V_{in} > V_+$ (i.e. $V_{in} > V_{Ht}$)

BASIC COMPARATOR CIRCUITS

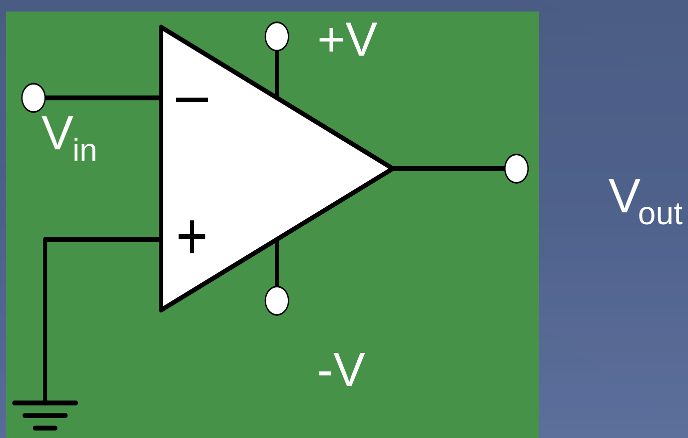
- COMPARATOR WITH ZERO REFERENCE
- COMPARATOR WITH NONZERO REFERENCE
- COMPARATOR WITH HYSTERESIS

NONLINEAR CIRCUITS

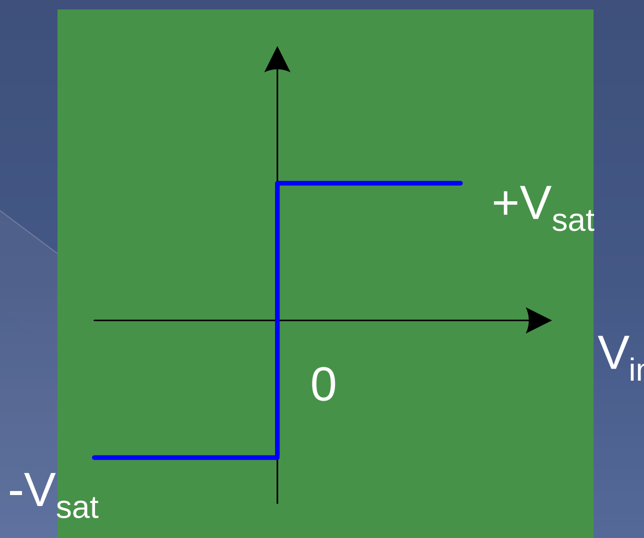
- Nonlinear circuits such as comparators, wave shapers and active-diode circuits.
- Linear circuits like voltage amplifier, current sources, and active filters.
- The output of nonlinear op-amp circuits usually has a different shape from the input signal. This is due to the op-amp saturates during part of the input cycle.

ZERO REFERENCE

- The simplest way to build a comparator is to connect op-amp without feedback resistors.



a) Comparator with zero reference



b) Input/output response

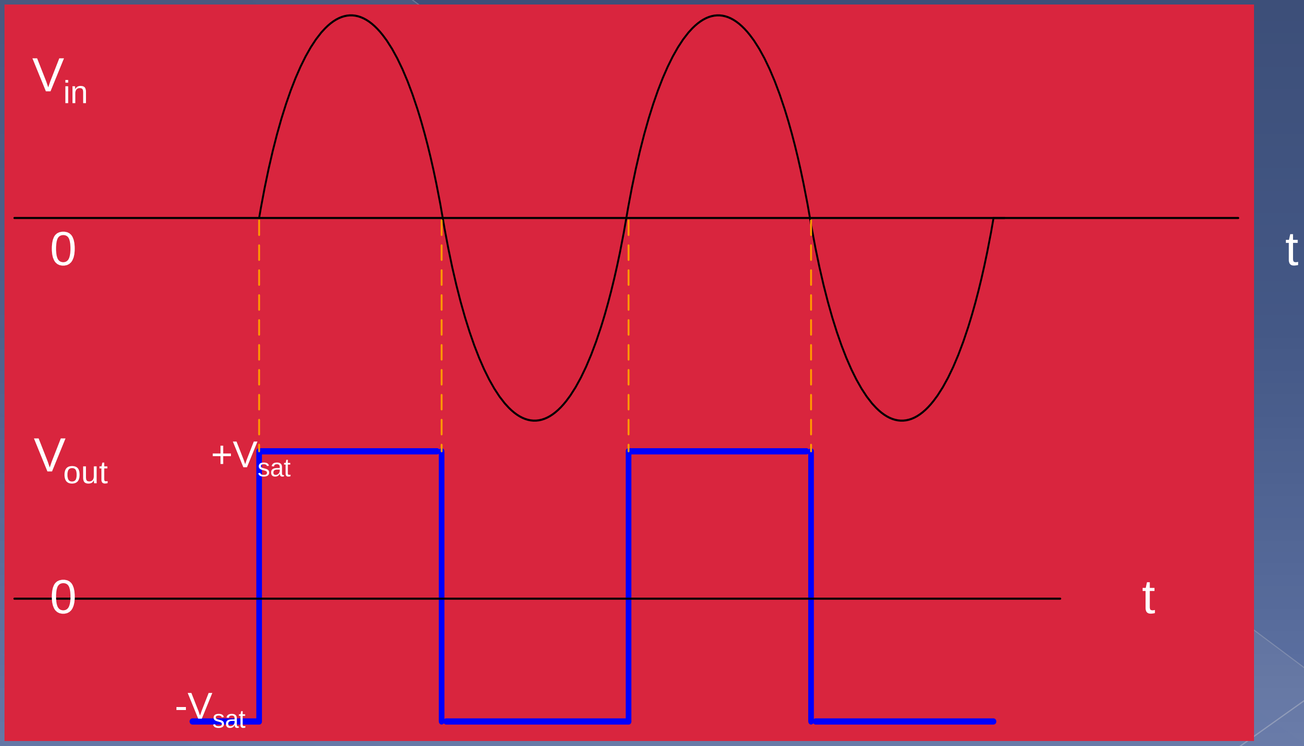
ZERO REFERENCE

- **Because of the high open-loop gain, positive input voltage produces positive saturation ($+V_{sat}$), and a negative input voltage produces negative saturation ($-V_{sat}$).**
- **This comparator is called a *zero-crossing detector.***
- **The minimum input voltage that produces saturation is:**

$$V_{in}(\min) = \frac{\pm V_{sat}}{A_{ol}}$$

ZERO REFERENCE

- If a sinusoidal input voltage applied to the non-inverting input of this circuit, the result will look like this:



ZERO REFERENCE

- **Let V_{sat} = 15V, A_{ol} = 100,000. Then the input voltage needed to produce saturation is:**

$$V_{in}(\min) = \frac{\pm 15V}{100{,}000} = \pm 0.015mV$$

V_{in} > +0.015 mV ⇨ +V_{sat}

V_{in} < -0.015 mV ⇨ -V_{sat}

ZERO REFERENCE

- The output is a two-state output, either $+V_{sat}$ or $-V_{sat}$
- This comparator can be used as a *squaring* circuit (i.e. produce square wave from sine wave).

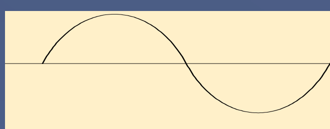
ZERO REFERENCE

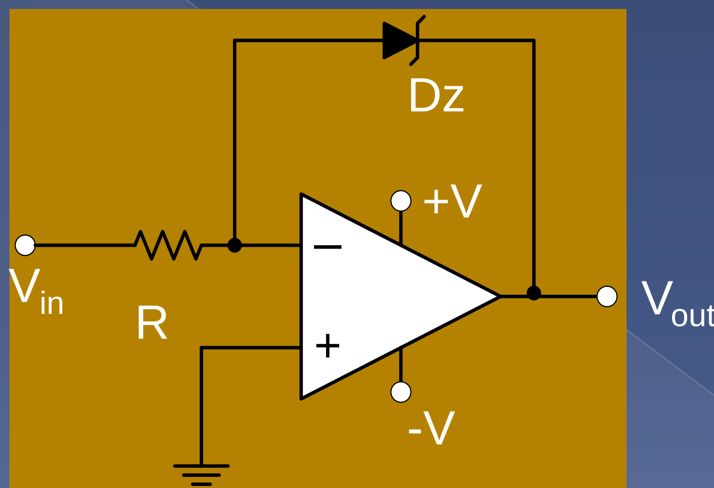
Bounded Output

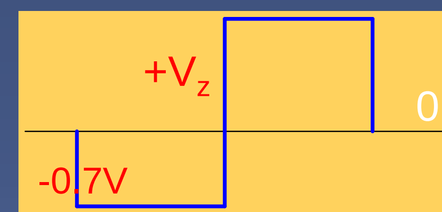
- The output swing of a zero-crossing detector may be too large in some applications.
- We can bound the output by using a zener diode.
- There are three types:
  1. Bounded at positive value
  2. Bounded at negative value
  3. Double bounded

ZERO REFERENCE

1.Bounded at positive value

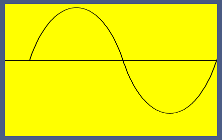


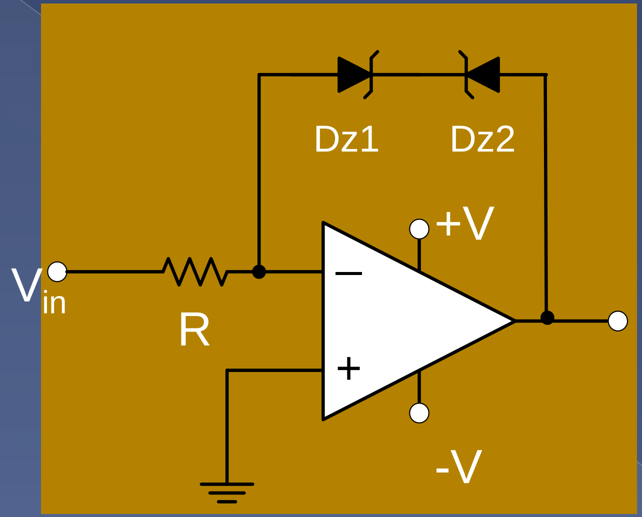




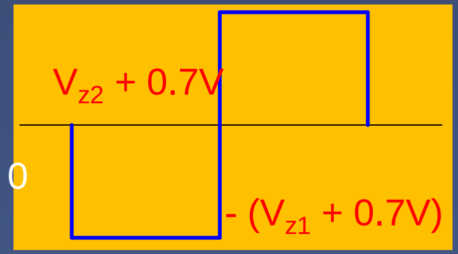
ZERO REFERENCE

3.Double-bounded





V_{out}

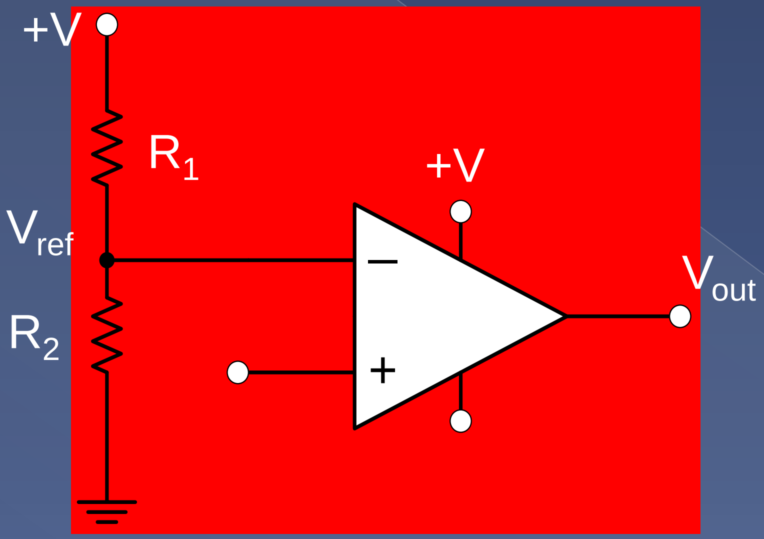


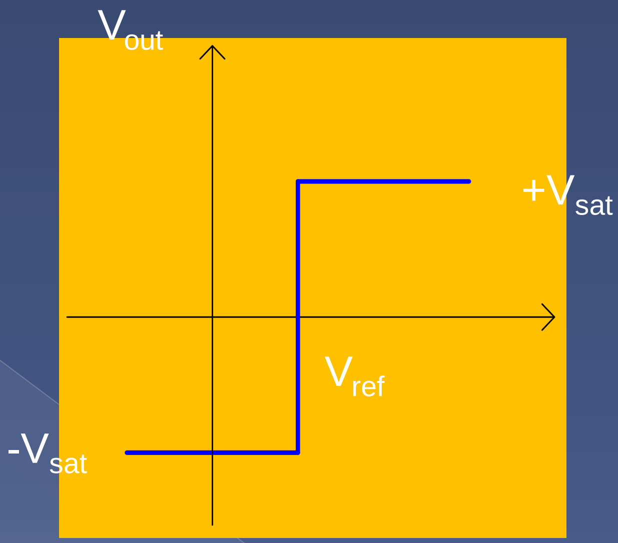
NON-ZERO REFERENCES

- In some applications a ***threshold voltage different from zero*** may be preferred. By biasing either input, we can change the threshold voltage as needed.
- It also known as ***non-zero level detection***

NON-ZERO REFERENCES

Positive Threshold





$$V_{ref} = \frac{R_2}{R_1 + R_2}(+V)$$

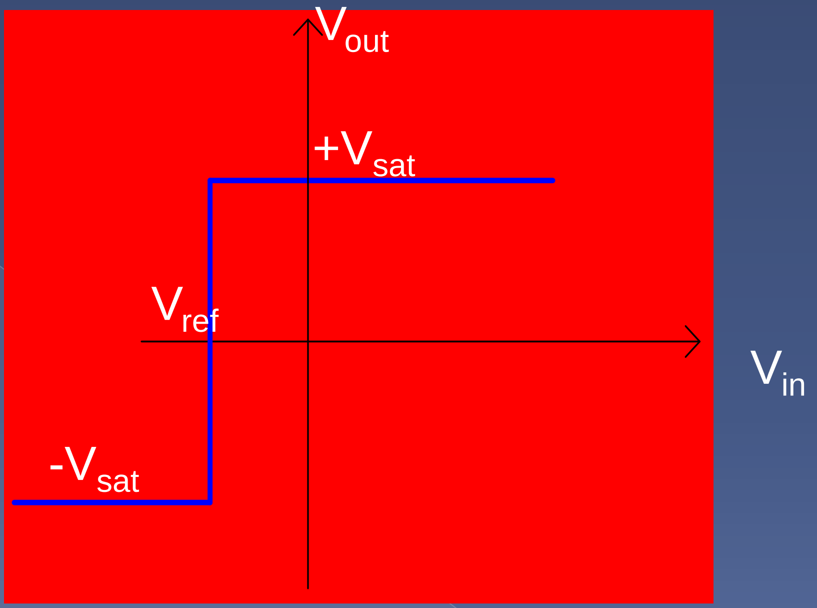
- When Vin > Vref, Vout is High (+Vsat)
- When Vin < Vref, Vout is Low (-Vsat)

NON-ZERO REFERENCES

Negative threshold

- **If a negative limit is preferred, connect –V to the voltage divider.**

$$V_{ref} = \frac{R_2}{R_1 + R_2}(-V)$$



- When Vin > Vref, Vout is High (+Vsat)
- When Vin < Vref, Vout is Low (-Vsat)

NON-ZERO REFERENCES

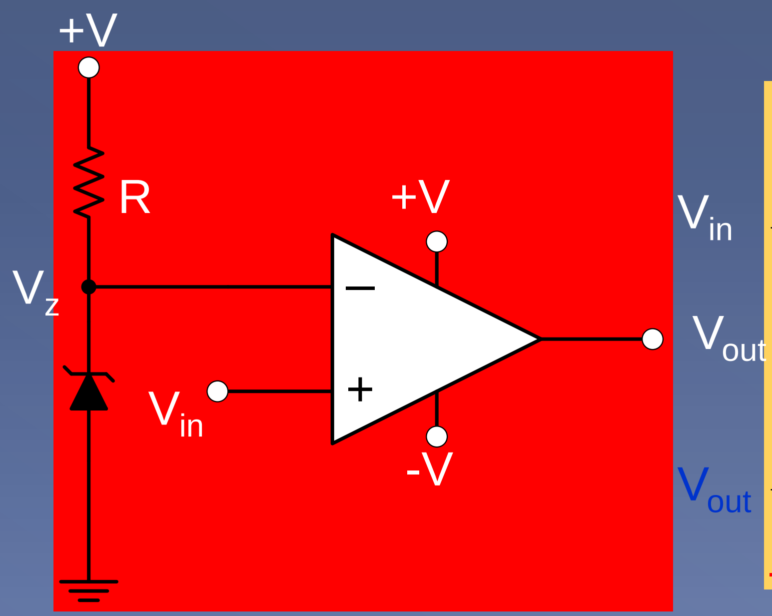
Using Zener diode

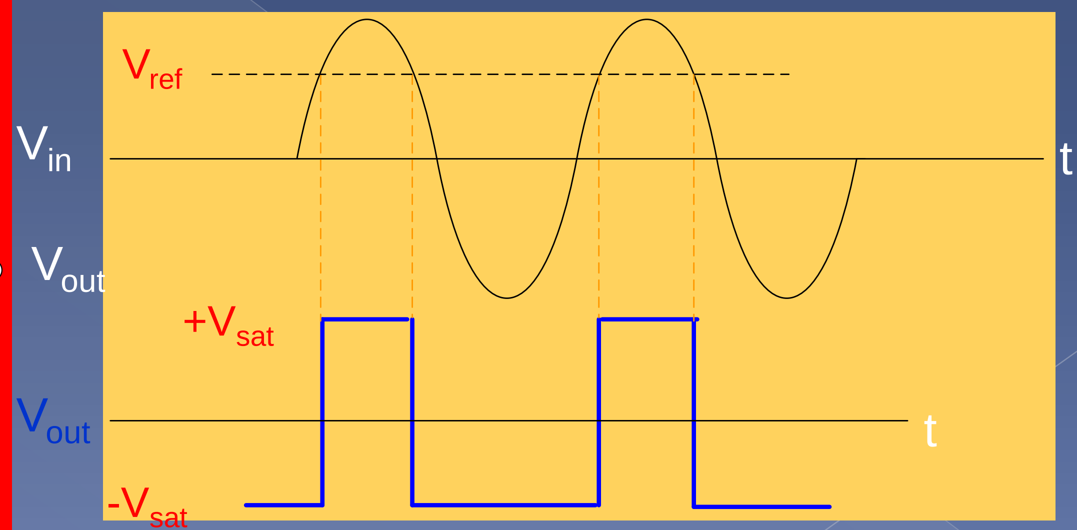
CONDITIONS:

• Vref = Vz

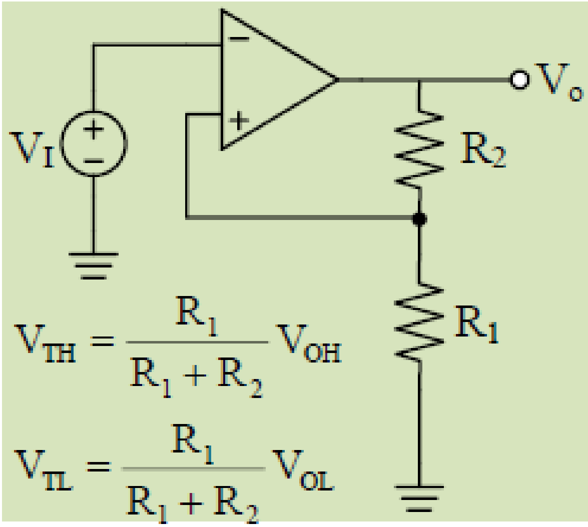
•When Vin is less than Vref, the output remains at the max negative level

•When Vin is more than Vref, the output goes to the max positive level



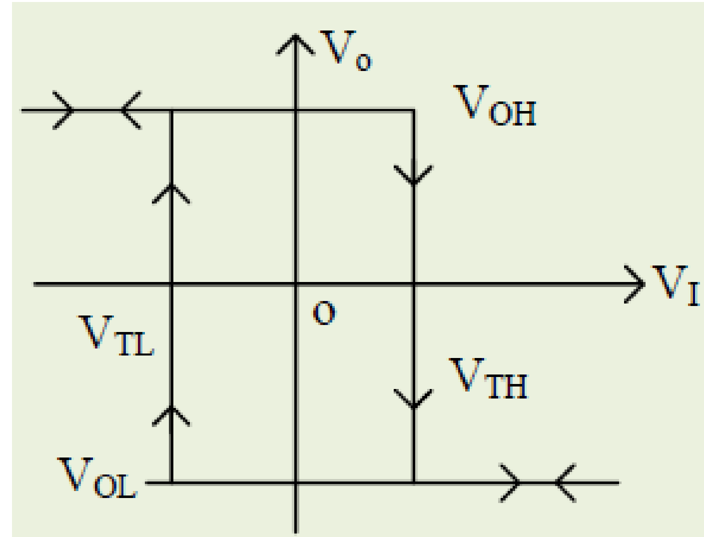


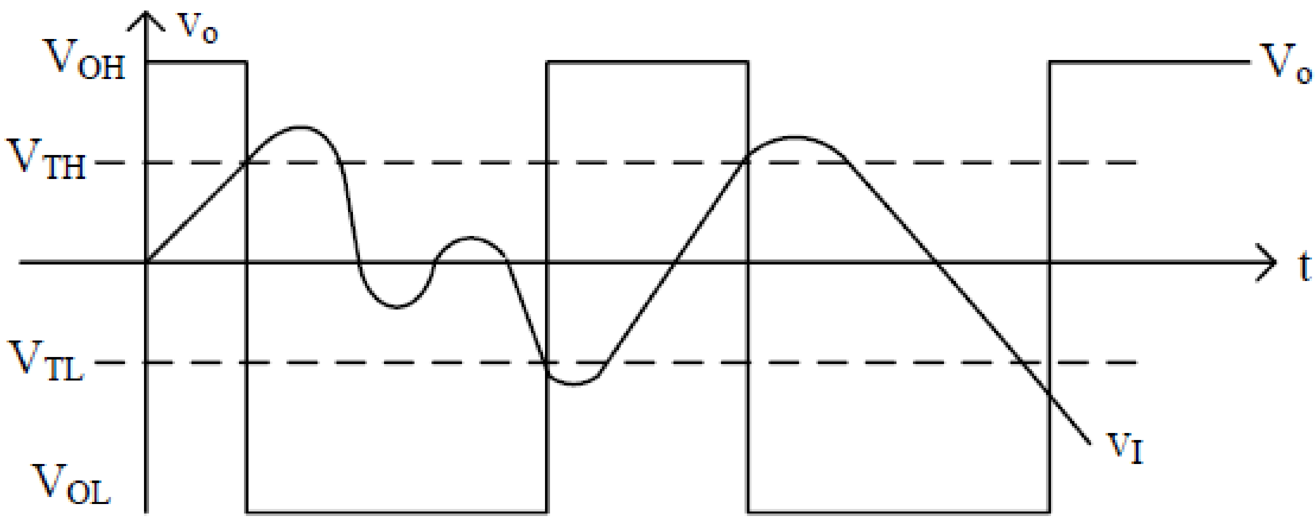
Inverting Schmitt Trigger



$$V_{TH} = \frac{R_1}{R_1 + R_2} V_{OH}$$

$$V_{TL} = \frac{R_1}{R_1 + R_2} V_{OL}$$





Inverting Schmitt Trigger...

$$V_{TH} = \frac{R_1}{R_1 + R_2} V_{OH} \quad \text{or} \quad V_{OH} = \left(1 + \frac{R_2}{R_1}\right) V_{TH}$$

$$V_{TL} = \frac{R_1}{R_1 + R_2} V_{OL} \quad \text{or} \quad V_{OL} = \left(1 + \frac{R_2}{R_1}\right) V_{TL}$$

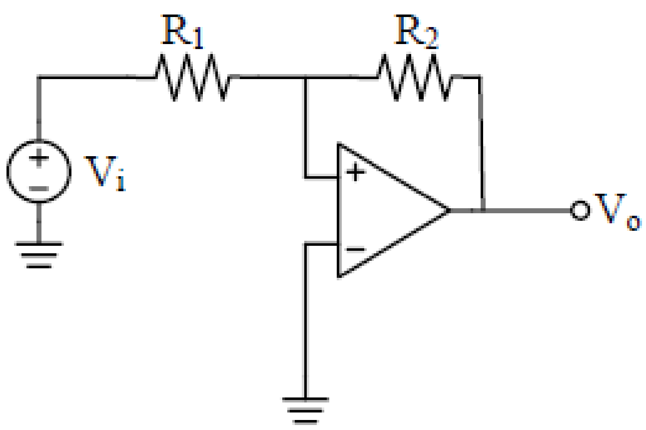
Hysteresis (window) Width:

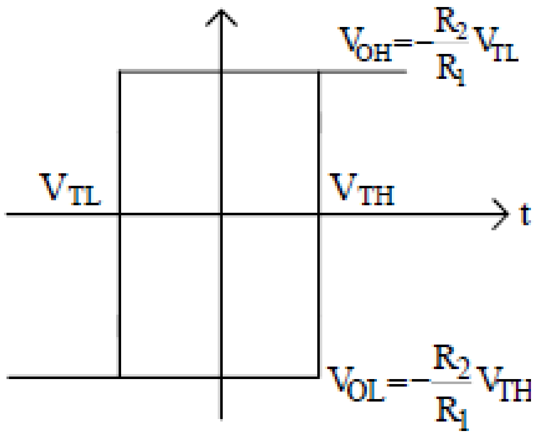
$$\Delta V_T = V_{TH} - V_{TL} = \frac{R_1}{R_1 + R_2} (V_{OH} - V_{OL})$$

or

$$V_{OH} - V_{OL} = \left(1 + \frac{R_2}{R_1}\right) \Delta V_T$$

Non-Inverting Schmitt Trigger



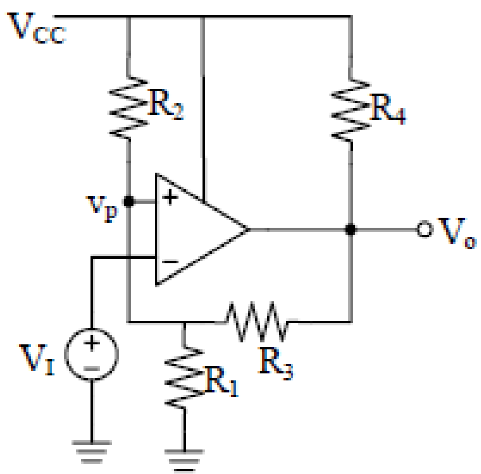


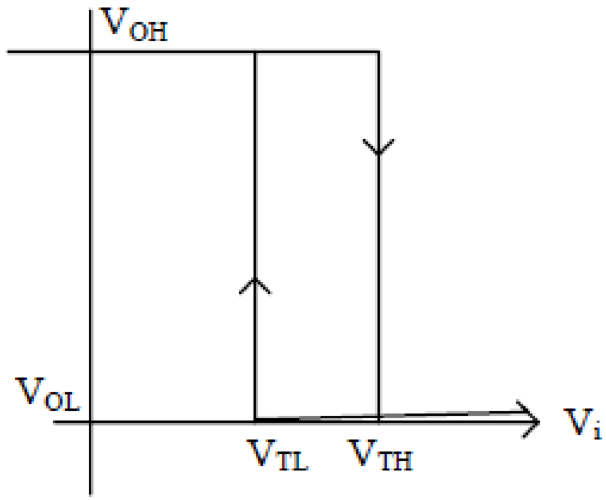
$$V_{TH} = -\frac{R_1}{R_2} V_{OL} \Leftarrow \frac{V_{TH} - 0}{R_1} = \frac{0 - V_{OL}}{R_2}$$

$$V_{TL} = -\frac{R_1}{R_2} V_{OH}$$

$$\Delta V_T = \frac{R_1}{R_2}\left(V_{OH} - V_{OL}\right) \quad \text{Hysteresis Window}$$

Schmitt Trigger in I/O in first quadrant and having a single supply.





Using Superposition

$$V_p = \frac{R_{1,3}}{R_{1,3} + R_2} V_{CC} + \frac{R_{1,2}}{R_{1,2} + R_3} V_o$$

where $R_{1,3} = R_1 // R_3$ and $R_{1,2} = R_1 // R_2$

If $V_{OH} \cong V_{CC}$ and $V_{OL} = 0$

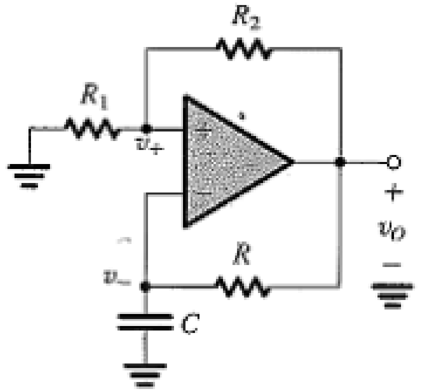
then $R_4 << R_3 + R_{1,2}$

thus, imposing $V_p = V_{TL}$ for $V_o = V_{OL} = 0$

and $v_p = V_{TH}$ for $V_o = V_{OH} = V_{CC}$, we get

$$V_{TL} = \frac{R_{1,3}}{R_{1,3} + R_2} V_{CC} \; ; \; V_{TH} = \frac{R_1}{R_1 + R_{2,3}} V_{CC}$$

Astable Circuit ..



Voltage across capacitor:

$$v_- = L_+ - (L_+ - \beta L_-)e^{-t/\tau}$$

Substituting $v_- = \beta L_+$ at $t = T_1$ gives

$$T_1 = \tau \ln \frac{1 - \beta(L_-/L_+)}{1-\beta}$$

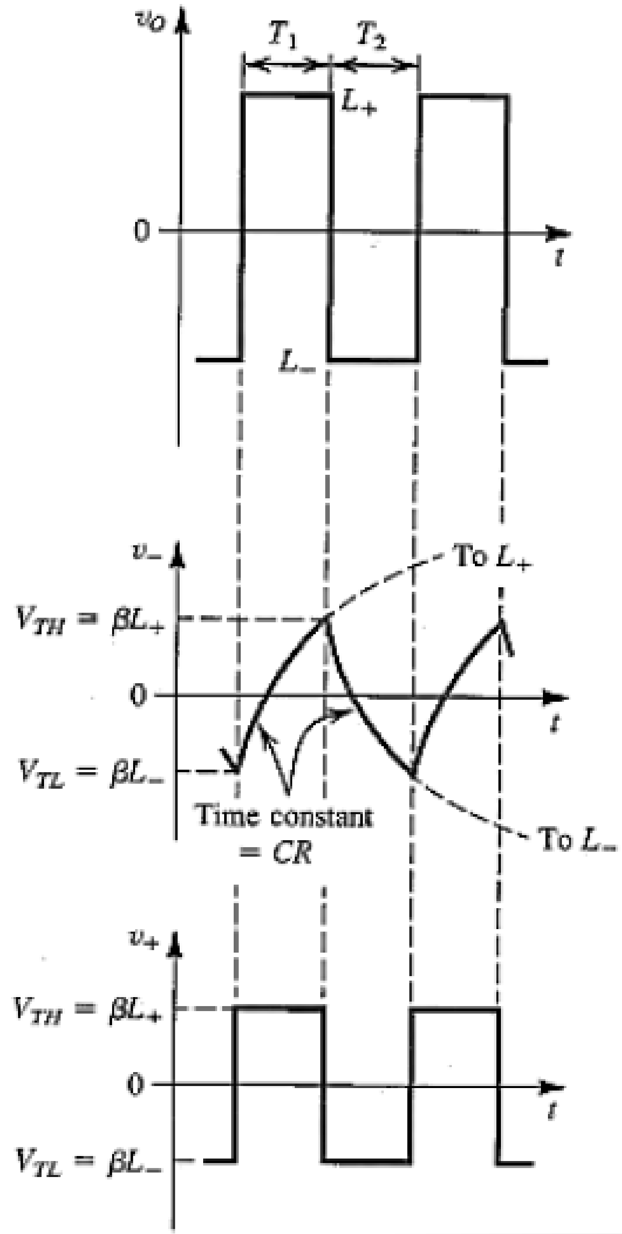
$$v_- = L_- - (L_- - \beta L_+)e^{-t/\tau}$$

$$T_2 = \tau \ln \frac{1 - \beta(L_+/L_-)}{1-\beta}$$

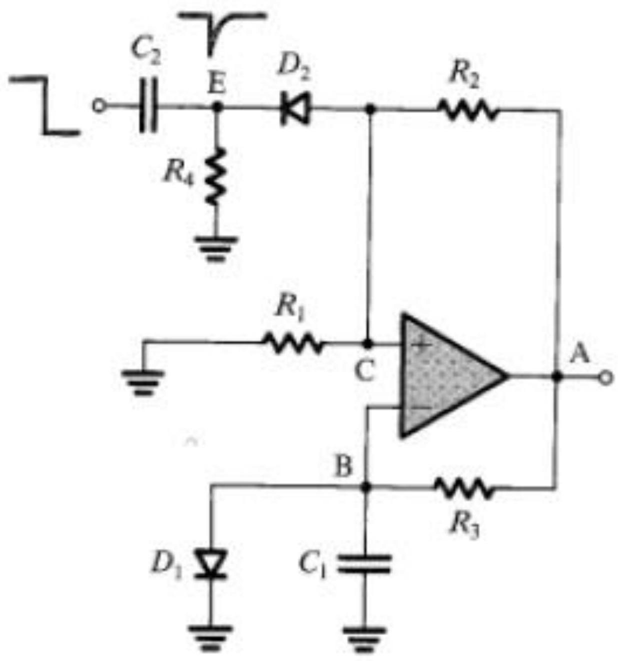
$$T = T_1 + T_2.$$

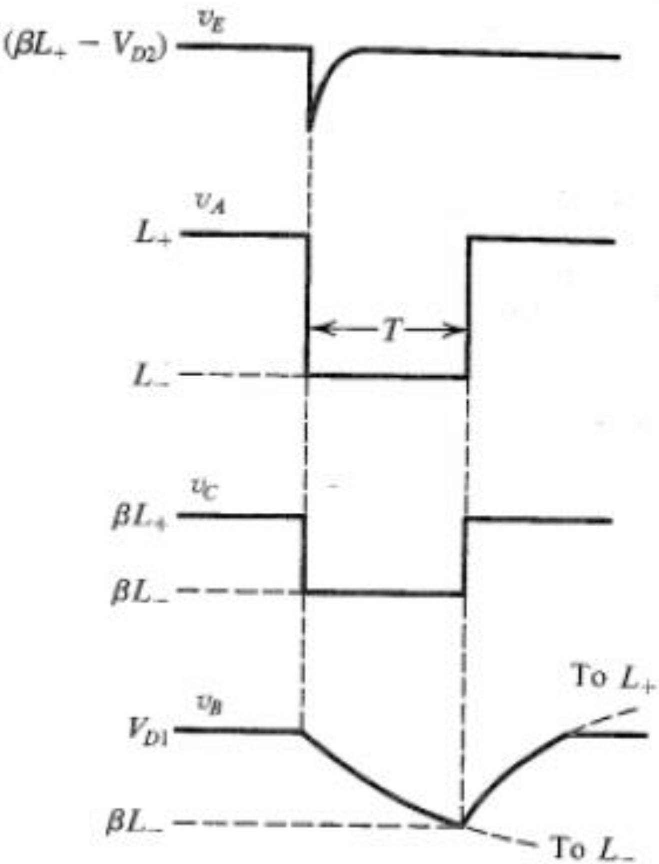
$$\boxed{T = 2\tau \ln \frac{1+\beta}{1-\beta}}$$

$\tau = CR.$



Monostable circuit





$$v_B(t) = L_- - (L_- - V_{D1})e^{-t/C_1R_3}$$

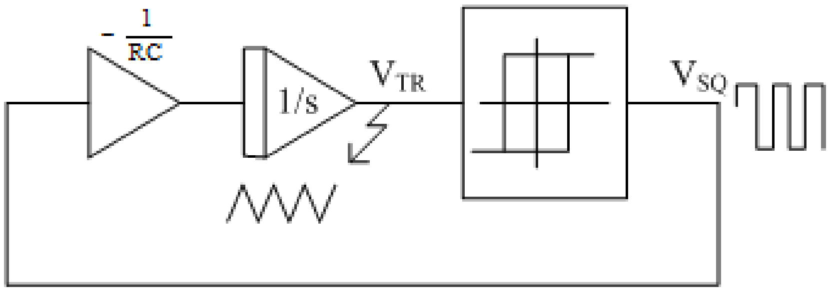
by substituting $v_B(T) = \beta L_-$,

$$\beta L_- = L_- - (L_- - V_{D1})e^{-T/C_1R_3}$$

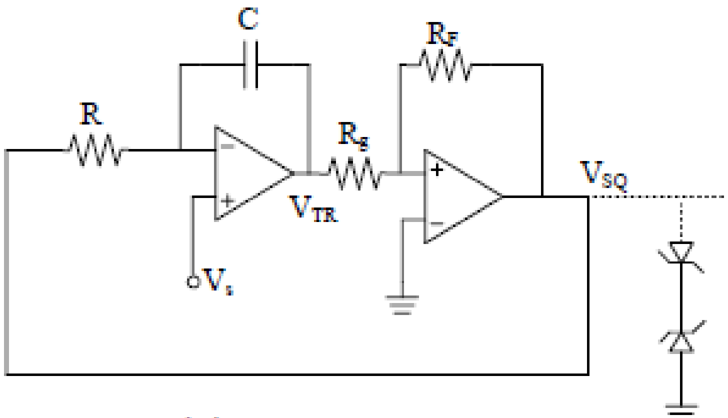
$$T = C_1R_3 \ln\left(\frac{V_{D1} - L_-}{\beta L_- - L_-}\right)$$

$$T \simeq C_1R_3 \ln\left(\frac{1}{1-\beta}\right)$$

Basic Triangular/Square Wave Generator



- Two Quasi-static state.
  - For outputs V_{OH} and V_{OL}
- The Schmitt Trigger Toggles between output states.



Transition occurs

$$V_{TR(trans)} = -\frac{R_g}{R_f} V_{SQ} = \mp \frac{R_g}{R_f} V_{OH}$$

$$V_{TR} = -\frac{1}{RC}\int \left[V_{SQ}(t) - V_s\right] dt$$

When, v_{SQ} is in the high state, V_{TR} is linearly decreasing between its toggle values.

$$v_{TR} = -\frac{1}{RC}\int (V_{OH} - V_s) dt = \frac{V_s - V_{OH}}{RC} t + v_{TR}(0^+)$$

Initial condition

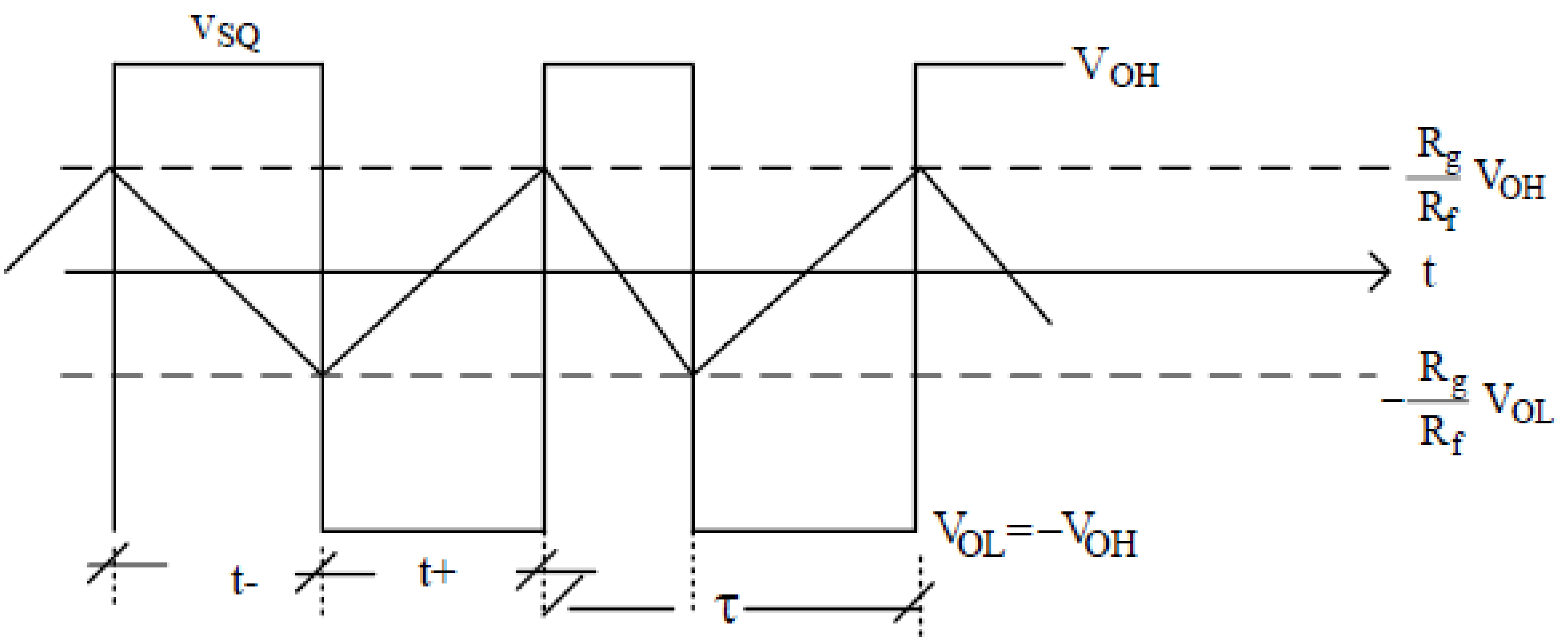
Thus, the voltage transition is the differences in toggle values divided by the slope of the linear transition.

$$2\frac{R_g}{R_f}V_{OH} = \frac{V_{OH} - V_s}{RC}t_-$$

Therefore

$$t_- = \frac{2R_g V_{OH} \cdot RC}{R_f(V_{OH} - V_s)}$$

Now when the positive transition occurs for $V_{s>o}$



$$v_{TR} = -\frac{1}{RC}\int -(V_{OH}+V_s)dt = \frac{V_{OH}+V_s}{RC}t + v_{ti}(o^-)$$

$$2\frac{R_g}{R_f}V_{OH} = \frac{V_{OH}+V_s}{RC}t_+ \Rightarrow t_+ = \frac{2R_gRCV_{OH}}{R_f(V_{OH}+V_s)}$$

Thus the period becomes:

$$T = t\_ + t_+ = 4R_gRC\frac{V_{OH}^2}{R_f(V_{OH}^2 - V_s^2)}\Bigg|\cong \frac{4RC}{R_g/R_f} \text{ for } V_s = 0 \quad \text{or } f_o = \frac{\frac{R_g}{R_f}}{4RC}$$

$$D = \text{Duty cycle} + = \frac{t_+}{T} = \frac{1}{2}\left(1 - \frac{V_s}{V_{OH}}\right)$$

$$\text{for } V_s = 0\text{, } D = 0.5$$

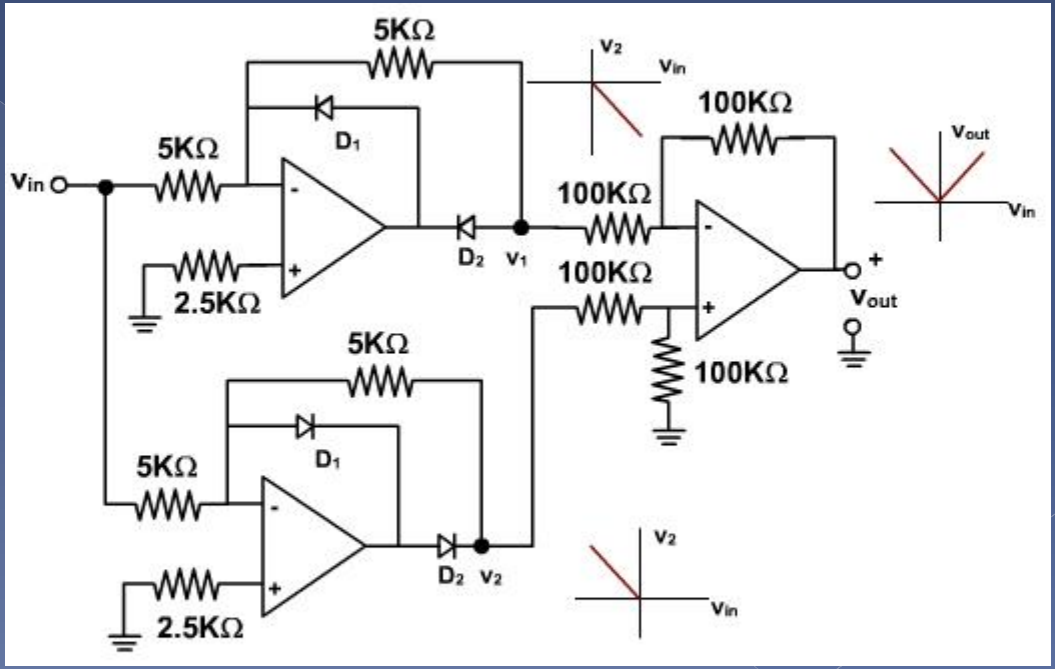
$$\text{for } V_s = \frac{1}{4}V_{OH} \quad , \quad \text{then } D = \frac{1}{2}(1-0.25) = \frac{3}{8}$$

Precision Rectifiers

- Useful when signal to be rectified is very low in amplitude and where good linearity is needed
- Frequency and power handling limitations of op amps limit the use of precision rectifiers to low-power applications (few hundred kHz)
- Precision full-wave rectifier is often referred to as absolute magnitude circuit

Precision Rectifier-Method 1

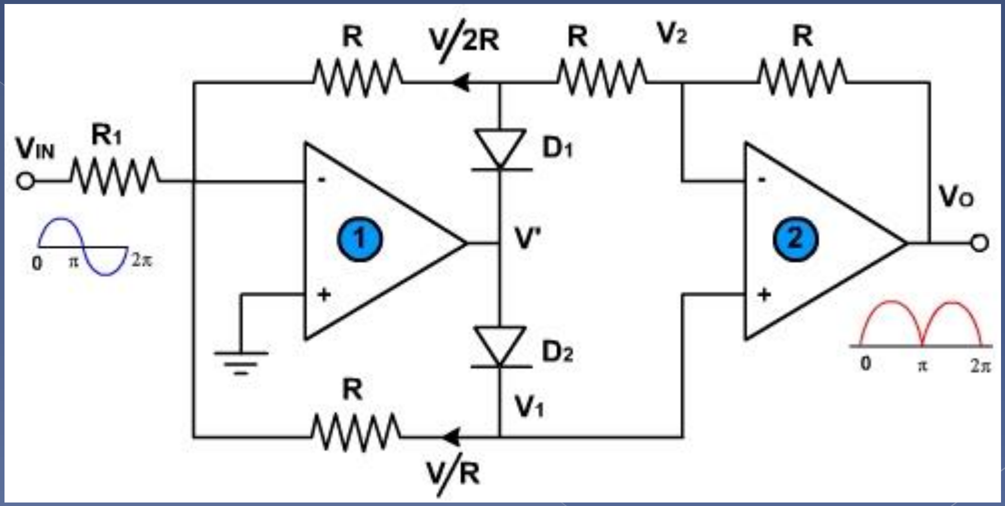
- to use two half wave rectifiers
- resistive network attached to the output summing op-amp is composed of resistors of higher value than those attached to the op-amp that generates v_1.
- Since the input impedance to the non-inverting terminal of the summing op-amp is high, the voltage, v+ is simply one half of v_2
- The voltage at the negative summing terminal, v-, is the same as v+, and therefore is equal to v_2 / 2.
- Now when v_{in} is negative, D_2 is open, and the node v_1 is connected to the inverting input of the first op-amp through a 5 KΩ resistor.
- The inverting input is a virtual ground since the non-inverting input is tied to ground through a resistor.



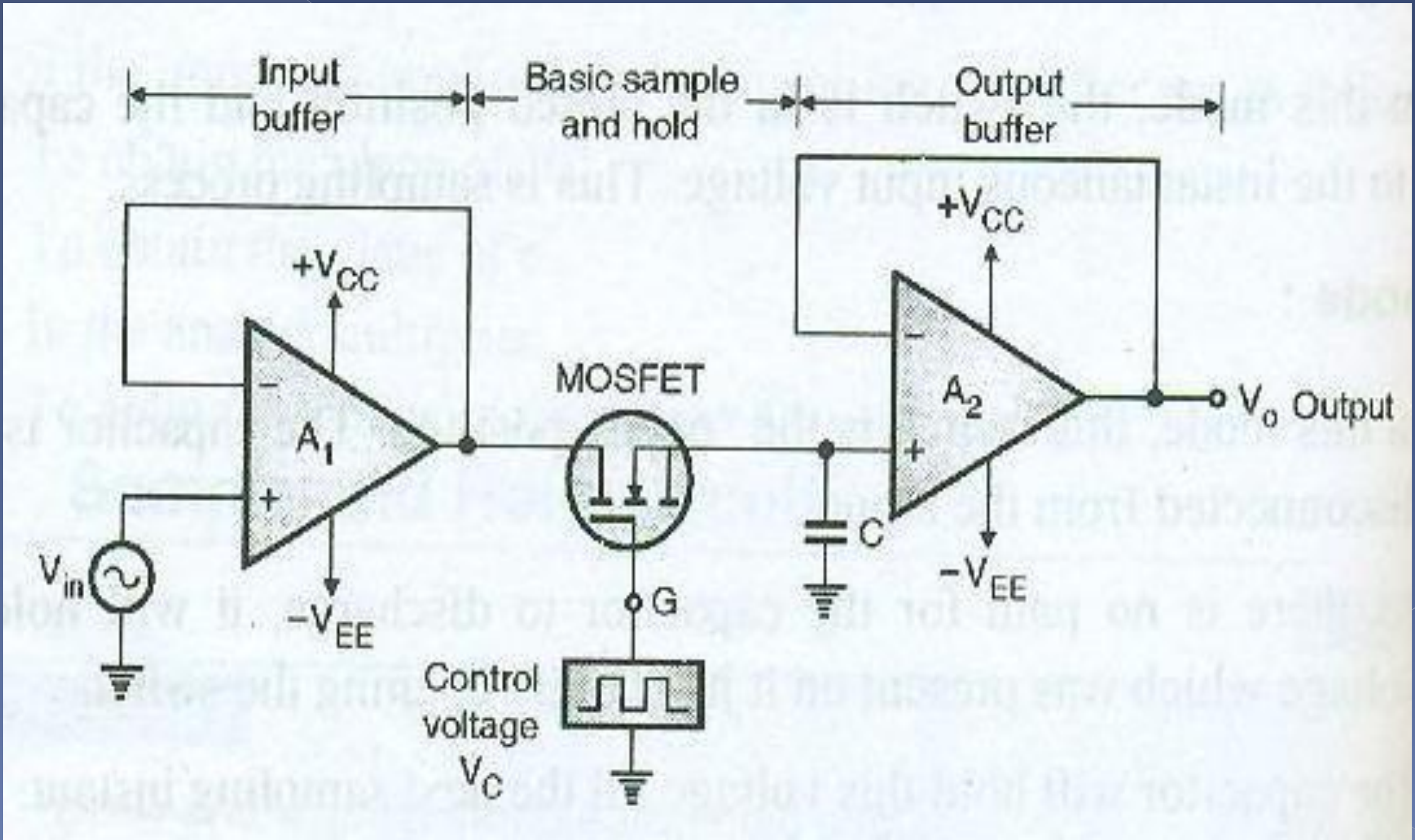
Precision Rectifier-Method 2

- For $v_{in} > 0$
  - $A_1 = -R / R_1$
  - $A_2 = -R / R = -1$
  - $v_o = (R / R_1)\, v_{in}$
- For $v_{in} < 0$
  - $V_2 = V_1 = V$
  - $$\frac{v_{in}}{R_1} + \frac{v}{R} + \frac{v_{in}}{2R} = 0$$
    or $$v = -\frac{2}{3}\frac{R}{R_1} v_{in}$$

$$\therefore v_o = \frac{v}{2R} * R + v = \frac{3}{2} v = -\frac{R}{R_1} v_{in}$$

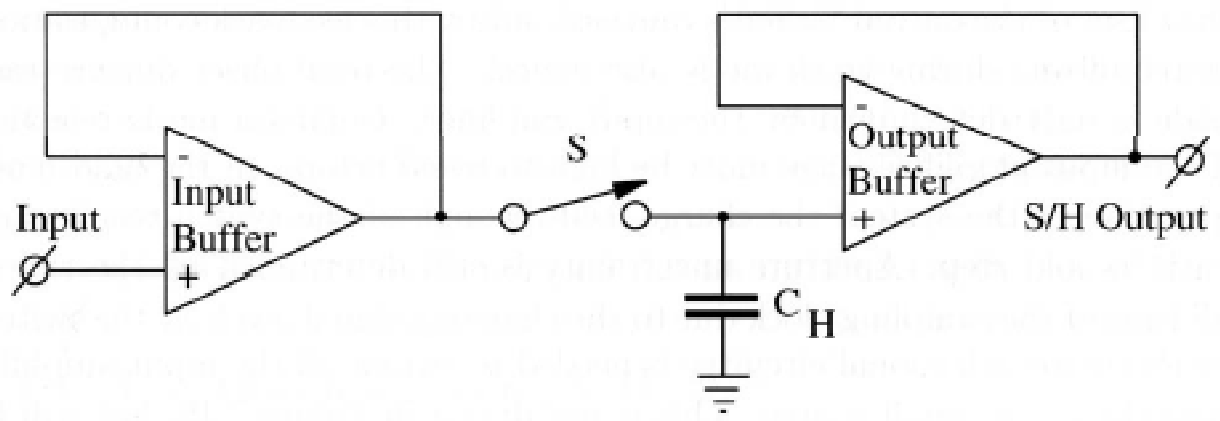


Sample & Hold Circuit



Sample & Hold Circuit…

Double Buffered S&H Configuration



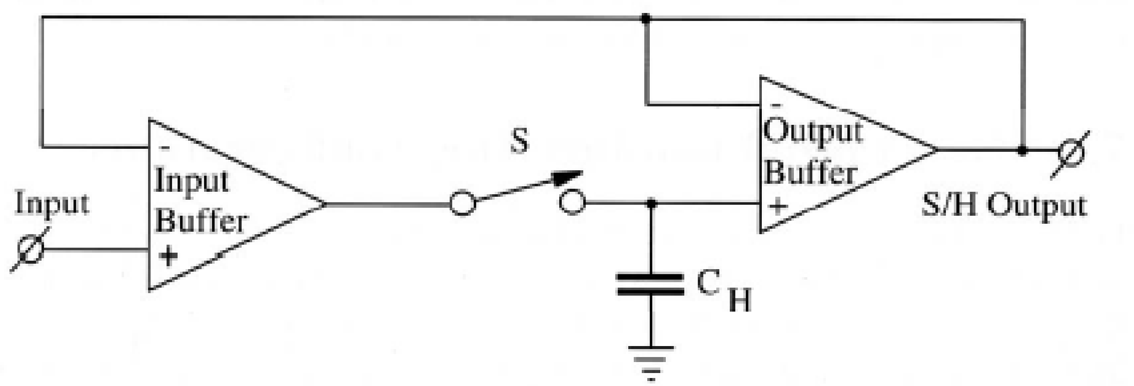
Advantages:

- Obtain a low droop rate during holding mode
- Stability is determined by the stabilities of OP Amps

Disadvantages:

- OP Amps offset can constrain the accuracy of SHA

Feedback Improved S&H Circuit



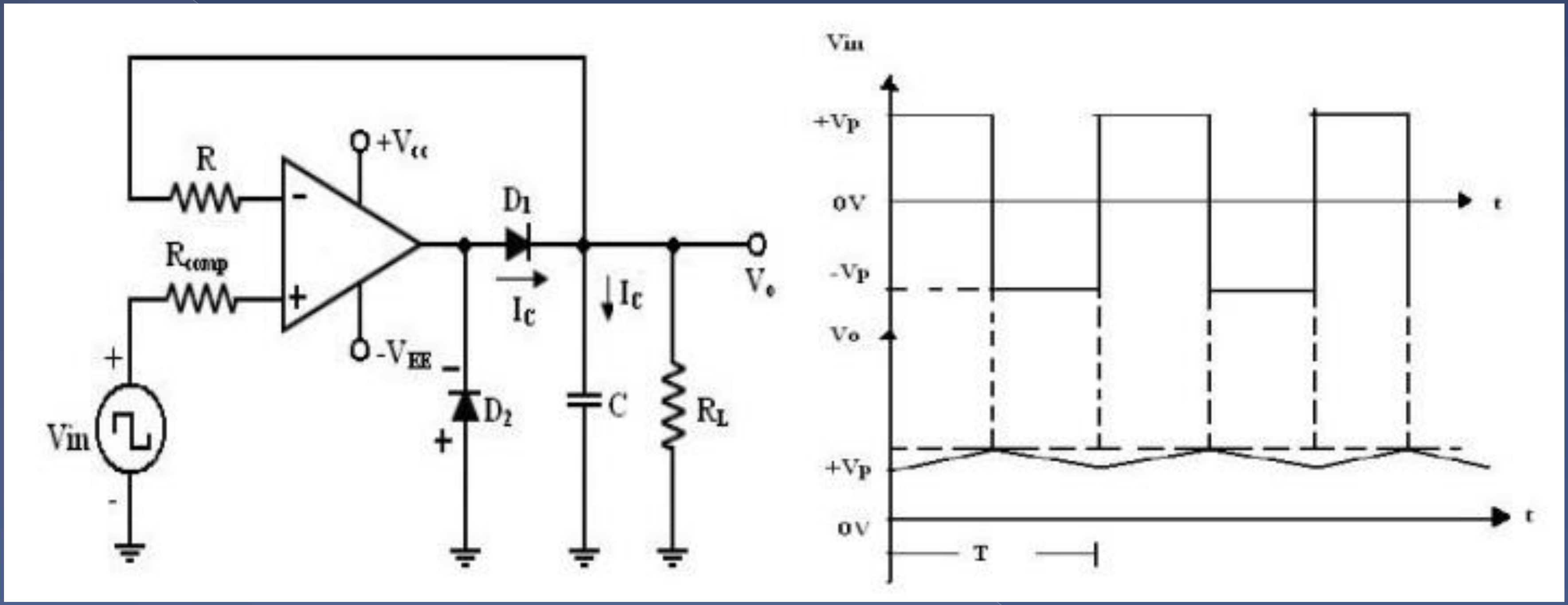
Advantages:

- Offset free → More accurate than double buffered SHA

Disadvantages:

- Common Mode Rejection of the Input OP amp must be high
- Special Care must be taken to obtain stability of SHA
- Needs a special circuitry to stabilize the input amplifier during the holding mode

ACTIVE PEAK DETECTOR



- **During the positive half cycle of Vin**:
  - the o/p of the op-amp drives D1 on. (Forward biased)
  - Charging capacitor C to the positive peak value Vp of the input volt Vin.
- **During the negative half cycle of Vin:**
  - D1 is reverse biased and voltage across C is retained.
  - The only discharge path for C is through RL since the input bias IB is negligible.