VLSI Design (BEC-41)
(Unit-2, Lecture-5)

Presented By:

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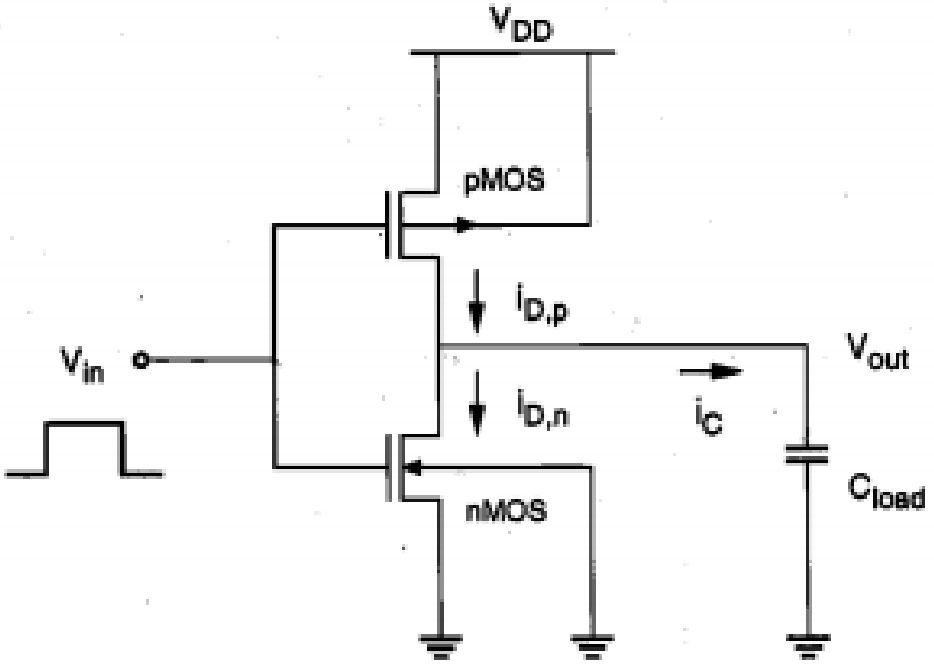
Switching Characteristics of CMOS Inverter



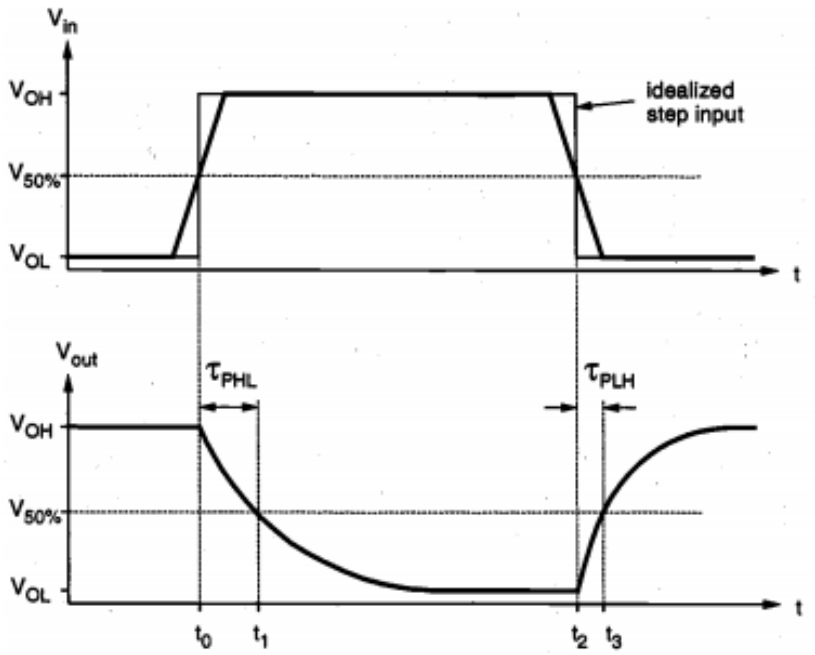


Fig. Input and output voltage waveforms of a typical inverter, and the definitions of propagation delay times.

- The propagation delay times τ_{PHL} and τ_{PLH} are found from Figure as

$$\tau_{PHL} = t_1 - t_0 \text{ and } \tau_{PLH} = t_3 - t_2$$

Switching Characteristics of CMOS Inverter

- The propagation delay times τ_{PHL} and τ_{PLH} determine the input-to-output signal delay during the high-to-low and low-to-high transitions of the output, respectively.
- By definition, τ_{PHL} is the time delay between the $V_{50\%}$-transition of the rising input voltage and the $V_{50\%}$ -transition of the falling output voltage.
- Similarly, τ_{PLH} is defined as the time delay between the $V_{50\%}$ -transition of the falling input voltage and the $V_{50\%}$ -transition of the rising output voltage.

Calculation of Delay Times

- The propagation delay times can be found more accurately by solving the state equation of the output node in the time domain. The differential equation associated with the output node is given below. Note that the capacitance current is also a function of the output voltage.

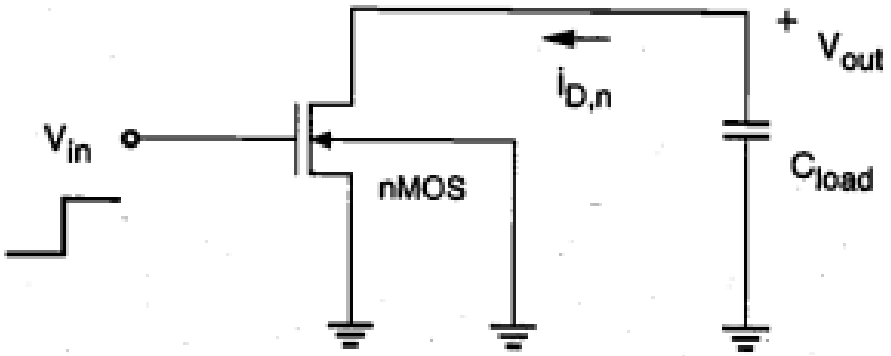


Fig. Equivalent circuit of the CMOS inverter during high-to-low output transition.

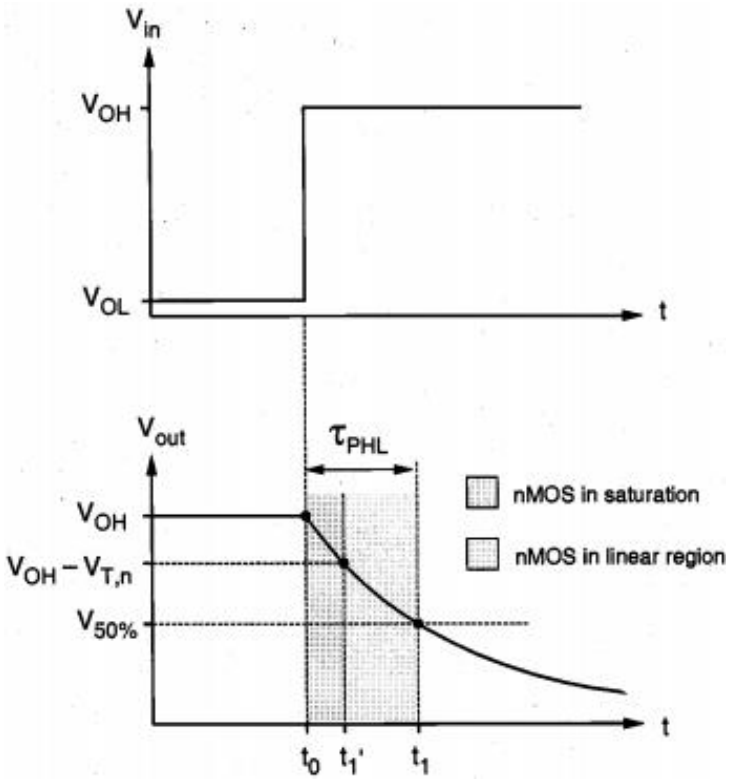


Fig. Input and output voltage waveforms during high-to-low transition.

Calculation of Delay Times

- First, consider the NMOS transistor operating in saturation.

$$i_{D,n} = \frac{k_n}{2}\left(V_{in} - V_{T,n}\right)^2$$

$$= \frac{k_n}{2}\left(V_{OH} - V_{T,n}\right)^2, \qquad for \quad V_{OH} - V_{T,n} < V_{out} \le V_{OH}$$

- the solution equation in the time interval between t_o and t_1' , can be found as

$$\int_{t=t_0}^{t=t_1'} dt = -C_{load} \int_{V_{out}=V_{OH}}^{V_{out}=V_{OH}-V_{T,n}} \left(\frac{1}{i_{D,n}}\right) dV_{out} = -\frac{2C_{load}}{k_n\left(V_{OH} - V_{T,n}\right)^2} \int_{V_{out}=V_{OH}}^{V_{out}=V_{OH}-V_{T,n}} dV_{out}$$

- Evaluating this simple integral yields

$$t_1' - t_0 = \frac{2C_{load}\,V_{T,n}}{k_n\left(V_{OH} - V_{T,n}\right)^2}$$

Calculation of Delay Times

- At t = t_1', the output voltage will be equal to ($V_{DD} – V_{T,n}$) and the transistor will be at the saturation-linear region boundary.
- Next, consider the NMOS transistor operating in the linear region:

$$i_{D,n} = \frac{k_n}{2}\left[2\left(V_{in} - V_{T,n}\right)V_{out} - {V_{out}}^2\right]$$

$$= \frac{k_n}{2}\left[2\left(V_{OH} - V_{T,n}\right)V_{out} - {V_{out}}^2\right], \quad for \quad V_{out} \le V_{OH} - V_{T,n}$$

- The solution of equation in the time interval between t_1' and t_1 can be found as

$$\int_{t=t_1'}^{t=t_1} dt = -C_{load} \int_{V_{out}=V_{OH}-V_{T,n}}^{V_{out}=V_{50\%}} \left(\frac{1}{i_{D,n}}\right) dV_{out}$$

$$= -2\,C_{load} \int_{V_{out}=V_{OH}-V_{T,n}}^{V_{out}=V_{50\%}} \left(\frac{1}{k_n\left[2\left(V_{OH} - V_{T,n}\right)V_{out} - V_{out}^2\right]}\right) dV_{out}$$

Calculation of Delay Times

$$t_1 - t_1' = \frac{C_{load}}{k_n\left(V_{OH} - V_{T,n}\right)} \ln\left(\frac{2\left(V_{OH} - V_{T,n}\right) - V_{50\%}}{V_{50\%}}\right)$$

- Finally, the propagation delay time for high-to-low output transition (T_{PHL}) can be found by combining both timing equations:

$$\tau_{PHL} = \frac{C_{load}}{k_n\left(V_{OH} - V_{T,n}\right)}\left[\frac{2V_{T,n}}{V_{OH} - V_{T,n}} + \ln\left(\frac{4\left(V_{OH} - V_{T,n}\right)}{V_{OH} + V_{OL}} - 1\right)\right]$$

- For $V_{OH} = V_{DD}$ and $V_{OL} = 0$, as is the case for the CMOS inverter, becomes:

$$\tau_{PHL} = \frac{C_{load}}{k_n\left(V_{DD} - V_{T,n}\right)}\left[\frac{2V_{T,n}}{V_{DD} - V_{T,n}} + \ln\left(\frac{4\left(V_{DD} - V_{T,n}\right)}{V_{DD}} - 1\right)\right]$$

Calculation of Delay Times (Continued..)

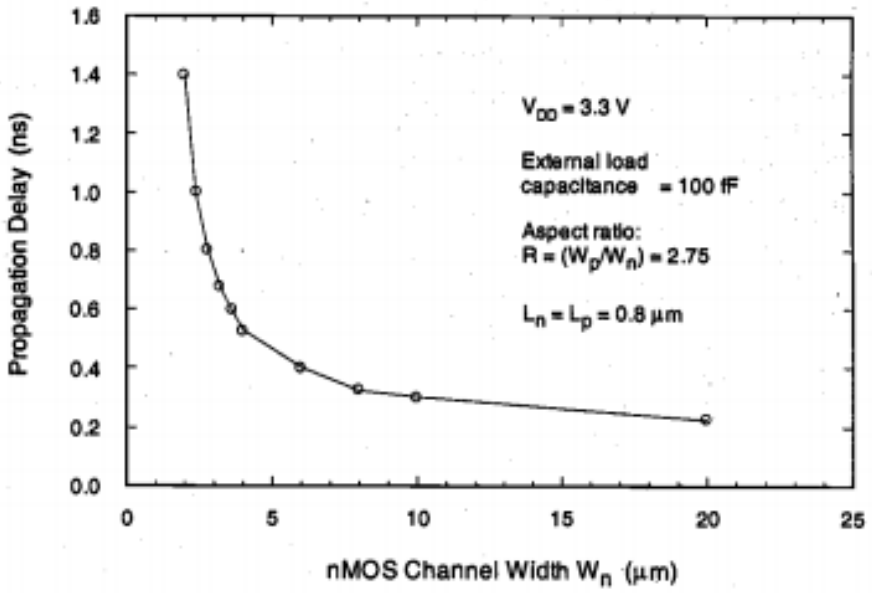
- In a CMOS inverter, the charge-up event of the output load capacitance for falling input transition is completely analogous to the charge-down event for rising input.
- When the input voltage switches from high (V_{OH}) to low (V_{OL}), the NMOS transistor is cut off, and the load capacitance is being charged up through the PMOS transistor.
- Following a very similar derivation procedure, the propagation delay time τ_{PLH} can be found as:

$$\tau_{PLH} = \frac{C_{load}}{k_p\left(V_{OH} - V_{OL} - |V_{T,p}|\right)}\left[\frac{2|V_{T,p}|}{V_{OH} - V_{OL} - |V_{T,p}|} + \ln\left(\frac{2\left(V_{OH} - V_{OL} - |V_{T,p}|\right)}{V_{OH} - V_{50\%}} - 1\right)\right]$$

- For $V_{OH} = V_{DD}$ and $V_{OL} = 0$, equation becomes

$$\tau_{PLH} = \frac{C_{load}}{k_p\left(V_{DD} - |V_{T,p}|\right)}\left[\frac{2|V_{T,p}|}{V_{DD} - |V_{T,p}|} + \ln\left(\frac{4\left(V_{DD} - |V_{T,p}|\right)}{V_{DD}} - 1\right)\right]$$

Calculation of Delay Times (Continued..)



- In fact, the increase in silicon area can be viewed as a design trade-off for delay reduction, since the circuit speed improvements are typically obtained at the expense of increased transistor dimensions.

- In the following figure, the falling-output propagation delay τ_{PHL} (obtained from SPICE simulation) is plotted as a function of the NMOS channel width.