Branch Operations

Allow the microprocessor to change the sequence of a program either unconditionally, or under certain test condition.

- Jump instructions
- Call and return instructions
- Restart instructions

JMP 16 bit address: The program sequence is transferred to memory location specified by the 16-bit address.

Memory Address	Code/data	Mnemonics
2000	C3	JMP 2500H
2001	00	
2002	25	

Opcode	Operand	Byte	M- Cycle	T-State
JMP	16 bit	3	3	10

No flags are affected

Jump Conditionally

.

Opcode	Description	Flag Status	Byte	M- Cycle	T-State
JC	Jump on Carry	CY=1	3	3/2*	10/7*
JNC	Jump on No Carry	CY=0	3	3/2*	10/7*
JP	Jump on positive	S=0	3	3/2*	10/7*
JM	Jump on minus	S=1	3	3/2*	10/7*
JZ	Jump on Zero	Z=1	3	3/2*	10/7*
JNZ	Jump on No Zero	Z=0	3	3/2*	10/7*
JPE	Jump on Parity Even	P=1	3	3/2*	10/7*
JPO	Jump on Parity Odd	P=0	3	3/2*	10/7*

***If condition is true, then 3M/10T**
***If condition is not true, then 2M/7T**
No flags are affected

CALL 16 bit address: The program sequence is transferred to address specified by operand (16-bit address).

Before the transfer, the address of next instruction to CALL (content of the PC) is pushed on the stack.

MSB of PC is stored at location specified by SP-1.

LSB of PC is stored at location specified by SP-2.

Call address is temporarily stored in internal WZ register (lower byte in Z register and higher byte in W register and placed on the bus for the fetch cycle of first instruction of subroutine.

Last instruction of subroutine: RET(unconditional return)

Opcode	Operand	Byte	M-cycle	T-State
CALL	16 bit address	3	5	18*

Opcode fetch cycle requires 6T

No flags are affected

Conditional Call

Opcode	Description	Flag Status	Byte	M- Cycle	T-State
CC	Call on Carry	CY=1	3	5/2*	18/9*
CNC	Call on No Carry	CY=0	3	5/2*	18/9*
CP	Call on positive	S=0	3	5/2*	18/9*
CM	Call on minus	S=1	3	5/2*	18/9*
CZ	Call on Zero	Z=1	3	5/2*	18/9*
CNZ	Call on No Zero	Z=0	3	5/2*	18/9*
CPE	Call on Parity Even	P=1	3	5/2*	18/9*
CPO	Call on Parity Odd	P=0	3	5/2*	18/9*

***If condition is true, then 5M/18T**
***If condition is not true, then 2M/9T**
Last instruction of subroutine: Conditional return
No flags are affected

RET: Return from subroutine unconditionally.

The program sequence is transferred from the subroutine to the main (calling) program.

Two bytes from the top of the stack are copied into PC and the program execution begins at the new address.

After execution of RET instruction SP is incremented by 2.

Opcode	Operand	Byte	M-cycle	T-State
RET	None	1	3	10

.

No flags are affected

Conditional Return

Opcode	Description	Flag Status	Byte	M- Cycle	T-State
RC	Return on Carry	CY=1	1	1/3*	6/12*
RNC	Return on No Carry	CY=0	1	1/3*	6/12*
RP	Return on positive	S=0	1	1/3*	6/12*
RM	Return on minus	S=1	1	1/3*	6/12*
RZ	Return on Zero	Z=1	1	1/3*	6/12*
RNZ	Return on No Zero	Z=0	1	1/3*	6/12*
RPE	Return on Parity Even	P=1	1	1/3*	6/12*
RPO	Return on Parity Odd	P=0	1	1/3*	6/12*

***If condition is true, then 3M/12T**
***If condition is not true, then 1M/6T**
No flags are affected

RST n: This is a single byte unconditional subroutine call instruction.

The address of the subroutine is fixed depending upon the decimal number “n” in the instruction.

Opcode/Operand	Byte	M- Cycle	T-State	Restart Address
RST 0	1	3	12	0000 H
RST 1	1	3	12	0008 H
RST 2	1	3	12	0010 H
RST 3	1	3	12	0018 H
RST 4	1	3	12	0020 H
RST 5	1	3	12	0028 H
RST 6	1	3	12	0030 H
RST 7	1	3	12	0038 H

No flags are affected

PCHL: Load PC with HL Contents

Move the content of register (H) to the higher byte of program counter (PCH) and move the content of register (L) to lower byte of program counter (PCL)

Control is transferred to the memory location whose address is available in (H, L) register pair.

Equivalent to 1-byte unconditional jump instruction (register indirect jump instruction).

Opcode	Operand	Byte	M-cycle	T-State
PCHL	None	1	1	6

.

No flags are affected

Stack and Machine Control Instructions

PUSH Rp/PSW: Push register pair/PSW onto stack

Contents of register pair/program status word (Accumulator and flag) are copied into stack.

SP is decremented by 1 and Contents of higher-order register (B,D,H,A) are copied into that location.

SP is again decremented by 1 and Contents of lower-order register (C,E,L,Flags) are copied into that location.

Opcode	Operand	Byte	M-cycle	T-State
PUSH	Rp/PSW	1	3	12

No flags are affected

POP Rp/PSW: Pop off stack to register pair /PSW

Contents of memory location pointed out by SP are copied to lower- order register (C,E,L,Flags).

SP is incremented by 1 and contents of memory location pointed out by SP are copied to higher-order register (B,D,H,A).

SP is again incremented by 1.

.

Opcode	Operand	Byte	M-cycle	T-State
POP	Rp/PSW	1	3	10

No flags are affected

HLT: Halt and enter to wait state

MPU finishes executing the current instruction and halts any further execution.

MPU enters halt acknowledge machine cycle and wait states are inserted in every clock period.

Address and data bus are placed in high impedance state.

Any interrupt/reset is required to exit from Halt state.

Opcode	Operand	Byte	M-cycle	T-State
HLT	None	1	2 or more	5 or more

NOP: No operation(Instruction is fetched and decoded; however, no operation is executed.)

Useful to fill time delays or to delete and insert instructions while troubleshooting.

Opcode	Operand	Byte	M-cycle	T-State
NOP	None	1	1	4

No flags are affected