VLSI Design (BEC-41)
(Unit-1, Lecture-5)

Presented By:

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MOSFET capacitances

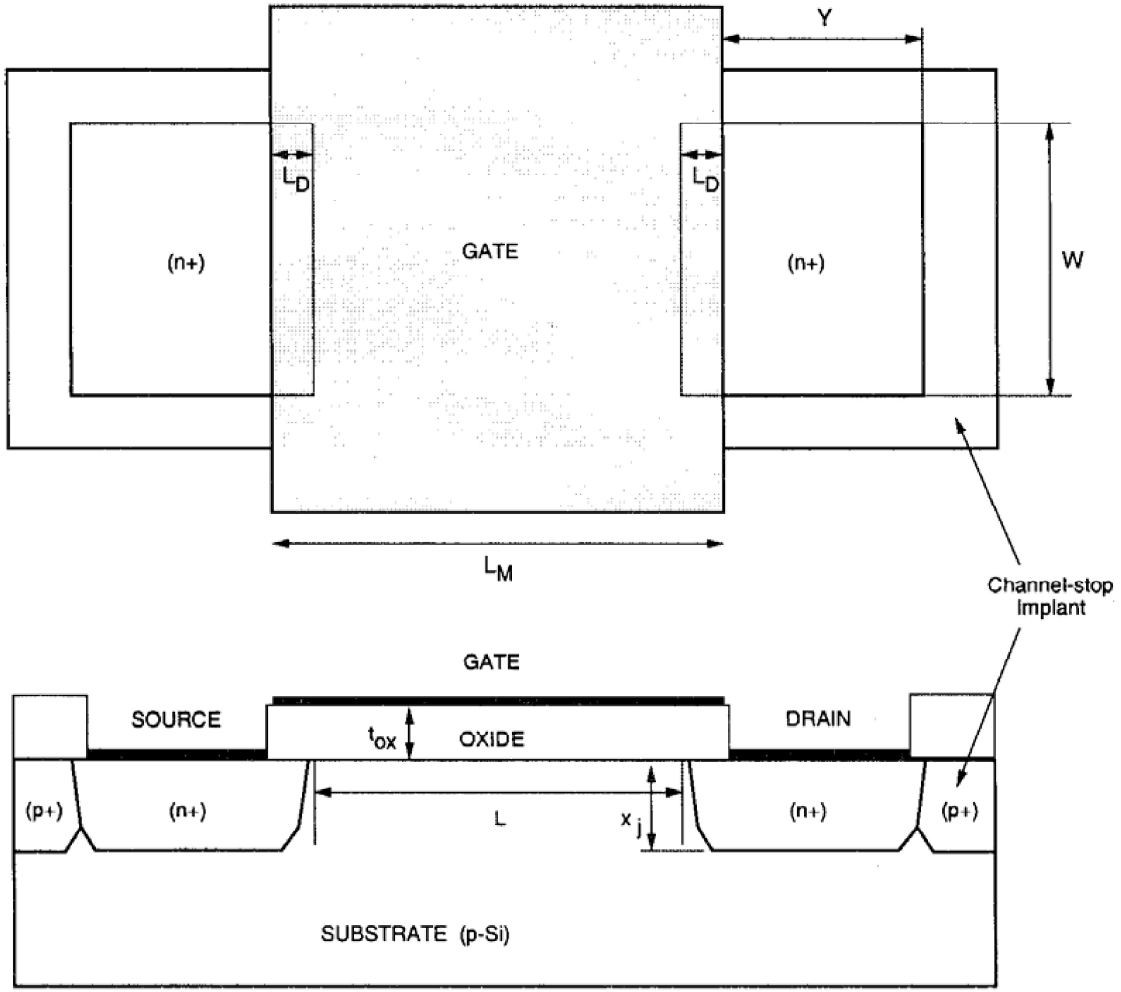


Figure 3.29 Cross-sectional view and the top view (mask view) of a typical n-channel MOSFET.

- $L=L_M-2L_D$
  - L: the actual channel length
  - L_M: the mask length of the gate
  - L_D: the gate-drain, the gate-source overlap
    - On the order of 0.1μm

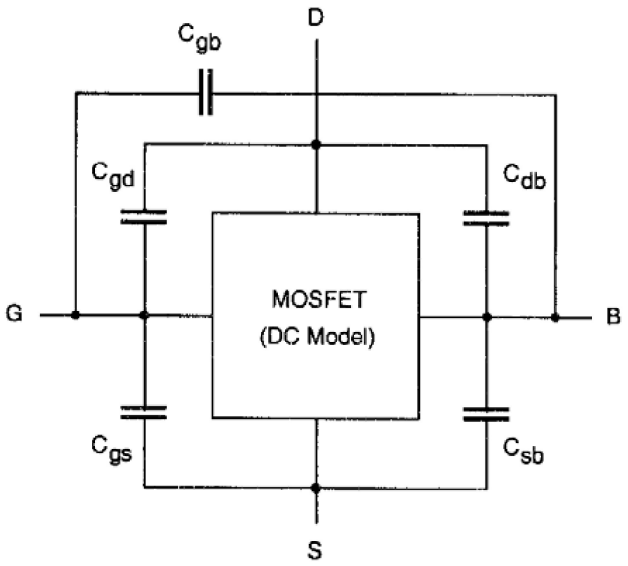


Figure 3.30 Lumped representation of the parasitic MOSFET capacitances.

Oxide related capacitance(1)

- The gate electrode overlap capacitance
  - $C_{GD(overlap)}=C_{ox}WL_D$
  - $C_{GS(overlap)}=C_{ox}WL_D$
    - *With* $C_{ox}=\varepsilon_{ox}/t_{ox}$
  - Both capacitance do not depend on the bias condition, they are voltage-independent
- The capacitances result from the interaction between the gate voltage and the channel charge
  - Cut-off mode
    - $C_{gs}=C_{gd}=0$
    - $C_{gb}=C_{ox}WL$
  - Linear mode
    - $C_{gb}=0$
    - $C_{gs}\cong C_{gd}\cong(1/2)\ C_{ox}WL$
  - Saturation mode
    - $C_{gb}= C_{gd} =0$
    - $C_{gs}\cong (2/3)\ C_{ox}WL$

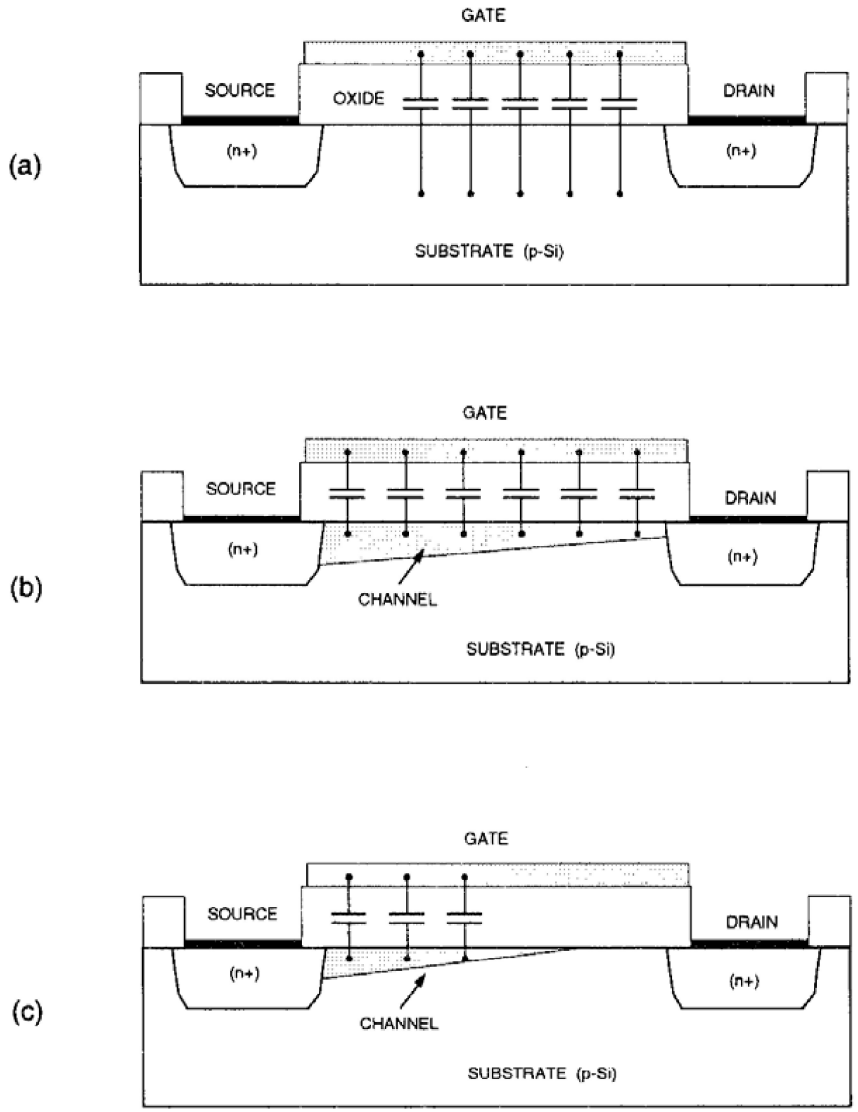


Figure 3.31 Schematic representation of MOSFET oxide capacitances during (a) cut-off, (b) linear, and (c) saturation modes.

Oxide related capacitance(2)

- The sum of all three voltage-dependent (distributed) gate oxide capacitances ($C_{gb}+C_{gs}+C_{gd}$)
  - A minimum value of $0.66C_{ox}WL$, in saturation mode
  - A maximum value of $C_{ox}WL$, in cut off and linear modes
  - For simple hand calculation
    - The three capacitances can be considered to be in parallel
    - A constant worst-case value of $C_{ox}W(L+2L_D)$ can be used for the sum of MOSFET gate oxide capacitances

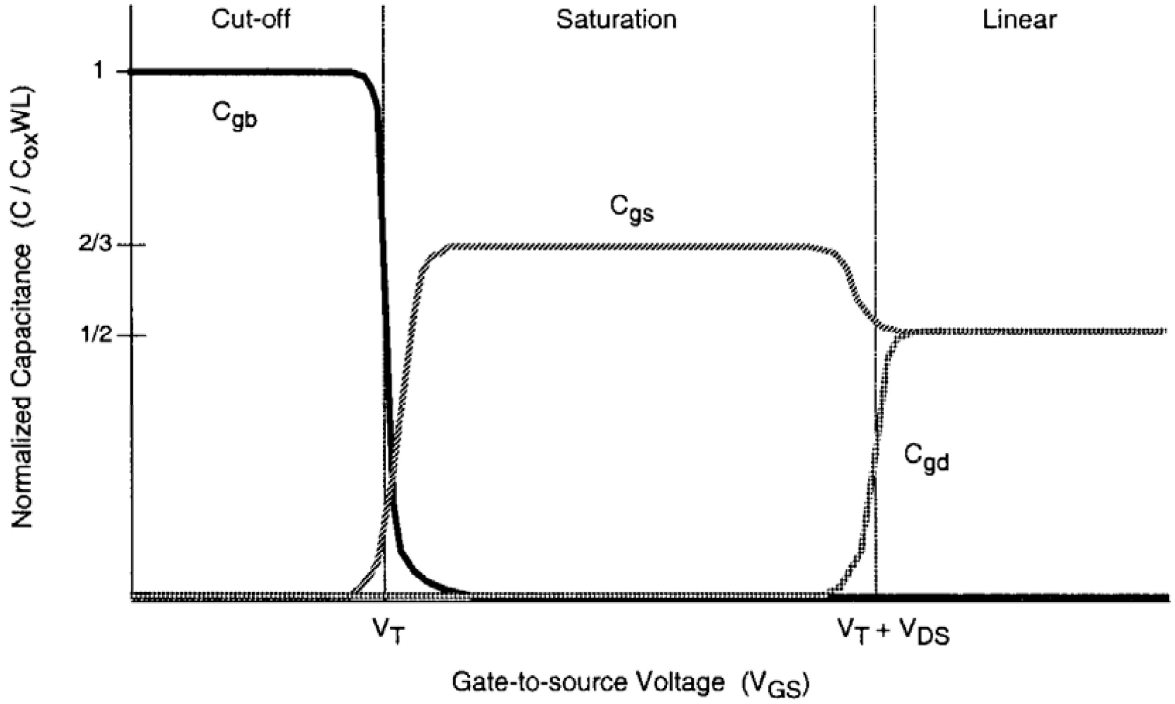


Figure 3.32 Variation of the distributed (gate-to-channel) oxide capacitar functions of gate-to-source voltage V_{GS}.

Junction capacitance(1)

The depletion region thickness $x_d = \sqrt{\frac{2\cdot\varepsilon_{Si}}{q}\cdot\frac{N_A+N_D}{N_A\cdot N_D}(\varphi_0 - V)}$

The built - in potential $\varphi_0 = \frac{kT}{q}\cdot\ln\left(\frac{N_A\cdot N_D}{n_i^2}\right)$

The depletion region charge $Q_j = A\cdot q\cdot\left(\frac{N_A\cdot N_D}{N_A+N_D}\right)\cdot x_d = A\sqrt{2\cdot\varepsilon_{Si}\cdot q\cdot\frac{N_A\cdot N_D}{N_A+N_D}(\varphi_0 - V)}$

The junction capacitance $C_j = \left|\frac{dQ_j}{dV}\right| = A\cdot\sqrt{\frac{\varepsilon_{Si}\cdot q}{2}\cdot\left(\frac{N_A\cdot N_D}{N_A+N_D}\right)}\cdot\frac{1}{\sqrt{\varphi_0 - V}}$

$C_j(V) = \frac{AC_{j0}}{\left(1-\frac{V}{\varphi_0}\right)^m}$, the parameter m is grading coefficient

The zero bias junction capacitance per unit area $C_{j0} = \sqrt{\frac{\varepsilon_{Si}\cdot q}{2}\cdot\left(\frac{N_A\cdot N_D}{N_A+N_D}\right)\cdot\frac{1}{\varphi_0}}$

The equivalent large - signal capacitance can be defined as

$$C_{eq} = \frac{\Delta Q}{\Delta V} = \frac{Q_j(V_2) - Q_j(V_1)}{V_2 - V_1} = \frac{1}{V_2 - V_1}\int_{V_1}^{V_2} C_j(V)dV$$

$$= -\frac{A\cdot C_{j0}\cdot\phi_0}{(V_2 - V)\cdot(1-m)}\cdot\left[\left(1-\frac{V_2}{\phi_0}\right)^{1-m} - \left(1-\frac{V_1}{\phi_0}\right)^{1-m}\right]$$

For the special case of abrupt pn - junctions

$$C_{eq} = -\frac{2\cdot A\cdot C_{j0}\cdot\varphi_0}{(V_2 - V)}\cdot\left[\sqrt{1-\frac{V_2}{\phi_0}} - \sqrt{1-\frac{V_1}{\phi_0}}\right]$$

$$C_{eq} = A\cdot C_{j0}\cdot K_{eq}$$

$$K_{eq} = -\frac{2\sqrt{\phi_0}}{V_2 - V_1}\cdot\left(\sqrt{\phi_0 - V_2} - \sqrt{\phi_0 - V_1}\right)$$

Table 3.7 Types and areas of the pn-junctions shown in Fig. 3.33

Junction	Area	Type
1	$W\cdot x_j$	n^+/p
2	$Y\cdot x_j$	n^+/p^+
3	$W\cdot x_j$	n^+/p^+
4	$Y\cdot x_j$	n^+/p^+
5	$W\cdot Y$	n^+/p

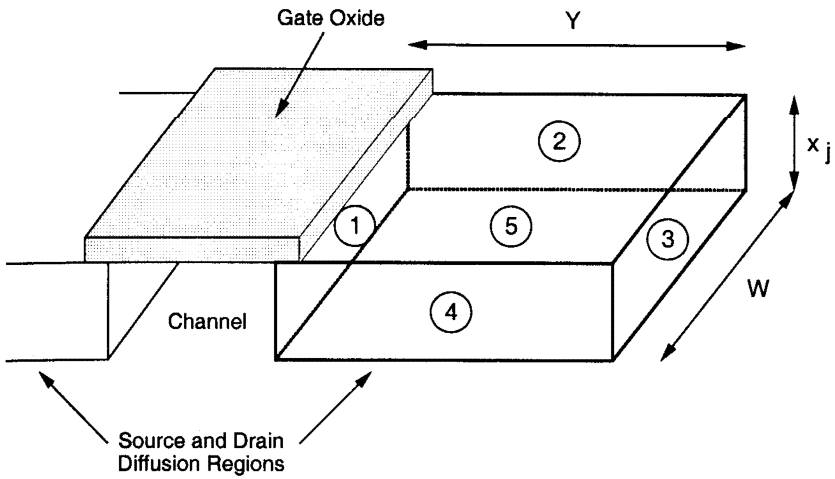
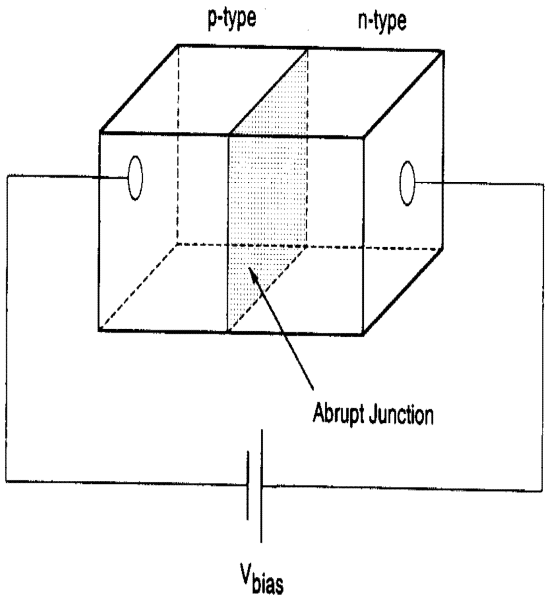


Figure 3.33 Three-dimensional view of the n^+ diffusion region within the p-type substrate.

Example 7

Consider a simple abrupt pn-junction, which is reverse-biased with a voltage V_{bias}. The doping density of the n-type region is $N_D = 10^{19}$ cm^{-3}, and the doping density of the p-type region is given as $N_A = 10^{16}$ cm^{-3}. The junction area is $A = 20\,\mu$m x $20\,\mu$m.



First, we will calculate the zero-bias junction capacitance per unit area, C_{j0}, for this structure. The built-in junction potential is found as

$$\phi_0 = \frac{kT}{q} \cdot \ln\left(\frac{N_A \cdot N_D}{n_i^2}\right) = 0.026\ \text{V} \cdot \ln\left(\frac{10^{16} \cdot 10^{19}}{2.1 \times 10^{20}}\right) = 0.88\ \text{V}$$

Using (3.105), we can calculate the zero-bias junction capacitance:

$$C_{j0} = \sqrt{\frac{\varepsilon_{Si} \cdot q}{2} \cdot \left(\frac{N_A \cdot N_D}{N_A + N_D}\right) \cdot \frac{1}{\phi_0}}$$

$$= \sqrt{\frac{11.7 \cdot 8.85 \times 10^{-14}\ \text{F/cm} \cdot 1.6 \times 10^{-19}\ \text{C}}{2} \cdot \left(\frac{10^{16} \cdot 10^{19}}{10^{16} + 10^{19}}\right) \cdot \frac{1}{0.88\ \text{V}}}$$

$$= 3.1 \times 10^{-8}\ \text{F/cm}^2$$

Next, find the equivalent large-signal junction capacitance assuming that the reverse bias voltage changes from $V_1 = 0$ to $V_2 = -5$ V. The voltage equivalence factor for this transition can be found as follows:

$$K_{eq} = -\frac{2\sqrt{\phi_0}}{V_2 - V_1} \cdot \left(\sqrt{\phi_0 - V_2} - \sqrt{\phi_0 - V_1}\right)$$

$$= -\frac{2\sqrt{0.88}}{-5} \cdot \left(\sqrt{0.88 - (-5)} - \sqrt{0.88}\right) = 0.56$$

Then, the average junction capacitance can be found simply by using (3.109).

$$C_{eq} = A \cdot C_{j0} \cdot K_{eq} = 400 \times 10^{-8}\ \text{cm}^2 \cdot 3.1 \times 10^{-8}\ \text{F/cm}^2 \cdot 0.56 = 69\ \text{fF}$$

Junction capacitance(2)

The sidewalls of a typical MOSFET source or drain diffusion region are surrounded by a p^+ channel-stop implant, with a higher doping density than the substrate doping density N_A

Assume the sidewall doping density is given by $N_{A(sw)}$,

the zero-bias capacitance per unit area can be found as

$$C_{j0sw} = \sqrt{\frac{\varepsilon_{Si} \cdot q}{2} \cdot \left(\frac{N_{A(sw)} \cdot N_D}{N_{A(sw)} + N_D} \right) \cdot \frac{1}{\varphi_{0sw}}}$$

$$C_{jsw} = C_{j0sw} \cdot x_j$$

The sidewall voltage equivalence factor

$$K_{eq(sw)} = -\frac{2\sqrt{\phi_{0sw}}}{V_2 - V_1} \cdot \left(\sqrt{\phi_{0sw} - V_2} - \sqrt{\phi_{0sw} - V_1} \right)$$

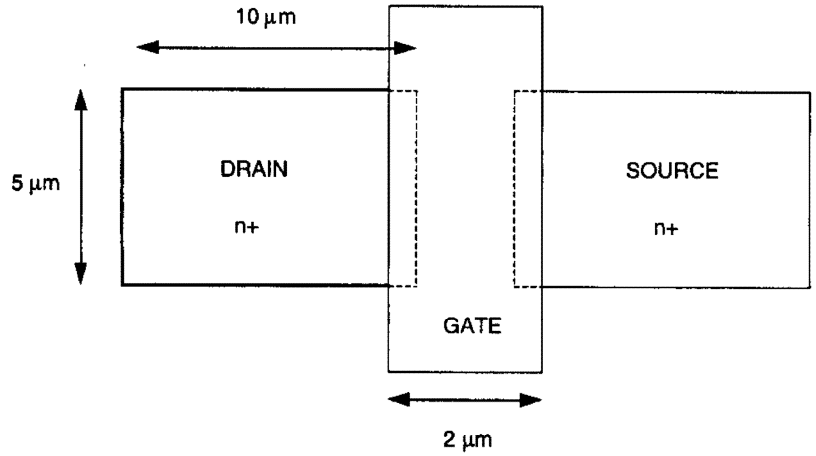
The equivalent large-signal junction capacitance $C_{eq(sw)}$ for a sidewall of length (perimeter) P can be

$$C_{eq(sw)} = P \cdot C_{jsw} \cdot K_{eq(sw)}$$

Example 8 (1)

Consider the n-channel enhancement-type MOSFET shown below. The process parameters are given as follows:

Substrate doping	$N_A = 2 \times 10^{15}\ \text{cm}^{-3}$
Source/drain doping	$N_D = 10^{19}\ \text{cm}^{-3}$
Sidewall (p^+) doping	$N_A(sw) = 4 \times 10^{16}\ \text{cm}^{-3}$
Gate oxide thickness	$t_{ox} = 45\ \text{nm}$
Junction depth	$x_j = 1.0\ \mu\text{m}$



Note that both the source and the drain diffusion regions are surrounded by p^+ channel-stop diffusion. The substrate is biased at 0 V. Assuming that the drain voltage is changing from 0.5 V to 5 V, find the average drain-substrate junction capacitance C_{db}.

First, we recognize that three sidewalls of the rectangular drain diffusion structure form n^+/p^+ junctions with the p^+ channel-stop implant, while the bottom area and the sidewall facing the channel form n^+/p junctions. Start by calculating the built-in potentials for both types of junctions.

$$\phi_0 = \frac{kT}{q} \cdot \ln\left(\frac{N_A \cdot N_D}{n_i^2}\right) = 0.026\ \text{V} \cdot \ln\left(\frac{2 \times 10^{15} \cdot 10^{19}}{2.1 \times 10^{20}}\right) = 0.837\ \text{V}$$

$$\phi_{0sw} = \frac{kT}{q} \cdot \ln\left(\frac{N_A(sw) \cdot N_D}{n_i^2}\right) = 0.026\ \text{V} \cdot \ln\left(\frac{4 \times 10^{16} \cdot 10^{19}}{2.1 \times 10^{20}}\right) = 0.915\ \text{V}$$

Example 8 (2)

Next, we calculate the zero-bias junction capacitances per unit area:

$$C_{j0} = \sqrt{\frac{\varepsilon_{Si} \cdot q}{2} \cdot \left(\frac{N_A \cdot N_D}{N_A + N_D}\right) \cdot \frac{1}{\phi_0}}$$

$$= \sqrt{\frac{11.7 \cdot 8.85 \times 10^{-14}\ \text{F/cm} \cdot 1.6 \times 10^{-19}\ \text{C}}{2} \cdot \left(\frac{2 \times 10^{15} \cdot 10^{19}}{2 \times 10^{15} + 10^{19}}\right) \cdot \frac{1}{0.837\ \text{V}}}$$

$$= 1.41 \times 10^{-8}\ \text{F/cm}^2$$

$$C_{j0sw} = \sqrt{\frac{\varepsilon_{Si} \cdot q}{2} \cdot \left(\frac{N_A(sw) \cdot N_D}{N_A(sw) + N_D}\right) \cdot \frac{1}{\phi_{0sw}}}$$

$$= \sqrt{\frac{11.7 \cdot 8.85 \times 10^{-14}\ \text{F/cm} \cdot 1.6 \times 10^{-19}\ \text{C}}{2} \cdot \left(\frac{4 \times 10^{16} \cdot 10^{19}}{4 \times 10^{16} + 10^{19}}\right) \cdot \frac{1}{0.915\ \text{V}}}$$

$$= 6.01 \times 10^{-8}\ \text{F/cm}^2$$

The zero-bias sidewall junction capacitance per unit length can also be found as follows.

$$C_{jsw} = C_{j0sw} \cdot x_j = 6.01 \times 10^{-8}\ \text{F/cm}^2 \cdot 10^{-4}\ \text{cm} = 6.01\ \text{pF/cm}$$

In order to take the given drain voltage variation into account, we must now calculate the voltage equivalence factors, K_{eq} and $K_{eq}(sw)$, for both types of junctions. This will allow us to find the average large-signal capacitance values.

$$K_{eq} = -\frac{2\sqrt{0.837}}{-5-(-0.5)} \cdot \left(\sqrt{0.837+5} - \sqrt{0.837+0.5}\right) = 0.51$$

$$K_{eq}(sw) = -\frac{2\sqrt{0.915}}{-5-(-0.5)} \cdot \left(\sqrt{0.915+5} - \sqrt{0.915+0.5}\right) = 0.53 \cong K_{eq}$$

The total area of the n^+/p junctions is calculated as the sum of the bottom area and the sidewall area facing the channel region.

$$A = (10 \times 5)\ \mu\text{m}^2 + (5 \times 1)\ \mu\text{m}^2 = 55\ \mu\text{m}^2$$

The total length of the n^+/p^+ junction perimeter, on the other hand, is equal to the sum of three sides of the drain diffusion area. Thus, the combined equivalent (average) drain-substrate junction capacitance can be found as follows:

$$\langle C_{db} \rangle = A \cdot C_{j0} \cdot K_{eq} + P \cdot C_{jsw} \cdot K_{eq}(sw)$$

$$= 55 \times 10^{-8}\ \text{cm}^2 \cdot 1.41 \times 10^{-8}\ \text{F/cm}^2 \cdot 0.51$$

$$+ 25 \times 10^{-4}\ \text{cm} \cdot 6.01 \times 10^{-12}\ \text{F/cm} \cdot 0.53 = 11.9 \times 10^{-15}\ \text{F} = \underline{\underline{11.9\ \text{fF}}}$$