VLSI Design (BEC-41)
(Unit-1, Lecture-2)

Presented By:

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The Metal Oxide Semiconductor (MOS) structure

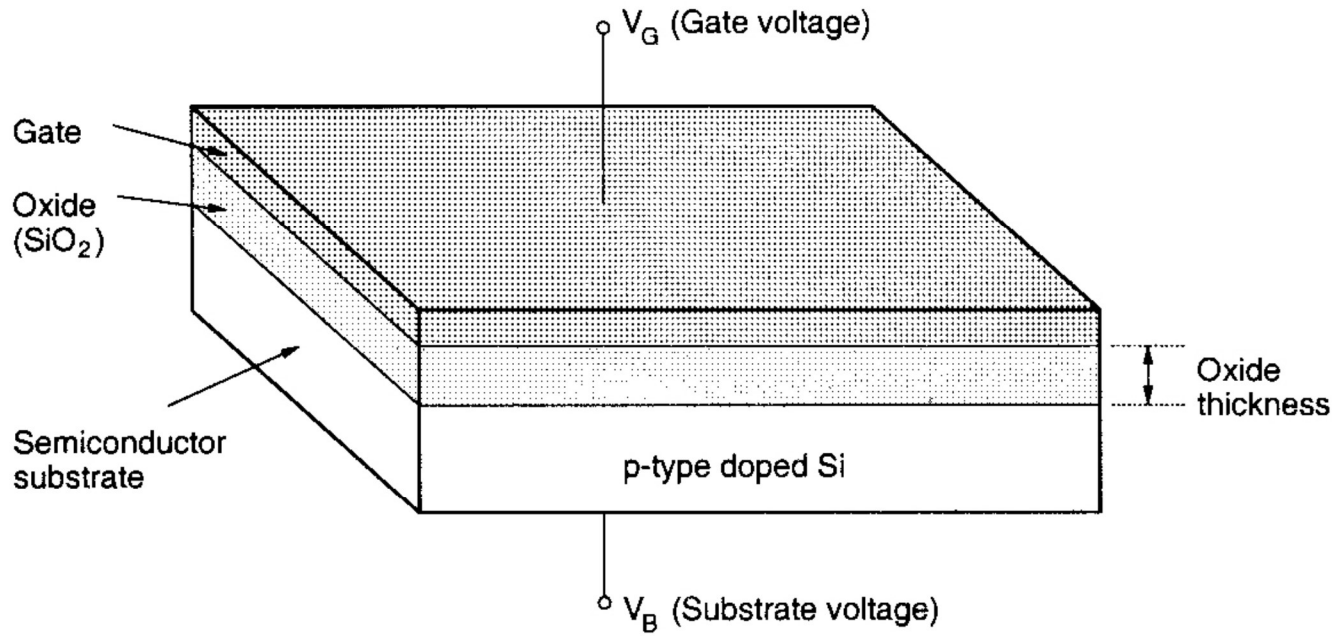


Figure 3.1 Two-terminal MOS structure.

- The structure consists of three layer
  - The metal gate electrode
  - The insulating oxide (SiO2) layer
  - The p-type bulk semiconductor

- The basic properties of the semiconductor

$$The\ mass\ action\ law: n \cdot p = n_i^2$$

$$Assume\ the\ substrate\ doping\ concentration\ N_A$$

$$then\ p_{n0} \cong \frac{n_i^2}{N_A}, \quad p_{p0} \cong N_A$$

Energy band diagram of a p-type silicon substrate

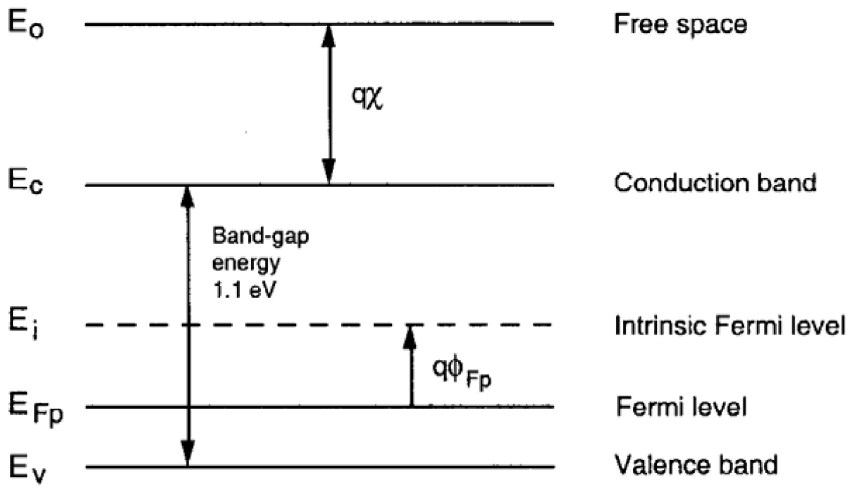


Figure 3.2 Energy band diagram of a p-type silicon substrate.

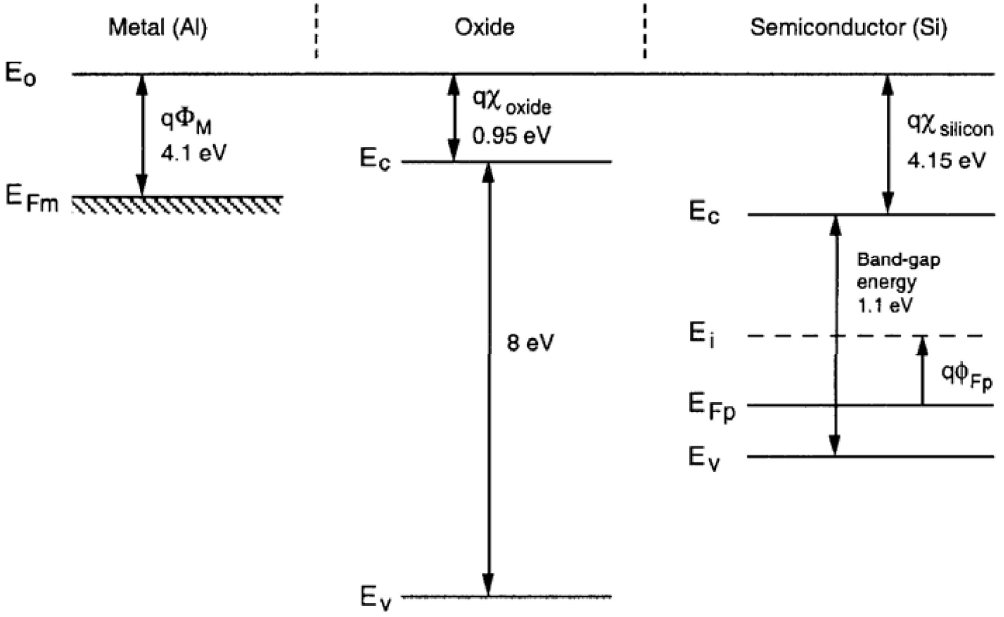


Figure 3.3 Energy band diagrams of the components that make up the MOS system.

The Fermi potential $\varphi_F = \dfrac{E_F - E_i}{q}$

For a p-type semiconductor, $\varphi_{Fp} = \dfrac{kT}{q} \ln \dfrac{n_i}{N_A}$

For a n-type semiconductor, $\varphi_{Fn} = \dfrac{kT}{q} \ln \dfrac{N_D}{n_i}$

The energy required for an electron to move from the Fermi level into *free space is called the work function*

$q\varphi_s = q\chi + (E_c - E_F)$

Energy diagram of the combined MOS system

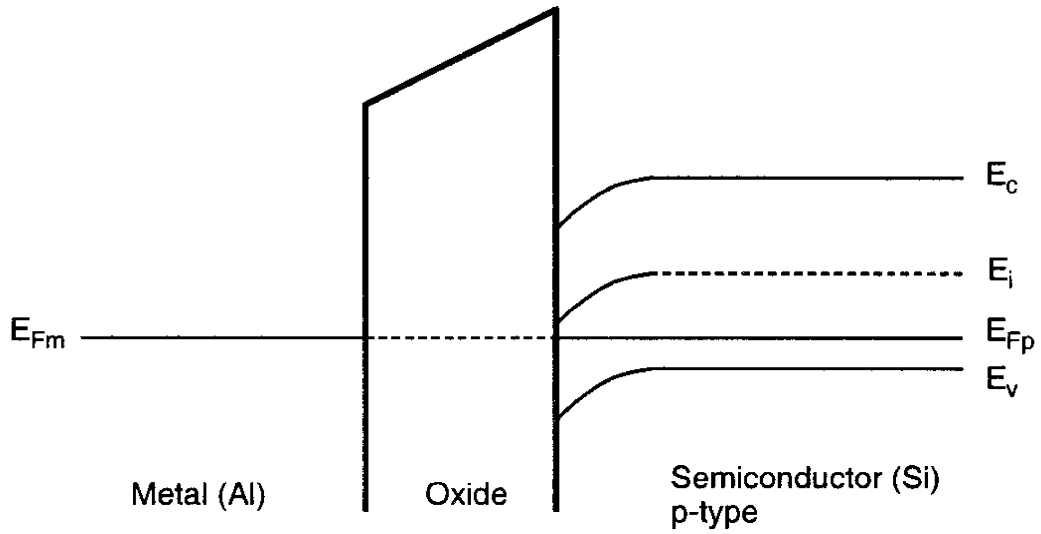


Figure 3.4 Energy band diagram of the combined MOS system.

- The equilibrium Fermi levels of the semiconductor (Si) substrate and the metal gate are at the same potential
- The bulk Fermi level is not significantly affected by the bending
- The surface Fermi level moves closer to the intrinsic Fermi level

Example 1

Consider the MOS structure that consists of a p-type doped silicon substrate, a silicon dioxide layer, and a metal (aluminum) gate. The equilibrium Fermi potential of the doped silicon substrate is given as $q\phi_{F_p} = 0.2$ eV. Using the electron affinity for silicon and the work function for aluminum given in Fig. 3.3, calculate the built-in potential difference across the MOS system. Assume that the MOS system contains no other charges in the oxide or on the silicon-oxide interface.

First, we have to calculate the work function for the doped silicon, which is given by (3.6). Since the electron affinity of silicon is 4.15 eV, the work function $q\Phi_S$ is found as

$$q\Phi_S = 4.15 \text{ eV} + 0.75 \text{ eV} = 4.9 \text{ eV}$$

Now calculate the work function difference between the silicon substrate and the aluminum gate. Note that the work function of aluminum is given as 4.1 eV in Fig. 3.3. Thus, the built-in potential difference across this MOS system is

$$q\Phi_M - q\Phi_S = 4.1 \text{ eV} - 4.9 \text{ eV} = -0.8 \text{ eV}$$

If a voltage corresponding to this potential difference is applied externally between the gate and the substrate, the bending of the energy bands near the surface can be compensated; i.e., the energy bands become "flat." Thus, the voltage defined by

$$V_{FB} = \Phi_M - \Phi_S$$

is called the *flat-band* voltage.

The MOS System under External Bias - accumulation

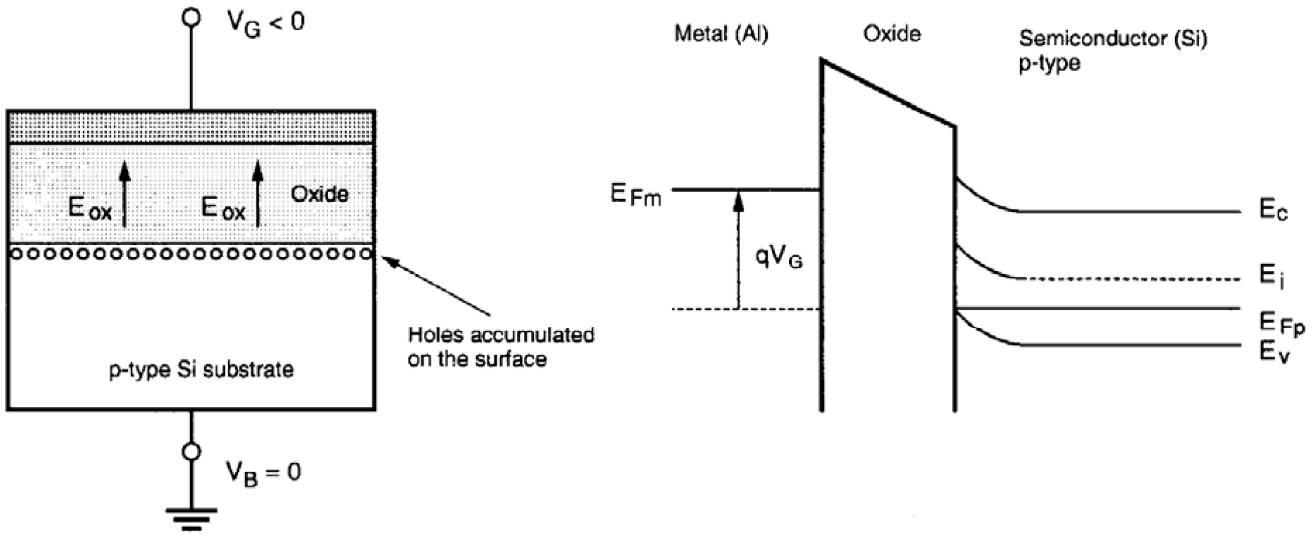


Figure 3.5 The cross-sectional view and the energy band diagram of the MOS structure operating in accumulation region.

- A negative voltage V_G is applied to the gate electrode.
  - The holes in the p-type substrate are attracted to the semiconductor-oxide surface
  - The majority carrier concentration > the equilibrium hole concentration
    - The electron concentration (minority carrier) decreases as the negatively charged electron are pushed deeper into the substrate
  - The oxide electric field is directed towards the gate electrode
  - Causing the energy bands bend up-ward near the surface

The MOS System under External Bias – depletion

- A small positive gate bias V_G is applied to the gate electrode
  - The oxide electric field will be directed towards the substrate
  - Causing the energy bands to bend downward near the surface
  - The majority carrier (hole) will be repelled backed into the substrate
    - Leaving negatively charged fixed acceptor ions behind (depletion region)

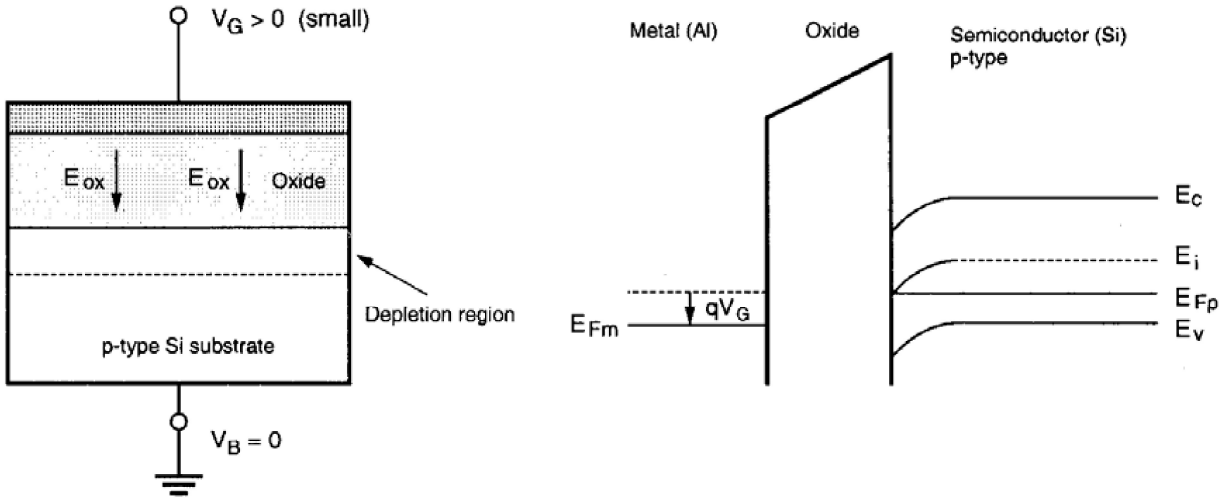


Figure 3.6 The cross-sectional view and the energy band diagram of the MOS structure operating in depletion mode, under small gate bias.

$$dQ = -q \cdot N_A \cdot dx$$

$$d\phi_s = -x \cdot \frac{dQ}{dx} = \frac{q \cdot N_A \cdot x}{\varepsilon_{Si}} dx$$

$$\int_{\phi_F}^{\phi_s} d\phi_s = \int_0^{x_d} \frac{q \cdot N_A \cdot x}{\varepsilon_{Si}} dx$$

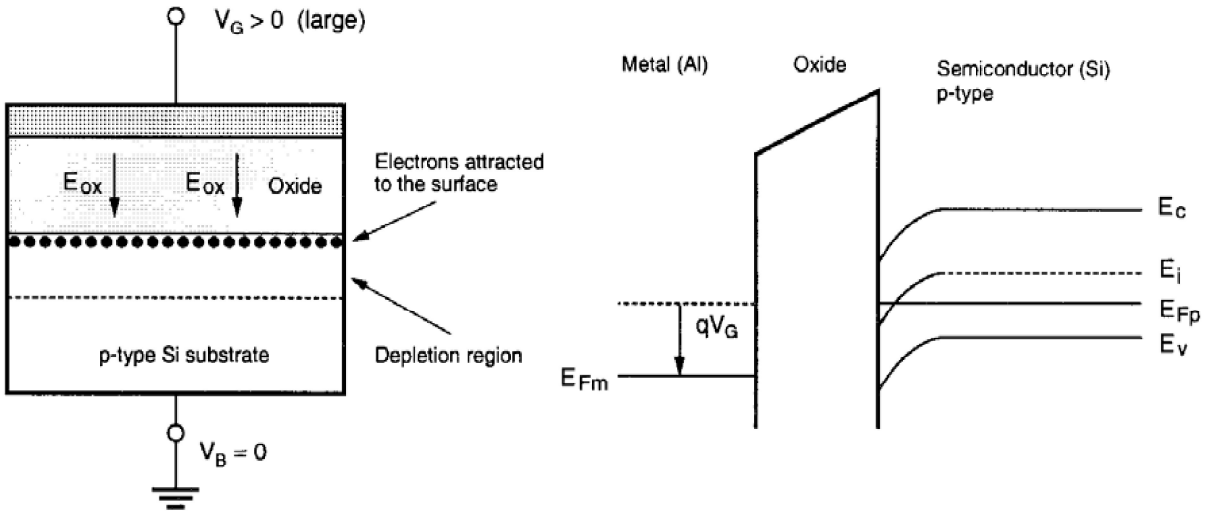
$$\phi_s - \phi_F = \frac{q \cdot N_A \cdot x_d^2}{\varepsilon_{Si}}$$

$$x_d = \sqrt{\frac{2\varepsilon_{Si} \cdot |\phi_s - \phi_F|}{q \cdot N_A}}$$

$$Q = -q \cdot N_A \cdot x_d = -\sqrt{2q \cdot N_A \cdot \varepsilon_{Si} \cdot |\phi_s - \phi_F|}$$

The MOS System under External Bias – inversion

- A further increase in the positive gate bias
  - Increasing surface potential ⇨the downward bending of the energy bands will increase
  - The mid-gap energy level E_i becomes smaller than the Fermi level E_{Fp} on the surface
    - The substrate semiconductor in this region become n-type
    - The electron density is larger than the majority hole density
    - Inversion layer, surface inversion
    - Can be utilized for conducting current between two terminal of the MOS transistor
  - The surface is said to be *inverted*
    - *The density of mobile electrons on the surface becomes equal to the density of holes in the bulk substrate*
    - Requiring the surface potential has the same magnitude, but the reverse polarity, as the bulk Fermi potential ϕ_F
    - Further increase gate voltage ⇨ electron concentration↑ ⇨ but not to an increase of the depletion depth



$$x_{dm} = \sqrt{\frac{2 \cdot \varepsilon_{Si} \cdot |2\phi_F|}{q \cdot N_A}}$$

Figure 3.7 The cross-sectional view and the energy band diagram of the MOS structure in surface inversion, under larger gate bias voltage.

The physical structure of a n-channel enhancement-type MOSFET

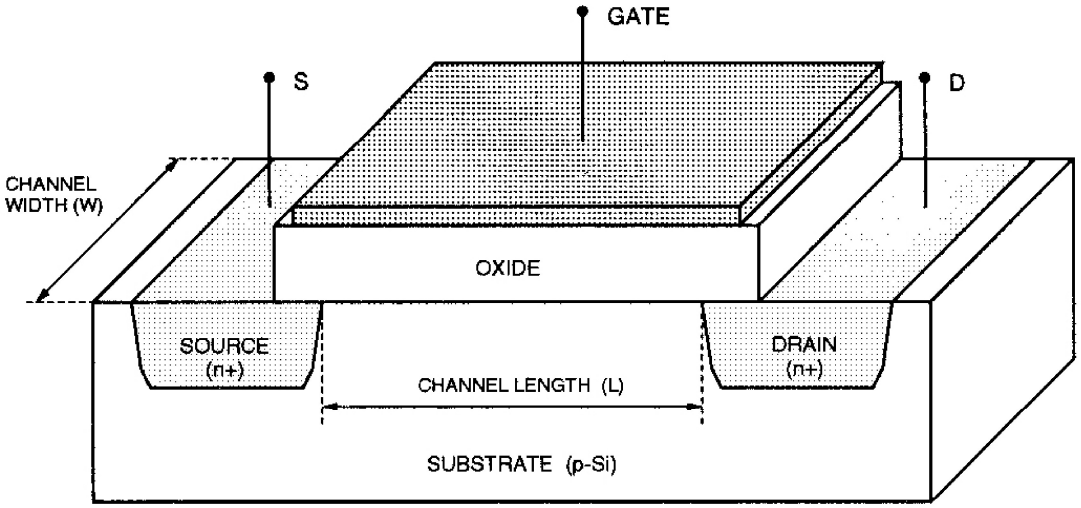


Figure 3.8 The physical structure of an n-channel enhancement-type MOSFET.

- MOS structure
  - polysilicon gate, thin oxide layer, semiconductor
- Source, drain n^+-region
  - The current conducting terminals of the device
    - Conducting channel, channel length L, channel width W
  - The device structure is completely symmetrical with respect to the drain and source
- The simple operation of this device
  - *Controlling the current conduction between the source and the drain, using the electric field generated by the gate voltage as a control variable*

Circuit symbols for enhancement-type MOSFET

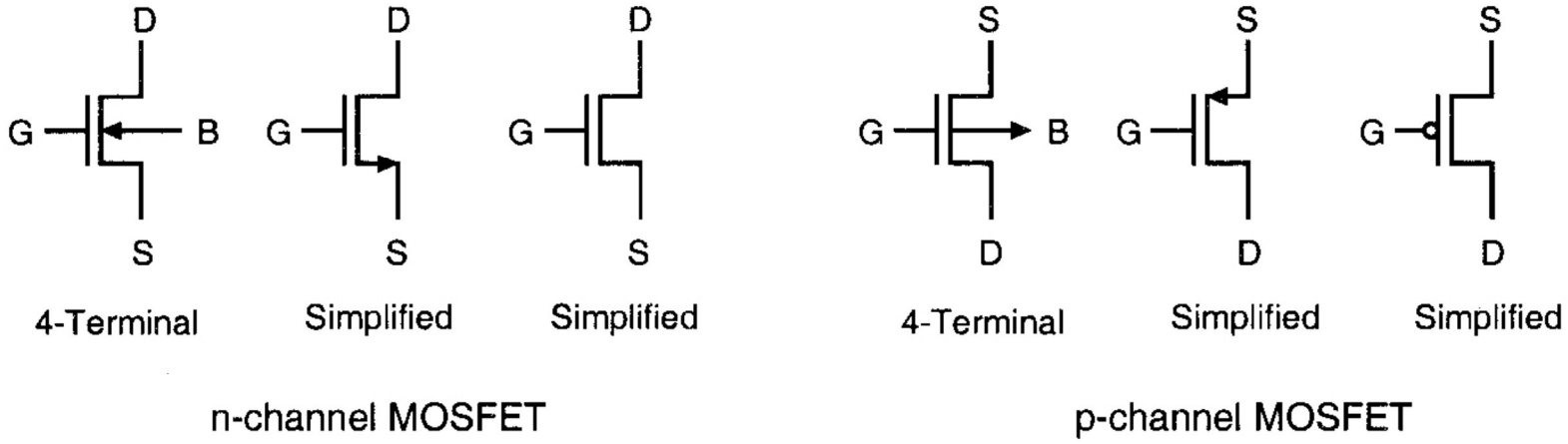


Figure 3.9 Circuit symbols for n-channel and p-channel enhancement-type MOSFETs.

- Enhancement-mode MOSFET
  - No conducting region at zero gate bias
- Depletion-mode MOSFET
  - A conducting channel already exists at zero gate bias
- The abbreviations used for device terminals are
  - G for the gate, D for the drain, S for the source, and B for the substrate
- The small arrow always marks the source terminal

Formation of a depletion region

- For small gate voltage level
  - The majority carriers (holes) are repelled back into the substrate
  - The surface of the p-type substrate is depleted
  - Current conduction between S and D is not possible

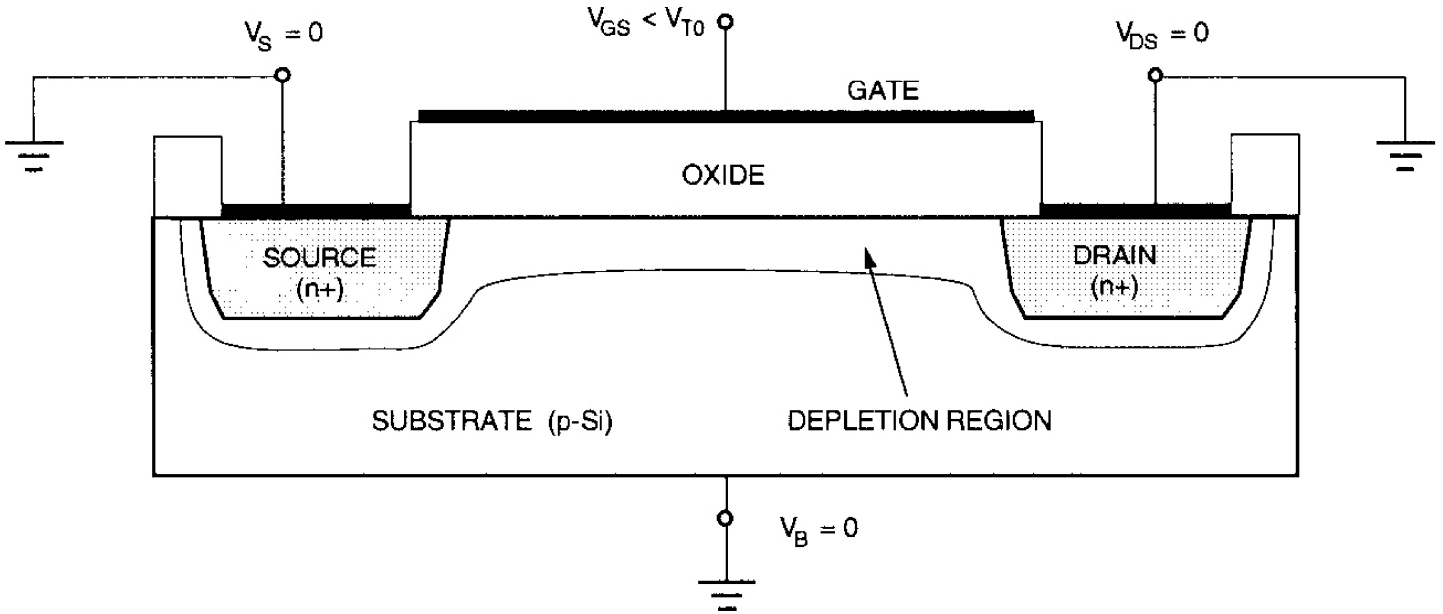


Figure 3.10 Formation of a depletion region in an n-channel enhancement-type MOSFET.

Formation of an inversion layer

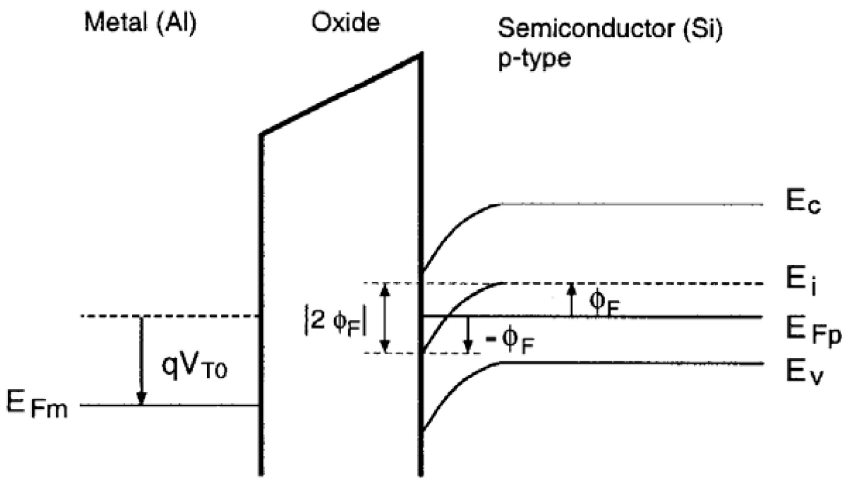


Figure 3.11 Band diagram of the MOS structure underneath the gate, at surface inversion. Notice the band bending by $|2\phi_F|$ at the surface.

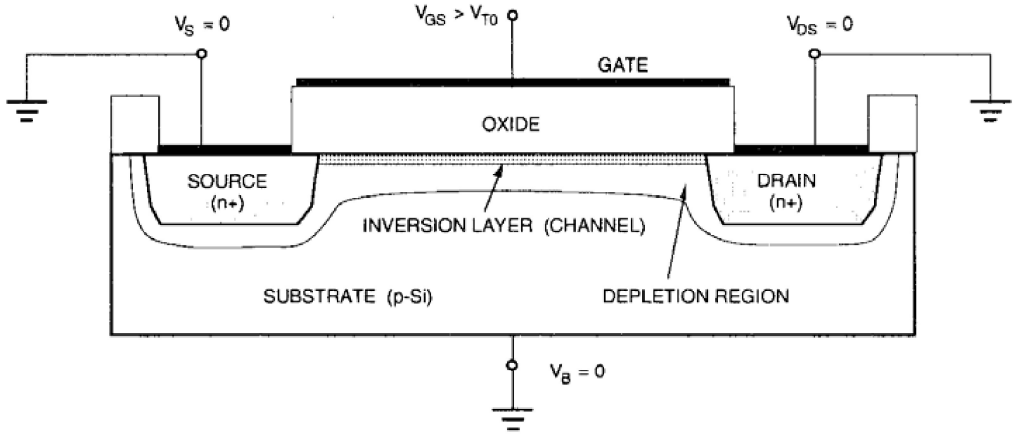


Figure 3.12 Formation of an inversion layer (channel) in an n-channel enhancement-type MOSFET.

- As the gate-to-source voltage is further increased
  - The surface potential reaches $-\phi_{Fp}$ ⇨ surface inversion will be established ⇨ conducting channel between S and D
  - Allowing current flow, as log as there is a potential difference between S and D
  - $V_{GS}<V_{T0}$ (threshold voltage)
    - Not sufficient to establish an inversion layer
    - No current between S and D
  - $V_{GS}>V_{T0}$ (threshold voltage)
    - Electrons are attracted to the surface
      - Contributing to channel current conduction
  - Further increase gate voltage
    - Not affect the surface potential and the depletion region depth

The threshold voltage

- Four physical components of V_{T0}
  - The work function difference between gate and the channel
    - ϕ_{GC}= ϕ_F(substrate)- ϕ_M for metal gate
    - ϕ_{GC}= ϕ_F(substrate)- ϕ_F(gate) for polysilicon gate
  - The gate voltage component to change the surface potential
    - To change the surface potential by $-2\phi_F$
  - The gate voltage component to offset the depletion region charge
    - $-Q_B/C_{ox}$
    - $$Q_B = -\sqrt{2q \cdot N_A \cdot \varepsilon_{Si} \cdot |-2\phi_F + V_{SB}|}$$
      $$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$
  - The voltage component to offset the fixed charge in the gate oxide and in the silicon-oxide interface
    - $-Q_{ox}/C_{ox}$
    - $$V_{T0} = \Phi_{GC} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} \text{ (no body effect)}$$
      $$V_T = V_{T0} + \gamma \cdot \left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right) \text{(with body effect)}$$
      $$\text{where } \gamma = \frac{\sqrt{2q \cdot N_A \cdot \varepsilon_{Si}}}{C_{ox}}$$

- Compared with the p-MOSFET
  - The substrate Fermi potential ϕ_F is negative in NMOS, positive in pMOS
  - The depletion region charge densities Q_{B0} and Q_B are negative in nMOS, positive in pMOS
  - The substrate bias coefficient γ is positive in nMOS, negative in pMOS
  - The substrate bias voltage V_{SB} is positive in nMOS, negative in pMOS

- Threshold voltage adjustment
  - Implanting p-type impurity ⇨ V_T increased
  - Implanting n-type impurity ⇨ V_T decreased
  - The amount of change in the threshold voltage
    - Shift qN_I/C_{ox}