VLSI Design (BEC-41)
(Unit-2, Lecture-4)

Presented By:

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CMOS Inverter

- The CMOS inverter has two important advantages over the other inverter configurations:
- The first and perhaps the most important advantage is that the steady-state power dissipation of the CMOS inverter circuit is virtually negligible, except for small power dissipation due to leakage currents. In all other inverter structures examined so far, a nonzero steady-state current is drawn from the power source when the driver transistor is turned on, which results in a significant DC power consumption.
- The other advantages of the CMOS configuration are that the voltage transfer characteristic (VTC) exhibits a full output voltage swing between 0 V and V_{DD}, and that the VTC transition is usually very sharp. Thus, the VTC of the CMOS inverter resembles that of an ideal inverter.

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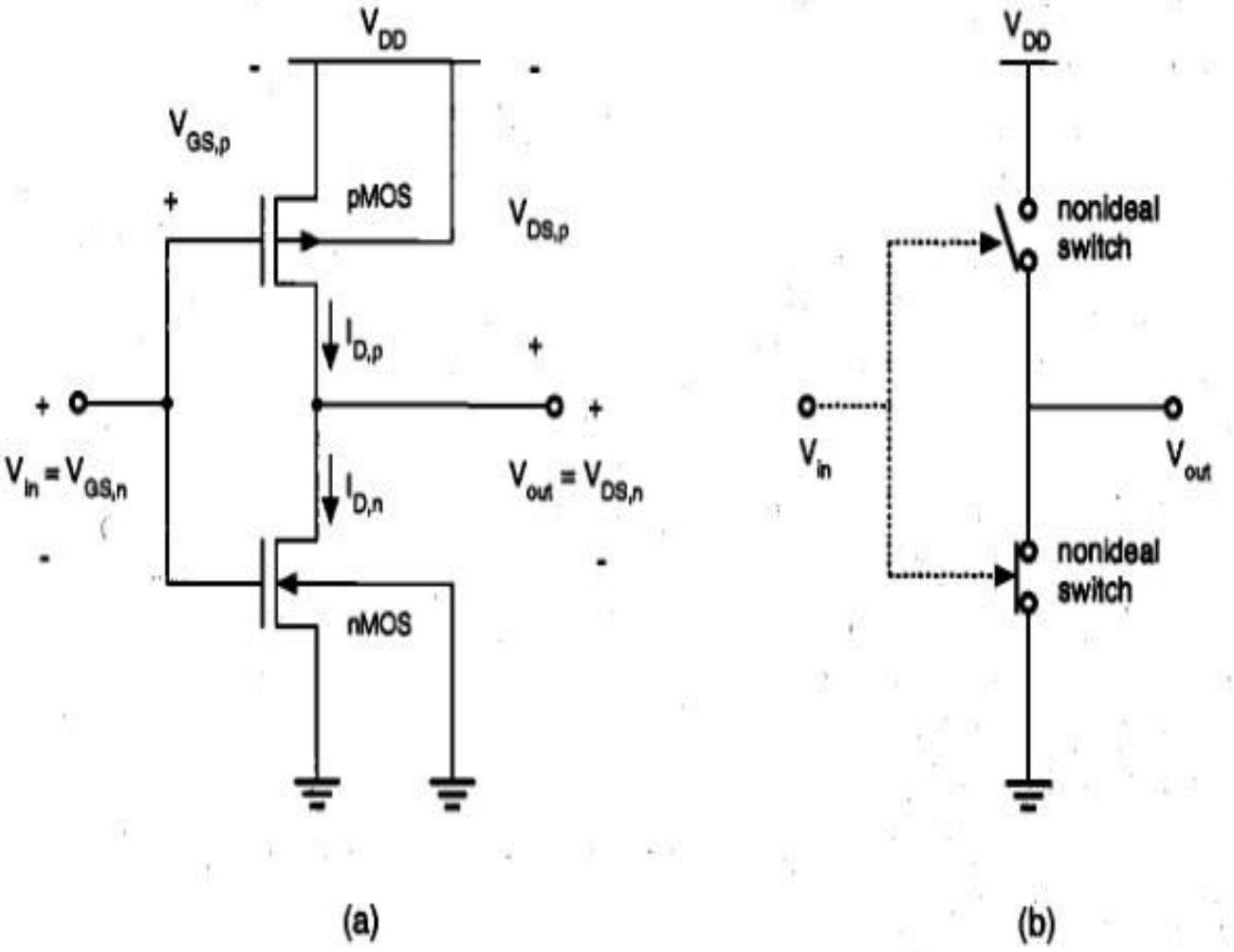

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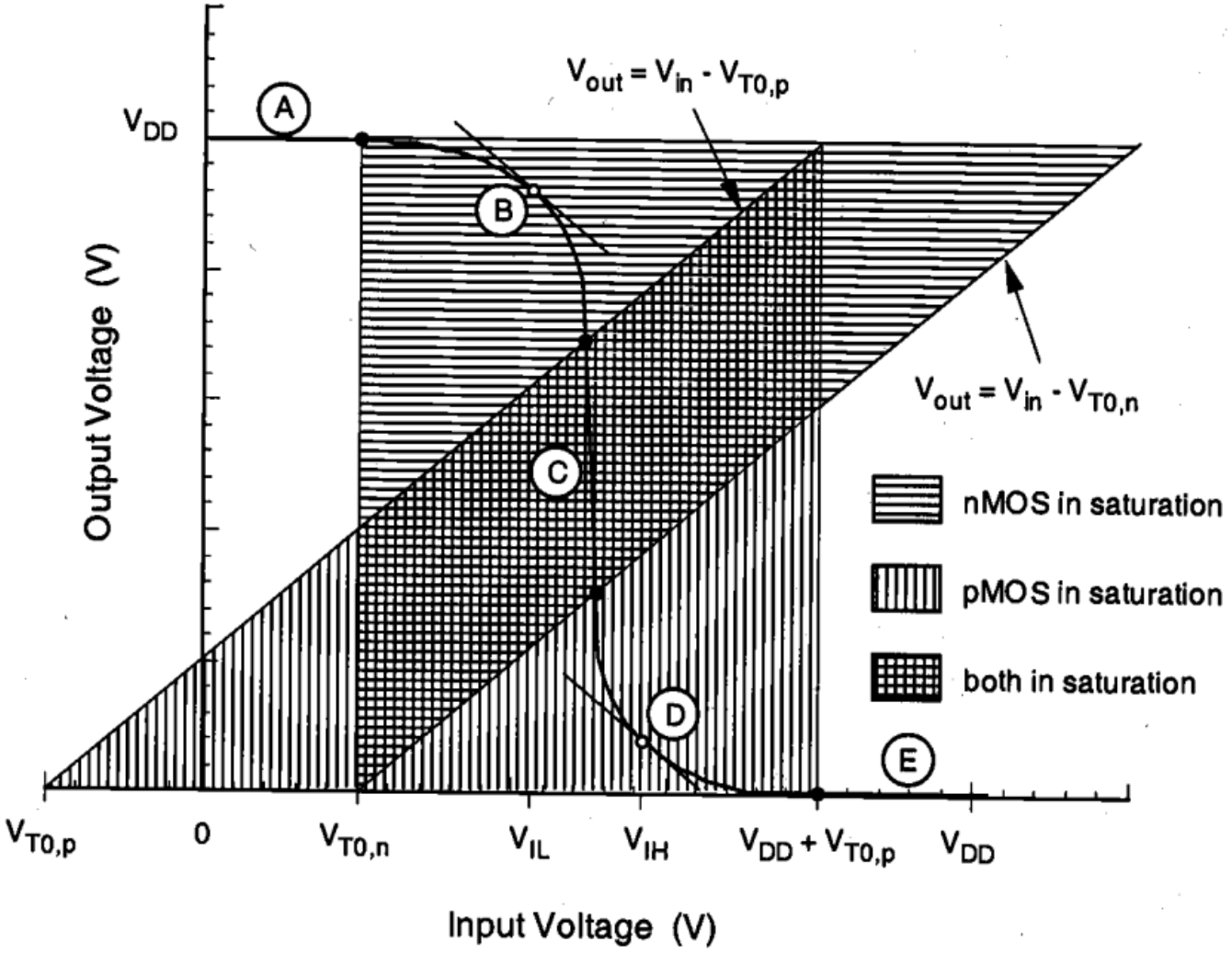

Fig. Operating regions of the nMOS and the pMOS transistors.

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Region	V_{in}	V_{out}	nMOS	pMOS
A	$< V_{T0,n}$	V_{OH}	cut-off	linear
B	V_{IL}	high $\approx V_{OH}$	saturation	linear
C	V_{th}	V_{th}	saturation	saturation
D	V_{IH}	low $\approx V_{OL}$	linear	saturation
E	$>\left(V_{DD}+V_{T0,p}\right)$	V_{OL}	linear	cut-off

- In **Region A**, where Vin< V_{T0}, the NMOS transistor is cut-off and the output voltage is equal to $V_{OH} = V_{DD}$.
- As the input voltage is increased beyond $V_{T0,n}$, (into **Region B**), the NMOS transistor starts conducting in saturation mode and the output voltage begins to decrease. Also note that the critical voltage V_{IL} which corresponds to $(dV_{out}/dV_{in}) = -1$ is located within **Region B**.

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- As the output voltage further decreases, the PMOS transistor enters saturation at the boundary of **Region C**. It is seen from figure that the inverter threshold voltage, where $V_{in}= V_{out}$, is located in **Region C**.
- When the output voltage V_{out}, falls below $(Vin – V_{T0,n})$, the NMOS transistor starts to operate in linear mode. This corresponds to **Region D** in figure, where the critical voltage point V_{IH} with $(dV_{out}/dV_{jn}) = -1$ is also located.
- Finally, in **Region E**, with the input voltage $V_{in} > (V_{DD} + V_{T0,p})$, the PMOS transistor is cut-off, and the output voltage is $V_{OL}= 0$.
- It has already been established that $V_{OH} = V_{DD}$ and $V_{OL} = 0$ for this inverter; thus, we will devote our attention to V_{IL}, V_{IH} and the inverter switching threshold, V_{th}.

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Calculation of V_{IL}

- By definition, the slope of the VTC is equal to (-1), i.e., $dV_{out}/dV_{in} = -1$ when the input voltage is $V_{in} = V_{IL}$.
- Note that in this case, the NMOS transistor operates in saturation while the PMOS transistor operates in the linear region.
- From $I_{D,n} = I_{D,p}$, we obtain the following current equation:

$$\frac{k_n}{2}\cdot\left(V_{GS,n}-V_{T0,n}\right)^2=\frac{k_p}{2}\cdot\left[2\cdot\left(V_{GS,p}-V_{T0,p}\right)\cdot V_{DS,p}-{V_{DS,p}}^2\right]$$

$$\frac{k_n}{2}\cdot\left(V_{in}-V_{T0,n}\right)^2=\frac{k_p}{2}\cdot\left[2\cdot\left(V_{in}-V_{DD}-V_{T0,p}\right)\cdot\left(V_{out}-V_{DD}\right)-\left(V_{out}-V_{DD}\right)^2\right]$$

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Calculation of V_{IL}

- To satisfy the derivative condition at V_{IL} , we differentiate both sides with respect to V_{in}.

$$k_n \cdot (V_{in} - V_{T0,n}) = k_p \cdot \left[(V_{in} - V_{DD} - V_{T0,p}) \cdot \left(\frac{dV_{out}}{dV_{in}} \right) + (V_{out} - V_{DD}) - (V_{out} - V_{DD}) \cdot \left(\frac{dV_{out}}{dV_{in}} \right) \right]$$

- Substituting $V_{in} = V_{IL}$ and $(dV_{out} / dV_{in}) = -1$ in above equation, we obtain:

$$V_{IL} = \frac{2V_{out} + V_{T0,p} - V_{DD} + k_R V_{T0,n}}{1 + k_R}$$

where k_R is defined as: $k_R = \frac{k_n}{k_p}$

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Calculation of V_{IH}

- When the input voltage is equal to V_{IH}, the NMOS transistor operates in the linear region, and the PMOS transistor operates in saturation. Applying KCL to the output node, we obtain

$$\frac{k_n}{2}\cdot\left[2\cdot\left(V_{GS,n}-V_{T0,n}\right)\cdot V_{DS,n}-{V_{DS,n}}^2\right]=\frac{k_p}{2}\cdot\left(V_{GS,p}-V_{T0,p}\right)^2$$

$$\frac{k_n}{2}\cdot\left[2\cdot\left(V_{in}-V_{T0,n}\right)\cdot V_{out}-{V_{out}}^2\right]=\frac{k_p}{2}\cdot\left(V_{in}-V_{DD}-V_{T0,p}\right)^2$$

- Now, differentiate both sides with respect to V_{in}:

$$k_n\cdot\left[\left(V_{in}-V_{T0,n}\right)\cdot\left(\frac{dV_{out}}{dV_{in}}\right)+V_{out}-V_{out}\cdot\left(\frac{dV_{out}}{dV_{in}}\right)\right]$$

$$=k_p\cdot\left(V_{in}-V_{DD}-V_{T0,p}\right)$$

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Calculation of V_{IH}

- Substituting, $V_{in} = V_{IH}$ and $(dV_{out}/ dV_{in}) = -1$ in above equation, we obtain

$$k_n \cdot \left(-V_{IH} + V_{T0,n} + 2V_{out}\right) = k_p \cdot \left(V_{IH} - V_{DD} - V_{T0,p}\right)$$

$$V_{IH} = \frac{V_{DD} + V_{T0,p} + k_R \cdot \left(2V_{out} + V_{T0,n}\right)}{1 + k_R}$$

- Again, this equation must be solved simultaneously with the KCL equation to obtain the numerical values of V_{IH} and V_{out}.

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Calculation of V_{th}

- The inverter threshold voltage is defined as $V_{th} = V_{th} = V_{out}$, Since the CMOS inverter exhibits large noise margins and a very sharp VTC transition, the inverter threshold voltage emerges as an important parameter characterizing the DC performance of the inverter.
- For $V_{in} = V_{out}$, both transistors are expected to be in saturation mode; hence, we can write the following KCL equation:

$$\frac{k_n}{2}\cdot\left(V_{GS,n}-V_{T0,n}\right)^2=\frac{k_p}{2}\cdot\left(V_{GS,p}-V_{T0,p}\right)^2$$

$$\frac{k_n}{2}\cdot\left(V_{in}-V_{T0,n}\right)^2=\frac{k_p}{2}\cdot\left(V_{in}-V_{DD}-V_{T0,p}\right)^2$$

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Calculation of V_{th}

- The correct solution for V_{in} for this equation is:

$$V_{in} \cdot \left(1+\sqrt{\frac{k_p}{k_n}}\right) = V_{T0,n} + \sqrt{\frac{k_p}{k_n}} \cdot \left(V_{DD} + V_{T0,p}\right)$$

- Finally, the inverter threshold (switching threshold) voltage V_{th}, is found as

$$V_{th} = \frac{V_{T0,n} + \sqrt{\frac{1}{k_R}} \cdot \left(V_{DD} + V_{T0,p}\right)}{\left(1+\sqrt{\frac{1}{k_R}}\right)}$$

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Calculation of V_{th}

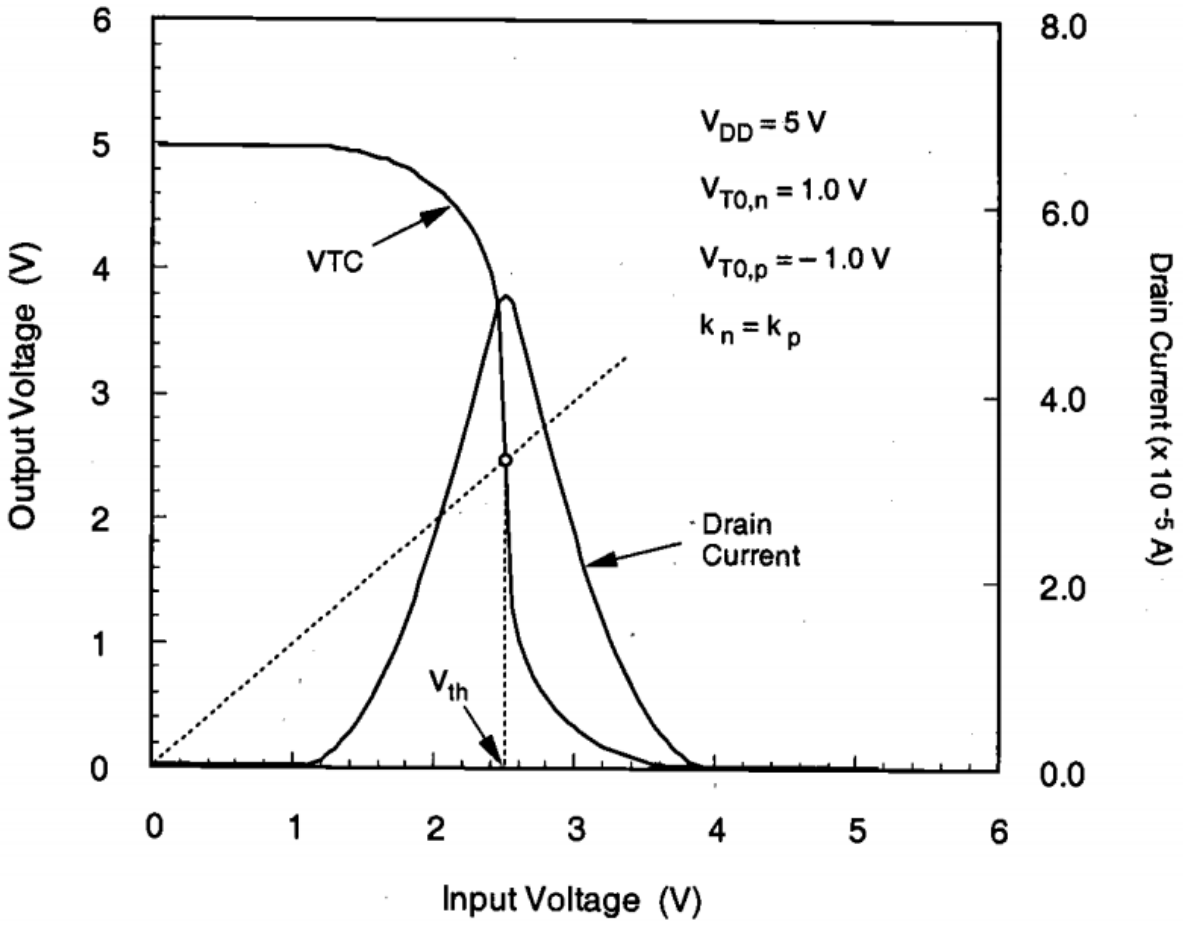

Fig. Typical VTC and the power supply current of a CMOS inverter circuit.

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Calculation of V_{th}

- Now solve for kR that is required to achieve the given V_{th}:

$$k_R = \frac{k_n}{k_p} = \left(\frac{V_{DD} + V_{T0,p} - V_{th}}{V_{th} - V_{T0,n}} \right)^2$$

- Recall that the switching threshold voltage of an ideal inverter is defined as:

$$V_{th,ideal} = \frac{1}{2} \cdot V_{DD}$$

$$\left(\frac{k_n}{k_p} \right)_{ideal} = \left(\frac{0.5 V_{DD} + V_{T0,p}}{0.5 V_{DD} - V_{T0,n}} \right)^2$$

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Calculation of V_{th}

- For a near-ideal CMOS VTC that satisfies the above condition. Since the operations of the NMOS and the PMOS transistors of the CMOS inverter are fully complementary, we can achieve completely symmetric input-output characteristics by setting the threshold voltages as $V_{T0} = V_{T0,p} = |V_{T0,p}|$. This reduces to:

$$\left(\frac{k_n}{k_p}\right)_{\substack{symmetric\\ inverter}} = 1$$

$$\frac{k_n}{k_p} = \frac{\mu_n C_{ox} \cdot \left(\frac{W}{L}\right)_n}{\mu_p C_{ox} \cdot \left(\frac{W}{L}\right)_p} = \frac{\mu_n \cdot \left(\frac{W}{L}\right)_n}{\mu_p \cdot \left(\frac{W}{L}\right)_p}$$

$$\frac{\left(\frac{W}{L}\right)_n}{\left(\frac{W}{L}\right)_p} = \frac{\mu_p}{\mu_n} \approx \frac{230\ \text{cm}^2/\text{V}\cdot\text{s}}{580\ \text{cm}^2/\text{V}\cdot\text{s}}$$

$$\left(\frac{W}{L}\right)_p \approx 2.5\left(\frac{W}{L}\right)_n$$

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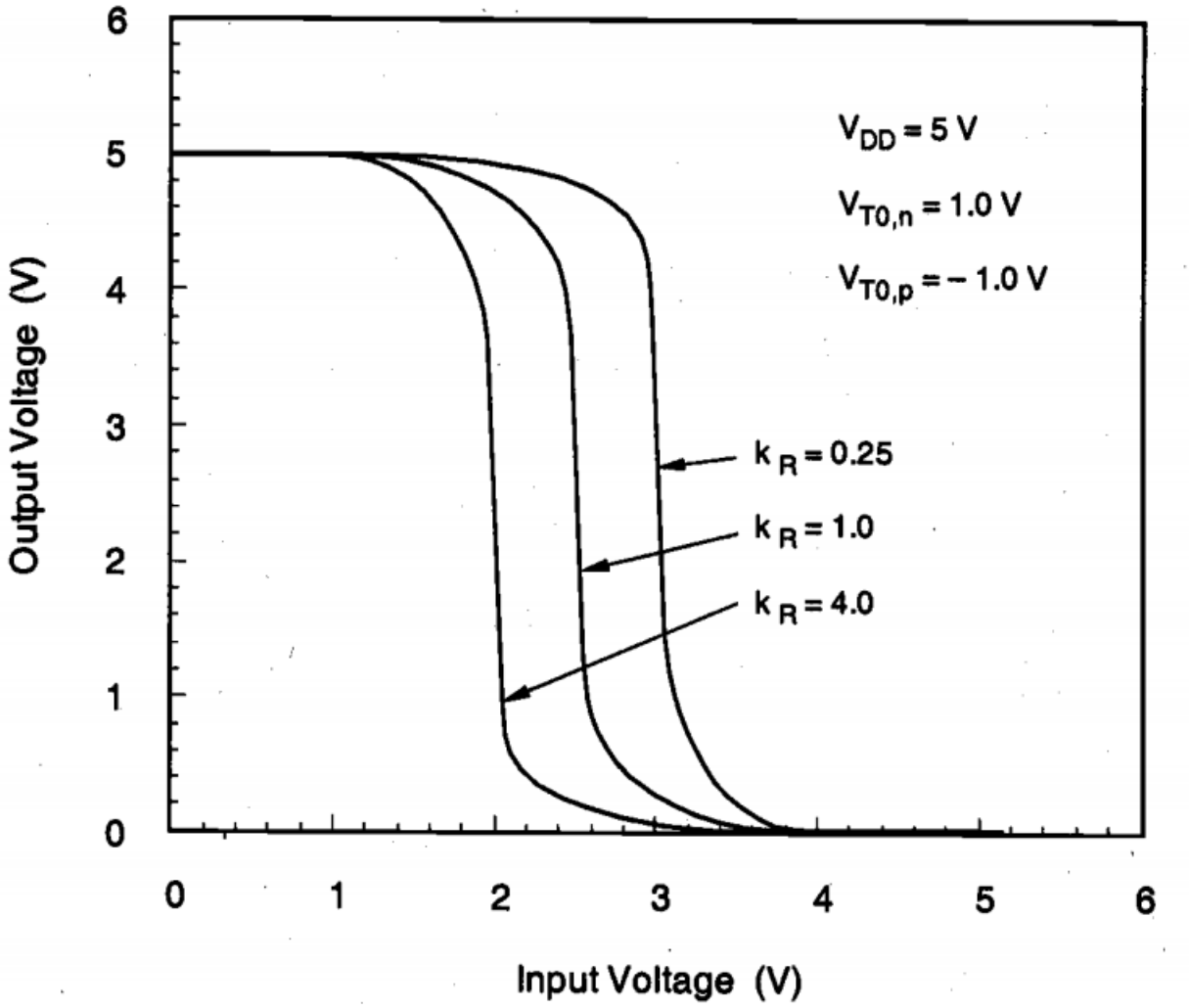

Fig. Voltage transfer characteristics of three CMOS inverters, with different NMOS-to-PMOS ratios.