VLSI Design (BEC-41)
(Unit-2, Lecture-1)

Presented By:

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Department of Electronics and Communication Engineering

Fabrication Process Flow: Basic Steps

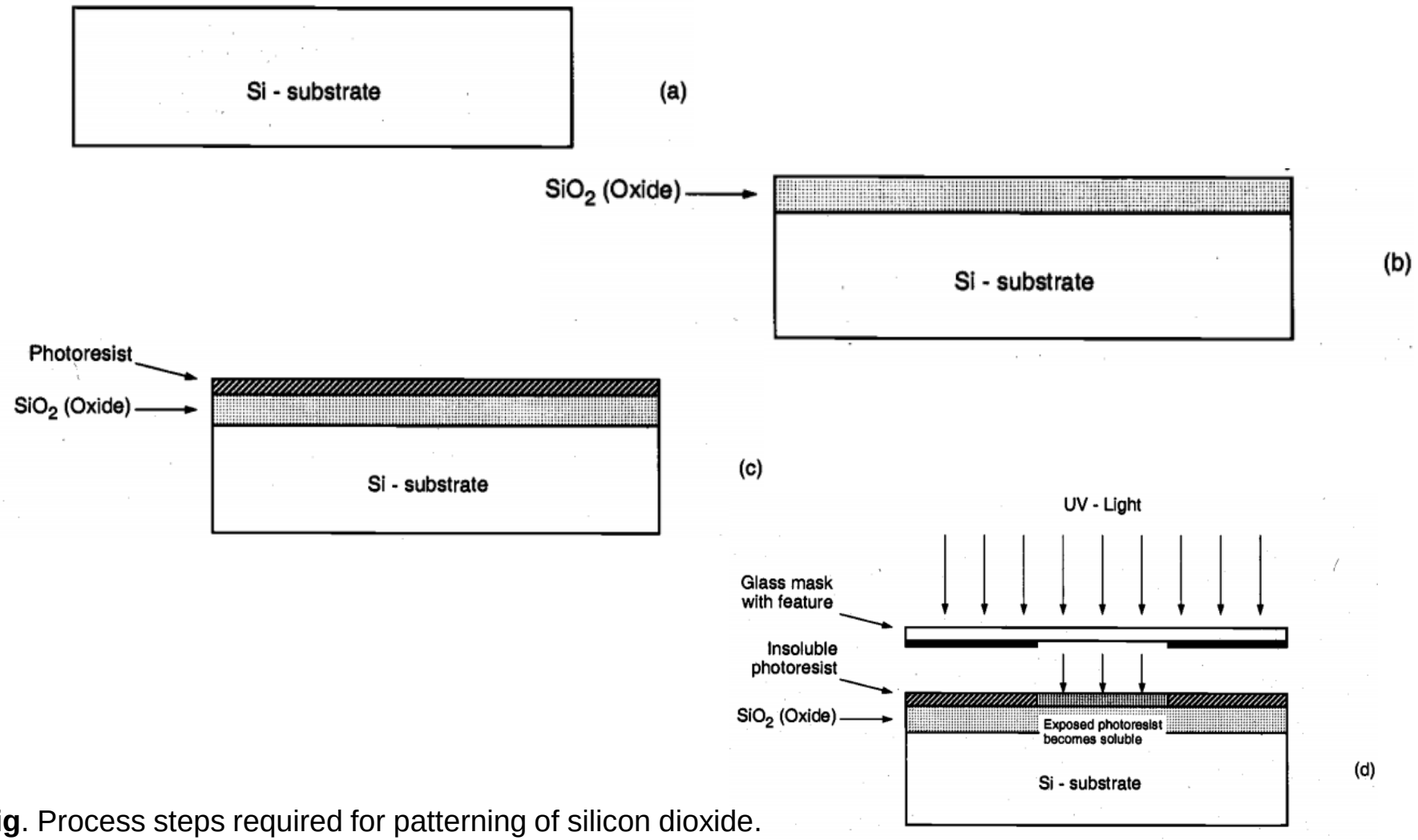


Fig. Process steps required for patterning of silicon dioxide.

Fabrication Process Flow: Basic Steps

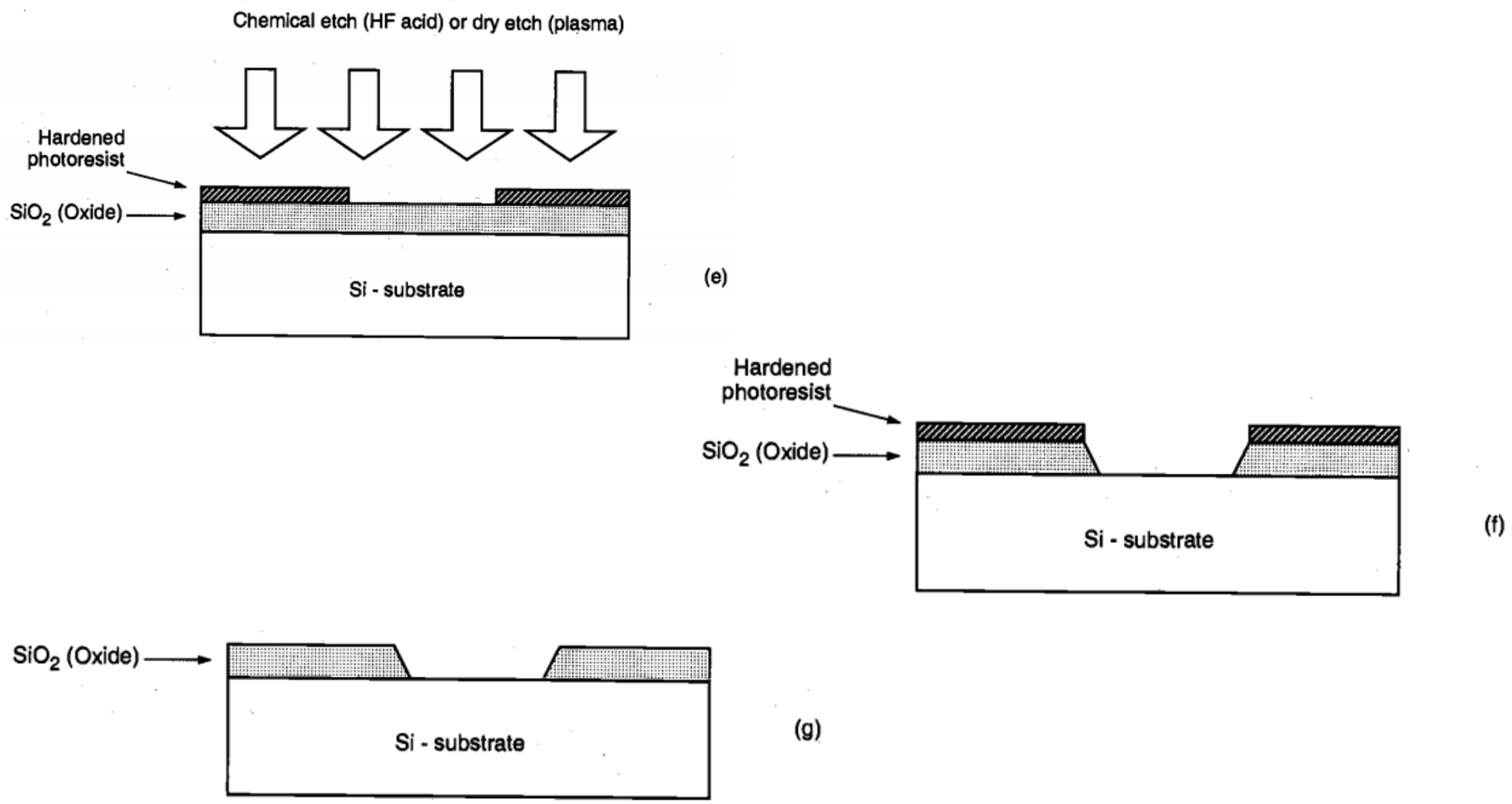
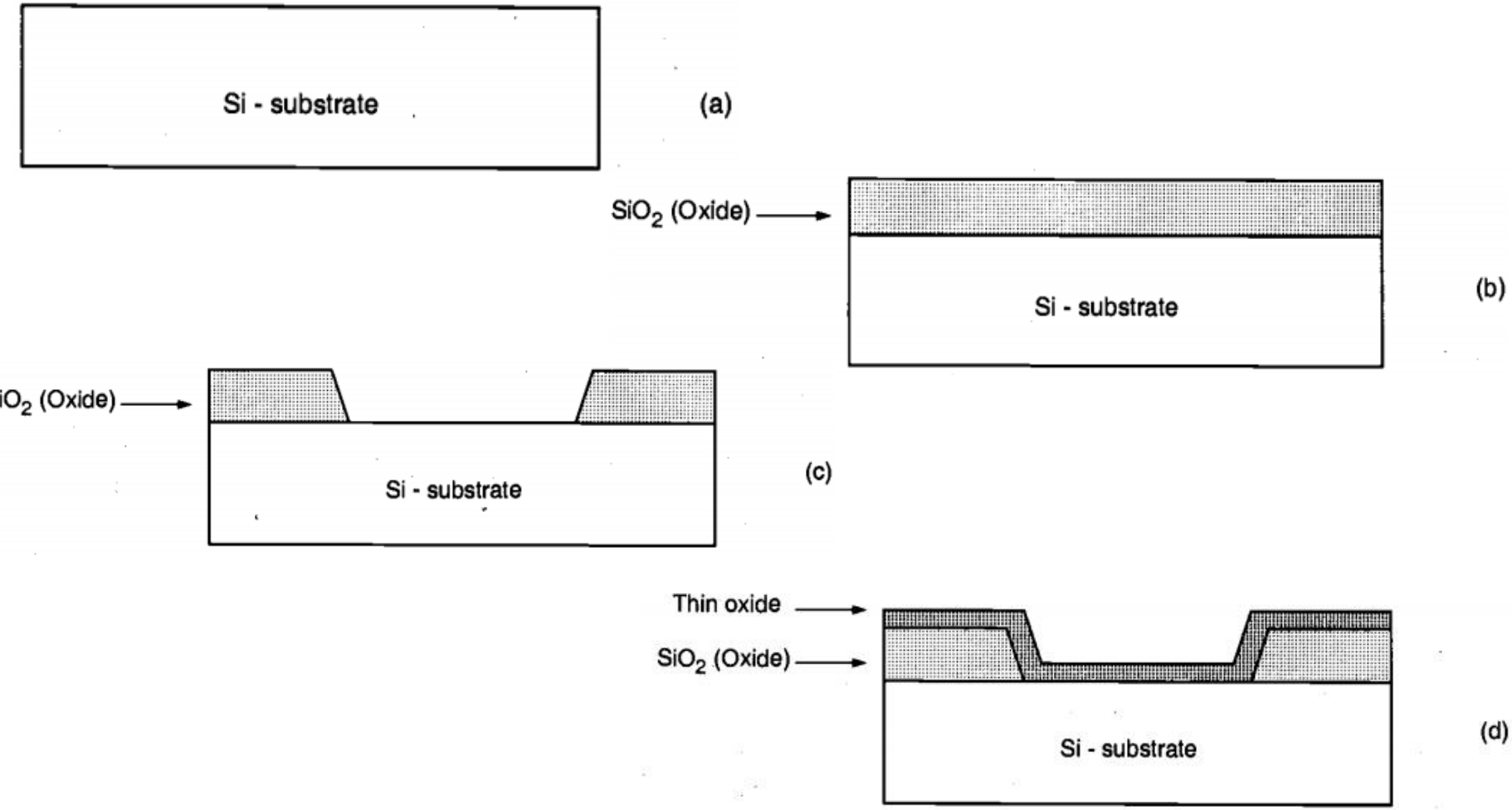
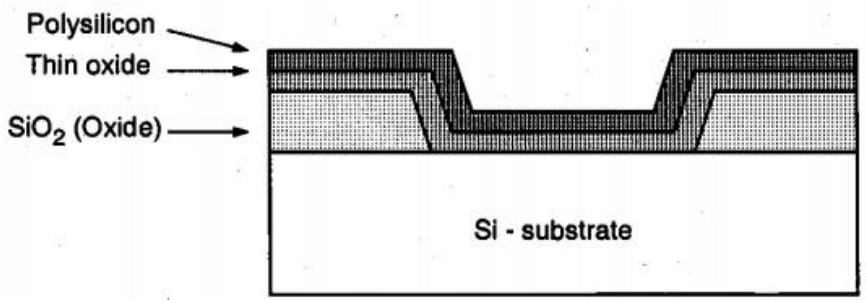


Fig. Process steps required for patterning of silicon dioxide (continued).

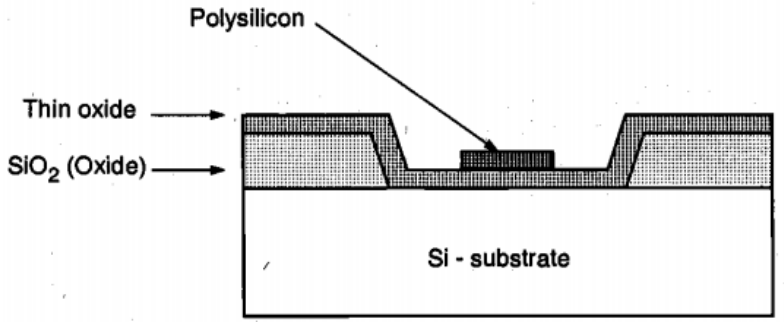
Fabrication of the nMOS Transistor



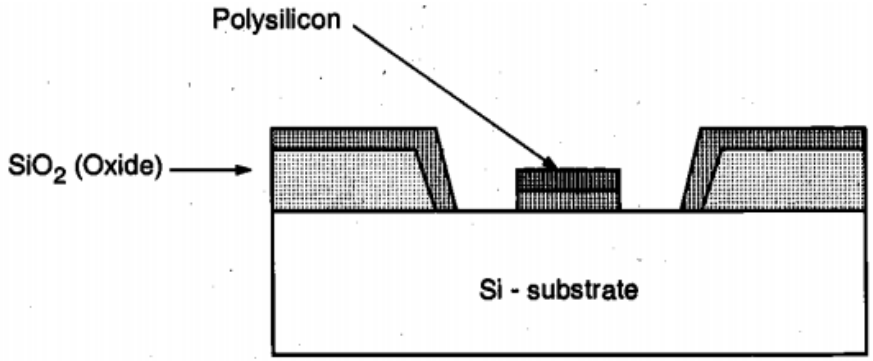
Fabrication of the nMOS Transistor



(e)

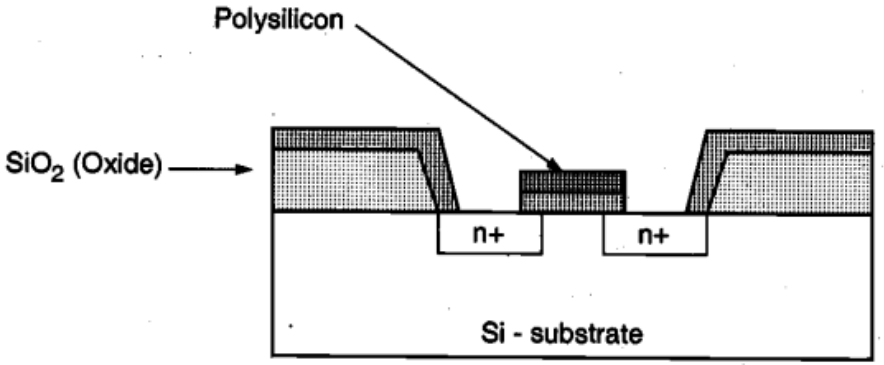


(f)

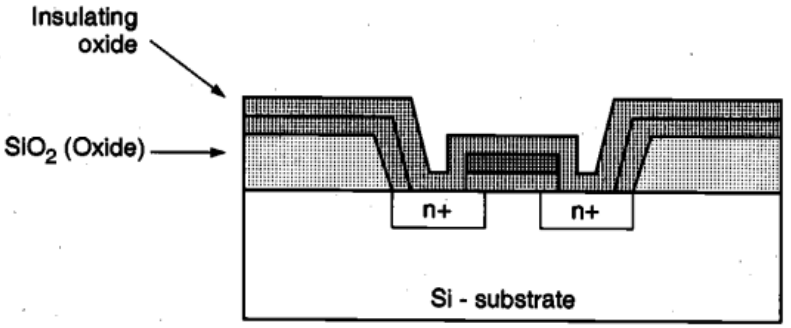


(g)

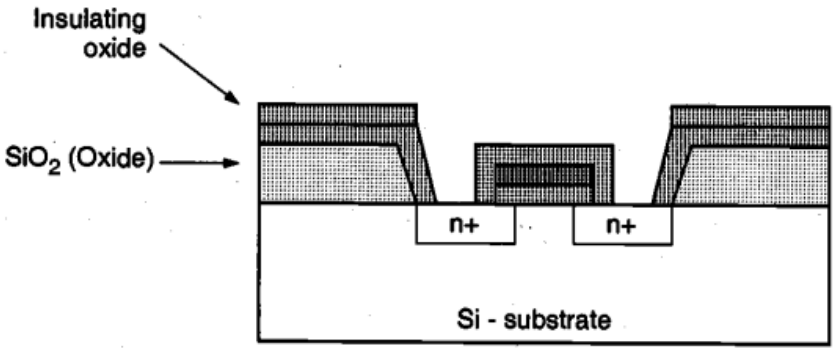
Fabrication of the nMOS Transistor



(h)

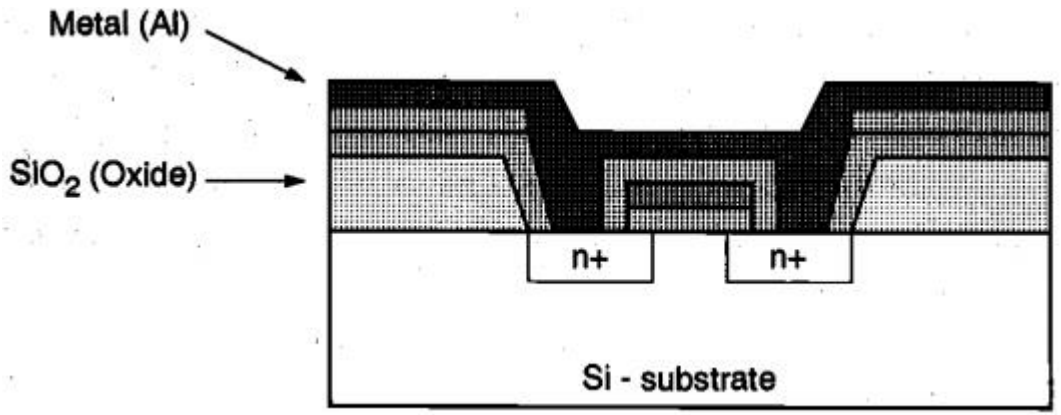


(i)

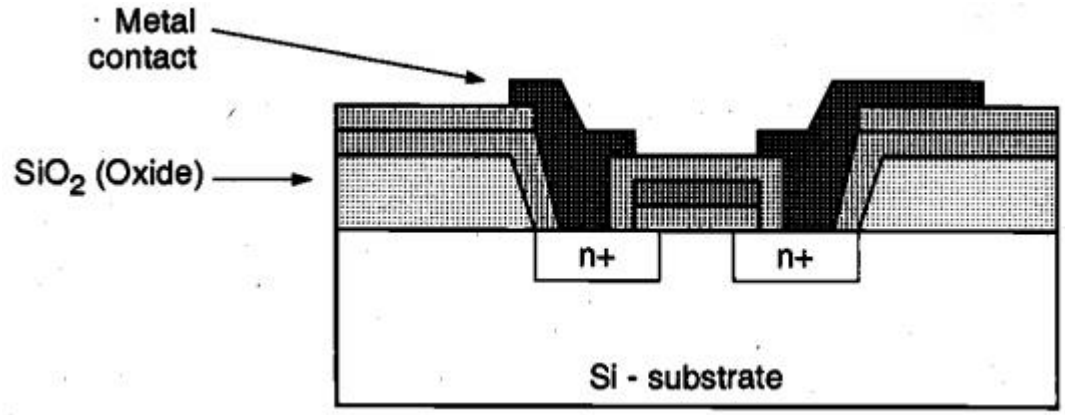


(j)

Fabrication of the nMOS Transistor



(k)

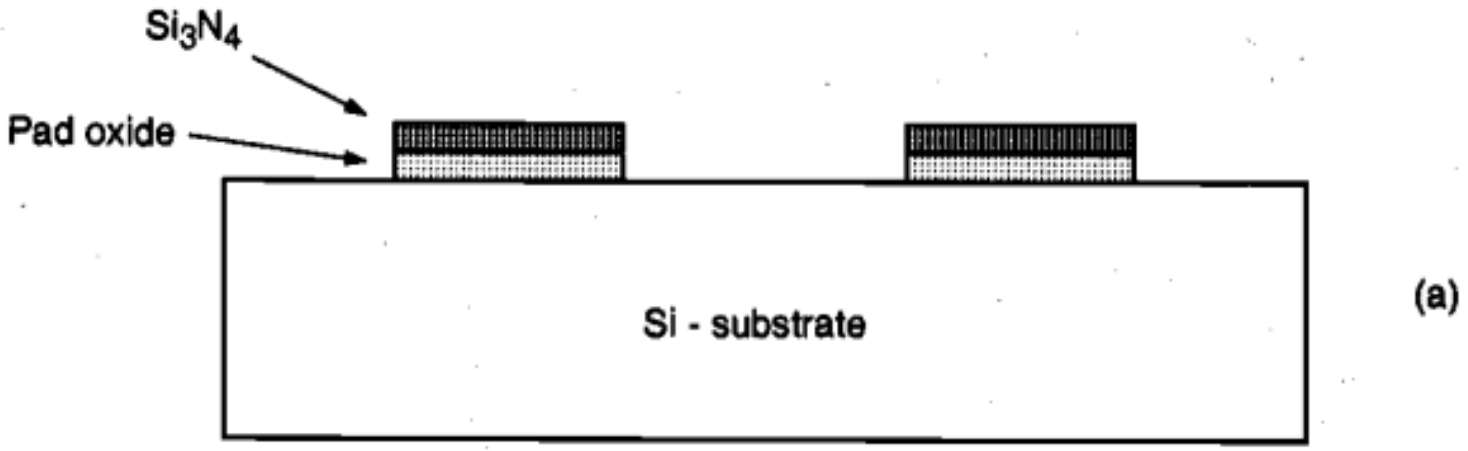


(l)

- The surface is covered with evaporated aluminum which will form the interconnects (Fig. k).
- Finally, the metal layer is patterned and etched, completing the interconnection of the MOS transistors on the surface (Fig. L).

The CMOS n-Well Process

- The n-well CMOS process starts with a moderately doped (with impurity concentration typically less than 10^{15} cm^{-3}) p-type silicon substrate.
- Then, an initial oxide layer is grown on the entire surface.
- The first lithographic mask defines the n-well region.
- Donor atoms, usually phosphorus, are implanted through this window in the oxide.



The CMOS n-Well Process

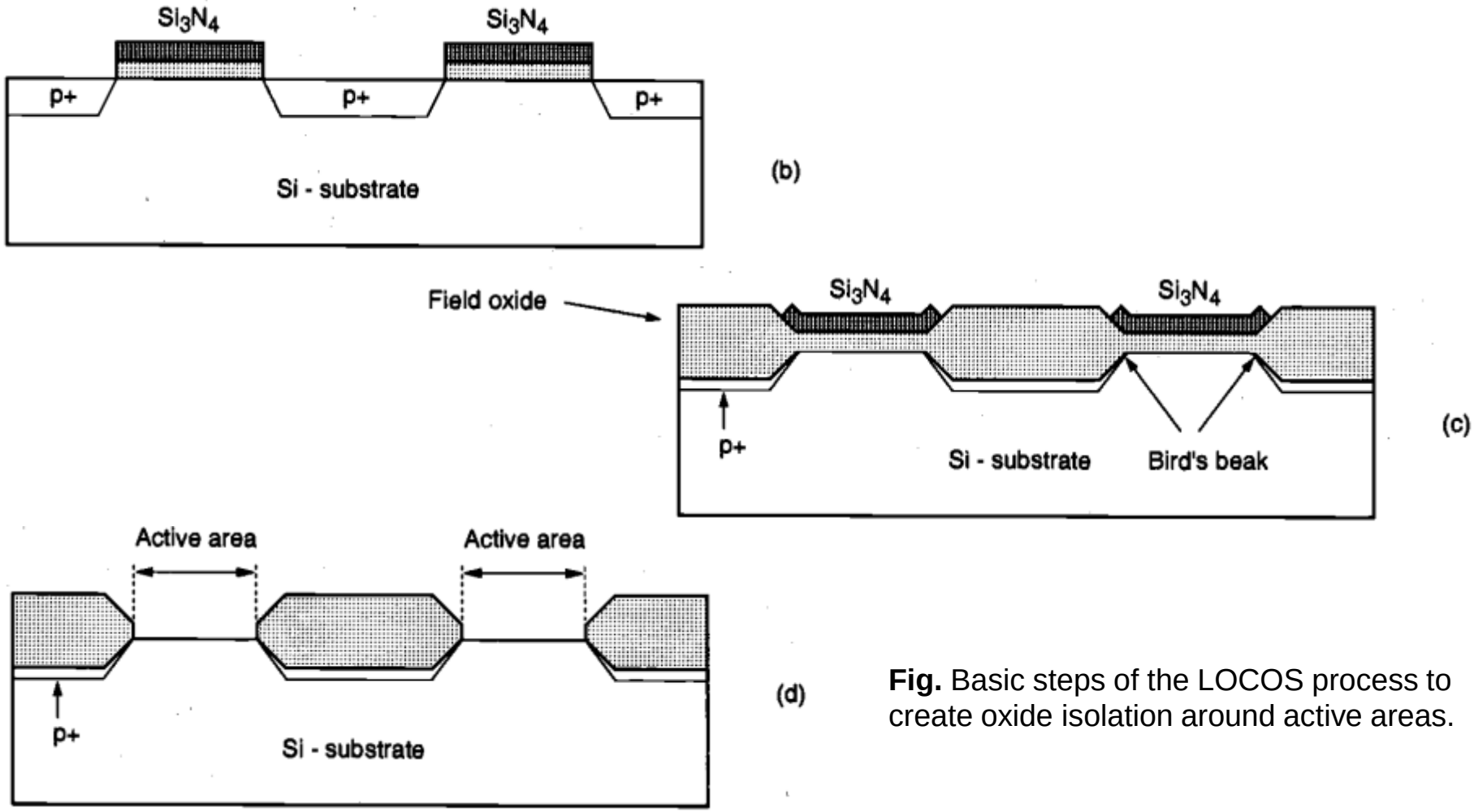


Fig. Basic steps of the LOCOS process to create oxide isolation around active areas.

The CMOS n-Well Process

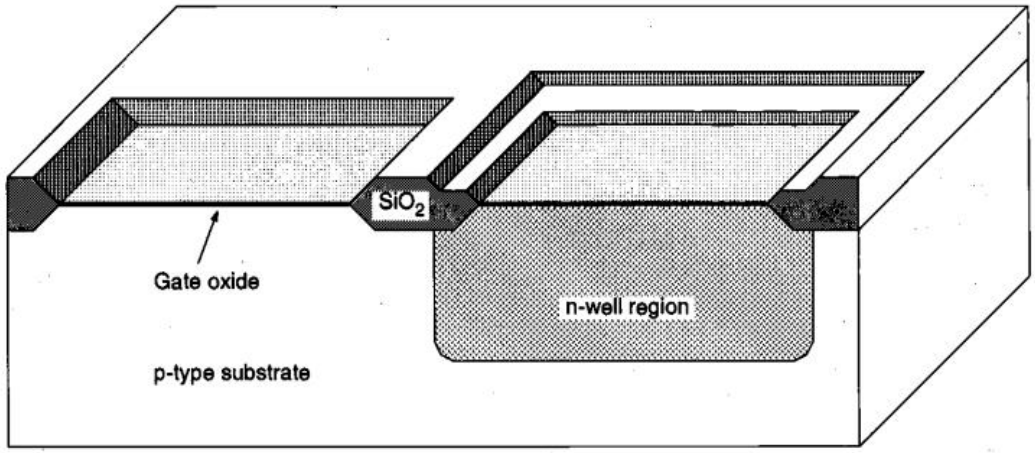


Fig. The creation of the n-well region, a thick field oxide is grown in the areas surrounding the transistor's active regions, and a thin gate oxide is grown on top of the active regions. The thickness and the quality of the gate oxide are two of the most critical fabrication parameters, since they strongly affect the operational characteristics of the MOS transistor, as well as its long-term reliability.

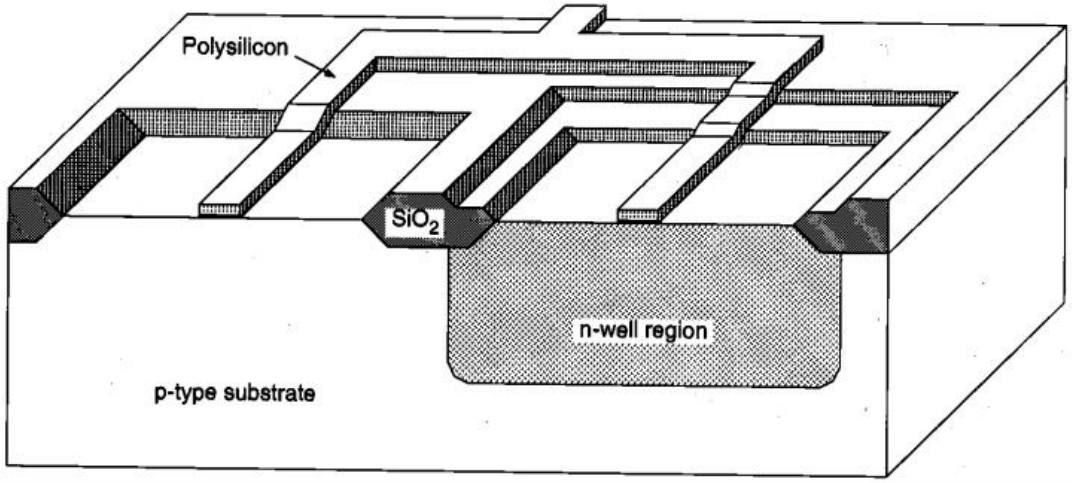


Fig. The polysilicon layer is deposited using chemical vapor deposition (CVD) and patterned by dry (plasma) etching. The created polysilicon lines will function as the gate electrodes of the nMOS and the pMOS transistors and their interconnects.

The CMOS n-Well Process

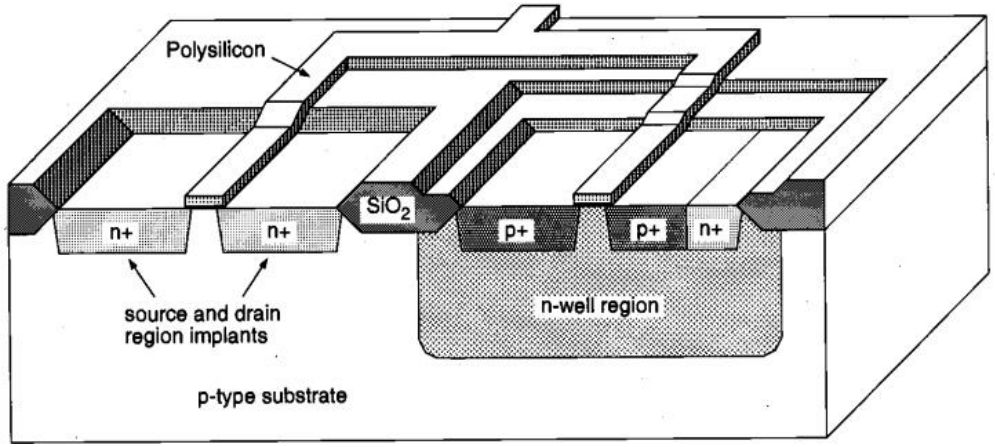


Fig. Using a set of two masks, the n+ and p+ regions are implanted into the substrate and into the n-well, respectively. Also, the ohmic contacts to the substrate and to the n-well are implanted in this process step.

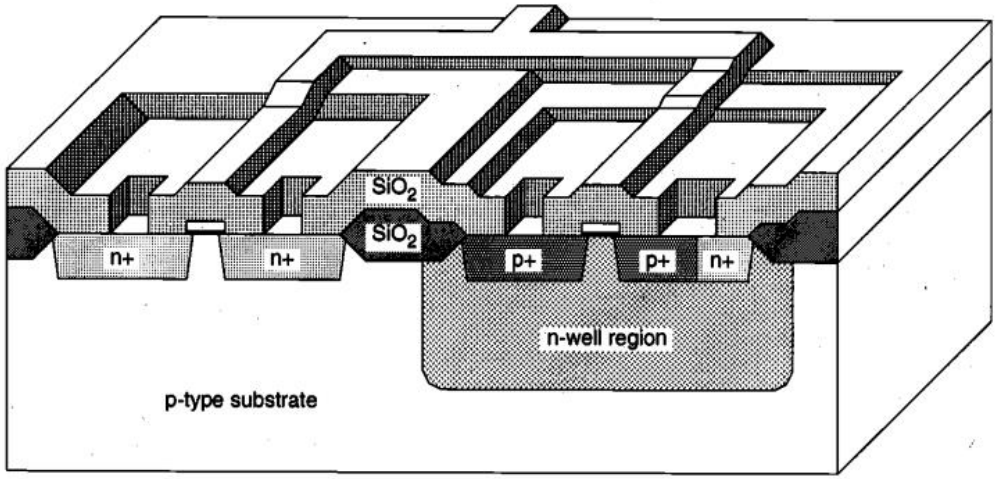


Fig. An insulating silicon dioxide layer is deposited over the entire wafer using CVD. Then, the contacts are defined and etched away to expose the silicon or polysilicon contact windows. These contact windows are necessary to complete the circuit interconnections using the metal layer, which is patterned in the next step.

The CMOS n-Well Process

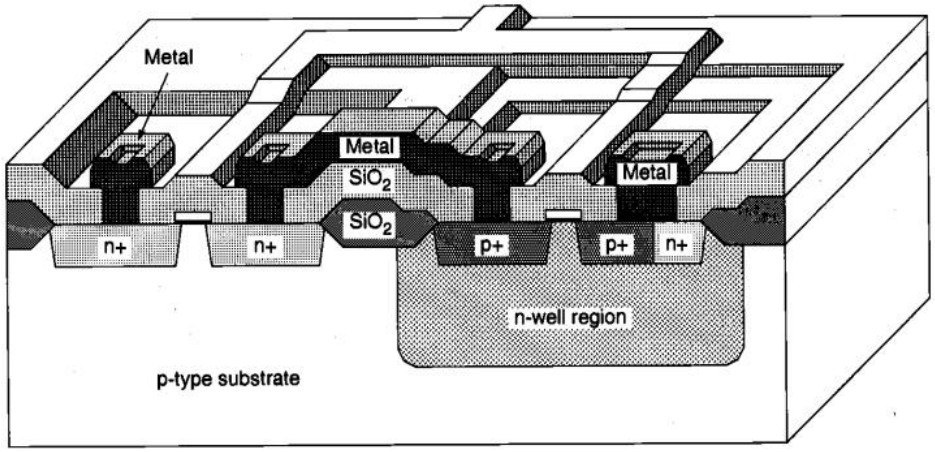


Fig. Metal (aluminum) is deposited over the entire chip surface using metal evaporation, and the metal lines are patterned through etching. Since the wafer surface is non-planar, the quality and the integrity of the metal lines created in this step are very critical and are ultimately essential for circuit reliability.

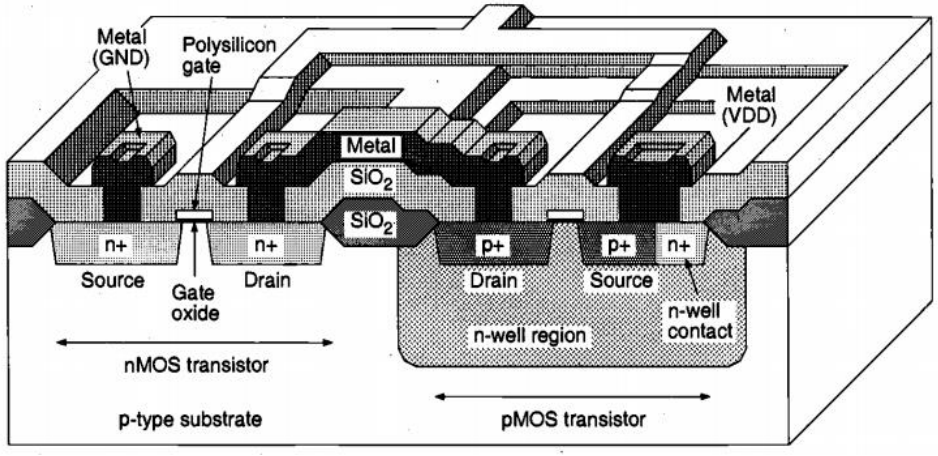


Fig. The composite layout and the resulting cross-sectional view of the chip, showing one nMOS and one pMOS transistor (in the n-well), and the polysilicon and metal interconnections. The final step is to deposit the passivation layer (for protection) over the chip, except over wire-bonding pad areas.