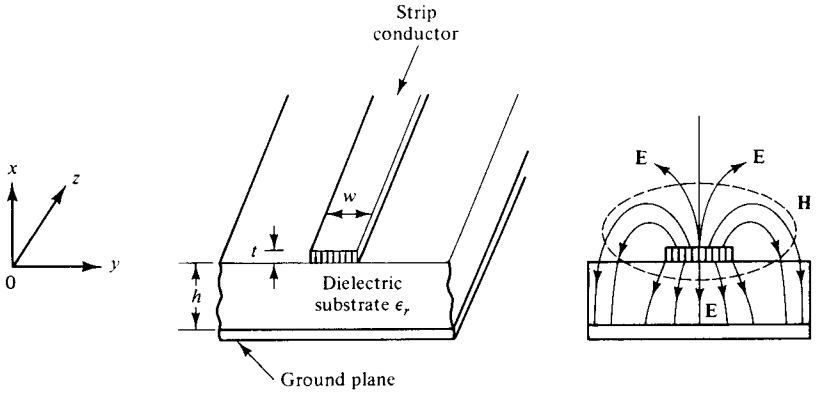
Chapter 11

Strip Lines

11-0 INTRODUCTION

Prior to 1965 nearly all microwave equipment utilized coaxial, waveguide, or parallel strip-line circuits. In recent years—with the introduction of monolithic microwave integrated circuits (MMICs)—microstrip lines and coplanar strip lines have been used extensively, because they provide one free and accessible surface on which solid-state devices can be placed. In this chapter parallel, coplanar, and shielded strip lines and microstrip lines, which are shown in Fig. 11-0-1 [1], are described.



(a) Schematic diagram (b) Field lines

Figure 11-0-1 Schematic diagrams of strip lines.

11-1 MICROSTRIP LINES

Chapter 3 described and discussed conventional transmission lines in detail. All electrical and electronic devices with high-power output commonly use conventional lines, such as coaxial lines or waveguides, for power transmission. However, the microwave solid-state device is usually fabricated as a semiconducting chip with a volume on the order of 0.008–0.08 mm^3. The method of applying signals to the chips and extracting output power from them is entirely different from that used for vacuum-tube devices. Microwave integrated circuits with microstrip lines are commonly used with the chips.The microstrip line is also called an *open-strip line*. In engineering applications, MKS units have not been universally adopted for use in designing the microstrip line. In this section we use either English units or MKS units, depending on the application, for practical purposes.

Modes on microstrip line are only quasi-transverse electric and magnetic (TEM). Thus the theory of TEM-coupled lines applies only approximately. Radiation loss in microstrip lines is a problem, particularly at such discontinuities as short-circuit posts, corners, and so on. However, the use of thin, high-dielectric materials considerably reduces the radiation loss of the open strip. A microstrip line has an advantage over the balanced-strip line because the open strip has better interconnection features and easier fabrication. Several researchers have analyzed the circuit of a microstrip line mounted on an infinite dielectric substrate over an infinite ground plane [2 to 5]. Numerical analysis of microstrip lines, however, requires large digital computers, whereas microstrip-line problems can generally be solved by conformal transformations without requiring complete numerical calculations.

11-1-1 Characteristic Impedance of Microstrip Lines

Microstrip lines are used extensively to interconnect high-speed logic circuits in digital computers because they can be fabricated by automated techniques and they provide the required uniform signal paths. Figure 11-1-1 shows cross sections of a microstrip line and a wire-over-ground line for purposes of comparison.

In Fig. 11-1-1(a) you can see that the characteristic impedance of a microstrip

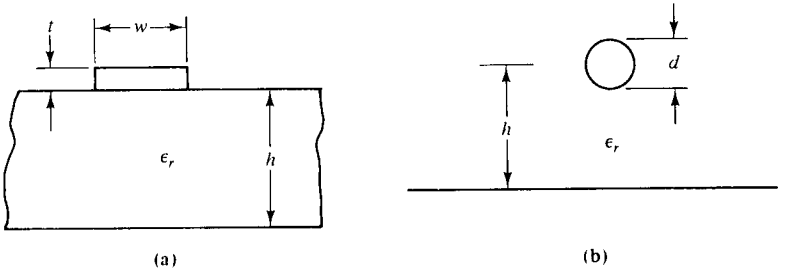


Figure 11-1-1 Cross sections of (a) a microstrip line and (b) a wire-over-ground line.

line is a function of the strip-line width, the strip-line thickness, the distance between the line and the ground plane, and the homogeneous dielectric constant of the board material. Several different methods for determining the characteristic impedance of a microstrip line have been developed. The field-equation method was employed by several authors for calculating an accurate value of the characteristic impedance [3 to 5]. However, it requires the use of a large digital computer and is extremely complicated. Another method is to derive the characteristic-impedance equation of a microstrip line from a well-known equation and make some changes [2]. This method is called a *comparative,* or an *indirect,* method. The well-known equation of the characteristic impedance of a wire-over-ground transmission line, as shown in Fig. 11-1-1(b), is given by

$$Z_0 = \frac{60}{\sqrt{\epsilon_r}} \ln \frac{4h}{d} \qquad \text{for } h \gg d \tag{11-1-1}$$

where ϵ_r = dielectric constant of the ambient medium
h = the height from the center of the wire to the ground plane
d = diameter of the wire

If the effective or equivalent values of the relative dielectric constant ϵ_r of the ambient medium and the diameter d of the wire can be determined for the microstrip line, the characteristic impedance of the microstrip line can be calculated.

Effective dielectric constant ϵ_{re}. For a homogeneous dielectric medium, the propagation-delay time per unit length is

$$T_d = \sqrt{\mu\epsilon} \tag{11-1-2}$$

where μ is the permeability of the medium and ϵ is the permittivity of the medium. In free space, the propagation-delay time is

$$T_{df} = \sqrt{\mu_0\epsilon_0} = 3.333 \quad \text{ns/m} \quad \text{or} \quad 1.016 \quad \text{ns/ft} \tag{11-1-3}$$

where

$$\mu_0 = 4\pi \times 10^{-7} \text{ H/m, or } 3.83 \times 10^{-7} \text{ H/ft}$$
$$\epsilon_0 = 8.854 \times 10^{-12} \text{ F/m, or } 2.69 \times 10^{-12} \text{ F/ft}$$

In transmission lines used for interconnections, the relative permeability is 1. Consequently, the propagation-delay time for a line in a nonmagnetic medium is

$$T_d = 1.106\sqrt{\epsilon_r} \qquad \text{ns/ft} \tag{11-1-4}$$

The effective relative dielectric constant for a microstrip line can be related to the relative dielectric constant of the board material. DiGiacomo and his coworkers discovered an empirical equation for the effective relative dielectric constant of a microstrip line by measuring the propagation-delay time and the relative dielectric constant of several board materials, such as fiberglass-epoxy and nylon phenolic [6].

The empirical equation, as shown in Fig. 11-1-2, is expressed as

$$\epsilon_{re} = 0.475\epsilon_r + 0.67 \tag{11-1-5}$$

where ϵ_r is the relative dielectric constant of the board material and ϵ_{re} is the effective relative dielectric constant for a microstrip line.

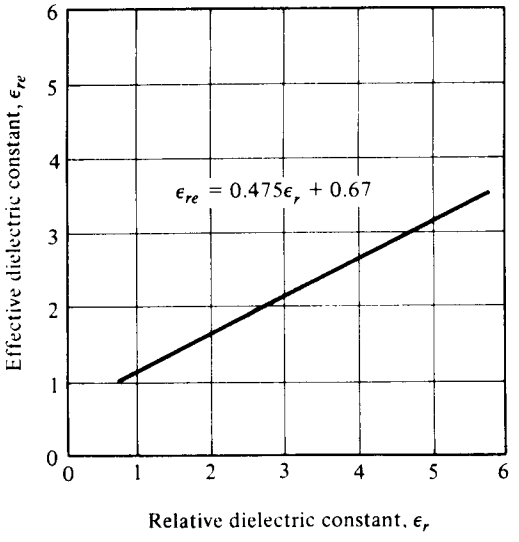


Figure 11-1-2 Effective dielectric constant as a function of relative dielectric constant for a microstrip line. (*After H. R., Kaupp [2]; reprinted by permission of IEEE, Inc.*)

Transformation of a rectangular conductor into an equivalent circular conductor. The cross-section of a microstrip line is rectangular, so the rectangular conductor must be transformed into an equivalent circular conductor. Springfield discovered an empirical equation for the transformation [7]. His equation is

$$d = 0.67w\left(0.8 + \frac{t}{w}\right) \tag{11-1-6}$$

where d = diameter of the wire over ground
w = width of the microstrip line
t = thickness of the microstrip line

The limitation of the ratio of thickness to width is between 0.1 and 0.8, as indicated in Fig. 11-1-3.

Characteristic impedance equation. Substituting Eq. (11-1-5) for the dielectric constant and Eq. (11-1-6) for the equivalent diameter in Eq. (11-1-1) yields

$$Z_0 = \frac{87}{\sqrt{\epsilon_r + 1.41}} \ln\left[\frac{5.98h}{0.8w + t}\right] \qquad \text{for } (h < 0.8w) \tag{11-1-7}$$

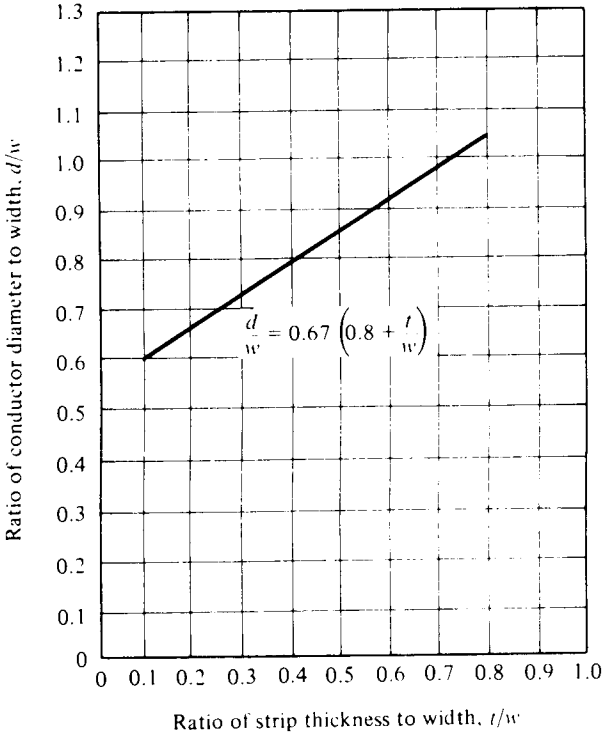


Figure 11-1-13 Relationship between a round conductor and a rectangular conductor far from its ground plane. (*After H. R. Kaupp [2]; reprinted by permission of IEEE, Inc.*)

where ϵ_r = relative dielectric constant of the board material
h = height from the microstrip line to the ground
w = width of the microstrip line
t = thickness of the microstrip line

Equation (11-1-7) is the equation of characteristic impedance for a narrow microstrip line. The velocity of propagation is

$$v = \frac{c}{\sqrt{\epsilon_{re}}} = \frac{3 \times 10^8}{\sqrt{\epsilon_{re}}} \quad \text{m/s} \tag{11-1-8}$$

The characteristic impedance for a wide microstrip line was derived by Assadourian and others [8] and is expressed by

$$Z_0 = \frac{h}{w}\sqrt{\frac{\mu}{\epsilon}} = \frac{377}{\sqrt{\epsilon_r}}\frac{h}{w} \quad \text{for } (w \gg h) \tag{11-1-9}$$

Limitations of Equation (11-1-7). Most microstrip lines are made from boards of copper with a thickness of 1.4 or 2.8 mils (1 or 2 ounces of copper per square foot). The narrowest widths of lines in production are about 0.005–0.010 in. Line widths are usually less than 0.020 in.; consequently, ratios of thickness to width of less than 0.1 are uncommon. The straight-line approximation from Eq. (11-1-6) is an accurate value of characteristic impedance, or the ratio of thickness to width between 0.1 and 0.8.

Since the dielectric constant of the materials used does not vary excessively with frequency, the dielectric constant of a microstrip line can be considered independent of frequency. The validity of Eq. (11-1-7) is doubtful for values of dielectric thickness h that are greater than 80% of the line width w. Typical values for the characteristic impedance of a microstrip line vary from 50 Ω to 150 Ω, if the values of the parameters vary from $\epsilon_r = 5.23$, $t = 2.8$ mils, $w = 10$ mils, and $h = 8$ mils to $\epsilon_r = 2.9$, $t = 2.8$ mils, $w = 10$ mils, and $h = 67$ mils [2].

Example 11-1-1: Characteristic Impedance of Microstrip Line

A certain microstrip line has the following parameters:

$$\epsilon_r = 5.23$$
$$h = 7 \text{ mils}$$
$$t = 2.8 \text{ mils}$$
$$w = 10 \text{ mils}$$

Calculate the characteristic impedance Z_0 of the line.

Solution

$$Z_0 = \frac{87}{\sqrt{\epsilon_r + 1.41}} \ln\left[\frac{5.98h}{0.8w + t}\right]$$

$$= \frac{87}{\sqrt{5.23 + 1.41}} \ln\left[\frac{5.98 \times 7}{0.8 \times 10 + 2.8}\right]$$

$$= 45.78\ \Omega$$

11-1-2 Losses in Microstrip Lines

Microstrip transmission lines consisting of a conductive ribbon attached to a dielectric sheet with conductive backing (see Fig. 11-1-4) are widely used in both microwave and computer technology. Because such lines are easily fabricated by printed-circuit manufacturing techniques, they have economic and technical merit.

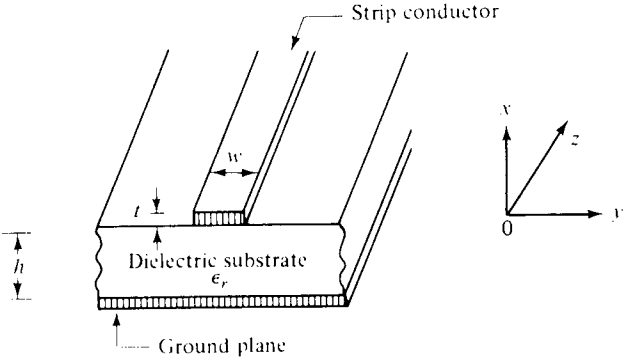


Figure 11-1-4 Schematic diagram of a microstrip line.

The characteristic impedance and wave-propagation velocity of a microstrip line was analyzed in Section 11-1-1. The other characteristic of the microstrip line is its attenuation. The attenuation constant of the dominant microstrip mode depends on geometric factors, electrical properties of the substrate and conductors, and on the frequency. For a nonmagnetic dielectric substrate, two types of losses occur in the dominant microstrip mode: (1) dielectric loss in the substrate and (2) ohmic skin loss in the strip conductor and the ground plane. The sum of these two losses may be expressed as losses per unit length in terms of an attenuation factor α. From ordinary transmission-line theory, the power carried by a wave traveling in the positive z direction is given by

$$P = \tfrac{1}{2} VI^* = \tfrac{1}{2}(V_+ e^{-\alpha z} I_+ e^{-\alpha z}) = \tfrac{1}{2}\frac{|V_+|^2}{Z_0} e^{-2\alpha z} = P_0 e^{-2\alpha z} \qquad (11\text{-}1\text{-}10)$$

where $P_0 = |V_+|^2/(2Z_0)$ is the power at $z = 0$.

The attenuation constant α can be expressed as

$$\alpha = -\frac{dP/dz}{2P(z)} = \alpha_d + \alpha_c \qquad (11\text{-}1\text{-}11)$$

where α_d is the dielectric attenuation constant and α_c is the ohmic attenuation constant.

The gradient of power in the z direction in Eq. (11-1-11) can be further expressed in terms of the power loss per unit length dissipated by the resistance and the power loss per unit length in the dielectric. That is,

$$\begin{aligned} -\frac{dP(z)}{dz} &= -\frac{d}{dz}(\tfrac{1}{2} VI^*) \\ &= \tfrac{1}{2}\left(-\frac{dV}{dz}\right) I^* + \tfrac{1}{2}\left(-\frac{dI^*}{dz}\right) V \\ &= \tfrac{1}{2}(RI) I^* + \tfrac{1}{2}\sigma V^* V \\ &= \tfrac{1}{2}|I|^2 R + \tfrac{1}{2}|V|^2 \sigma = P_c + P_d \end{aligned} \qquad (11\text{-}1\text{-}12)$$

where σ is the conductivity of the dielectric substrate board.

Substitution of Eq. (11-1-12) into Eq. (11-1-11) results in

$$\alpha_d \simeq \frac{P_d}{2P(z)} \qquad \text{Np/cm} \qquad (11\text{-}1\text{-}13)$$

and

$$\alpha_c \simeq \frac{P_c}{2P(z)} \qquad \text{Np/cm} \qquad (11\text{-}1\text{-}14)$$

Dielectric losses. As stated in Section 2-5-3, when the conductivity of a dielectric cannot be neglected, the electric and magnetic fields in the dielectric are no longer in time phase. In that case the dielectric attenuation constant, as expressed in Eq. (2-5-20), is given by

$$\alpha_d = \frac{\sigma}{2}\sqrt{\frac{\mu}{\epsilon}} \qquad \text{Np/cm} \tag{11-1-15}$$

where σ is the conductivity of the dielectric substrate board in $\mho$/cm. This dielectric constant can be expressed in terms of dielectric loss tangent as shown in Eq. (2-5-17):

$$\tan\theta = \frac{\sigma}{\omega\epsilon} \tag{11-1-16}$$

Then the dielectric attenuation constant is expressed by

$$\alpha_d = \frac{\omega}{2}\sqrt{\mu\epsilon}\tan\theta \qquad \text{Np/cm} \tag{11-1-17}$$

Since the microstrip line is a nonmagnetic mixed dielectric system, the upper dielectric above the microstrip ribbon is air, in which no loss occurs. Welch and Pratt [9] derived an expression for the attenuation constant of a dielectric substrate. Later on, Pucel and his coworkers [10] modified Welch's equation [9]. The result is

$$\begin{aligned}\alpha_d &= 4.34\frac{q\sigma}{\sqrt{\epsilon_{re}}}\sqrt{\frac{\mu_0}{\epsilon_0}} \\ &= 1.634 \times 10^3 \frac{q\sigma}{\sqrt{\epsilon_{re}}} \qquad \text{dB/cm}\end{aligned} \tag{11-1-18}$$

In Eq. (11-1-18) the conversion factor of 1 Np = 8.686 dB is used, ϵ_{re} is the effective dielectric constant of the substrate, as expressed in Eq. (11-1-5), and q denotes the dielectric filling factor, defined by Wheeler [3] as

$$q = \frac{\epsilon_{re} - 1}{\epsilon_r - 1} \tag{11-1-19}$$

We usually express the attenuation constant per wavelength as

$$\alpha_d = 27.3\left(\frac{q\epsilon_r}{\epsilon_{re}}\right)\frac{\tan\theta}{\lambda_g} \qquad \text{dB}/\lambda_g \tag{11-1-20}$$

where $\lambda_g = \dfrac{\lambda_0}{\sqrt{\epsilon_{re}}}$ and λ_0 is the wavelength in free space, or

$\lambda_g = \dfrac{c}{f\sqrt{\epsilon_{re}}}$ and c is the velocity of light in vacuum.

If the loss tangent, $\tan\theta$, is independent of frequency, the dielectric attenuation per wavelength is also independent of frequency. Moreover, if the substrate conductivity is independent of frequency, as for a semiconductor, the dielectric attenuation per unit is also independent of frequency. Since q is a function of ϵ_r and w/h, the filling factors for the loss tangent $q\epsilon_n/\epsilon_{re}$ and for the conductivity $q/\sqrt{\epsilon_{re}}$ are also functions of these quantities. Figure 11-1-5 shows the loss-tangent filling factor against w/h for a range of dielectric constants suitable for microwave inte-

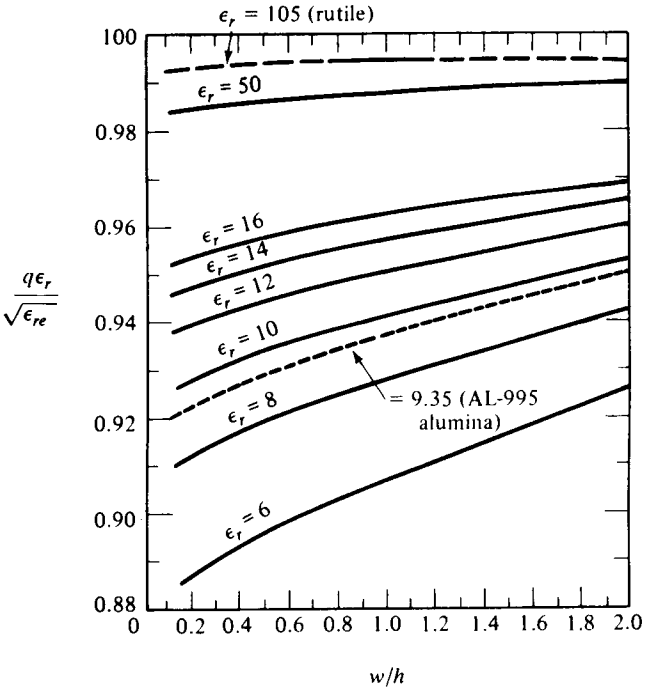


Figure 11-1-5 Filling factor for loss tangent of microstrip substrate as a function of w/h. (*After R. A. Pucel et al. [10]; reprinted by permission of IEEE, Inc.*)

grated circuits. For most practical purposes, this factor is considered to be 1. Figure 11-1-6 illustrates the product $\alpha_d \rho$ against w/h for two semiconducting substrates, silicon and gallium arsenide, that are used for integrated microwave circuits. For design purposes, the conductivity filling factor, which exhibits only a mild dependence on w/h, can be ignored.

Ohmic losses. In a microstrip line over a low-loss dielectric substrate, the predominant sources of losses at microwave frequencies are the nonperfect conductors. The current density in the conductors of a microstrip line is concentrated in a sheet that is approximately a skin depth thick inside the conductor surface and exposed to the electric field. Both the strip conductor thickness and the ground plane thickness are assumed to be at least three or four skin depths thick. The current density in the strip conductor and the ground conductor is not uniform in the transverse plane. The microstrip conductor contributes the major part of the ohmic loss. A diagram of the current density J for a microstrip line is shown in Fig. 11-1-7.

Because of mathematical complexity, exact expressions for the current density of a microstrip line with nonzero thickness have never been derived [10]. Several researchers [8] have assumed, for simplicity, that the current distribution is uniform and equal to I/w in both conductors and confined to the region $|x| < w/2$. With this assumption, the conducting attenuation constant of a wide microstrip line is given by

$$\alpha_c \simeq \frac{8.686 R_s}{Z_0 w} \quad \text{dB/cm} \quad \text{for } \frac{w}{h} > 1 \tag{11-1-21}$$

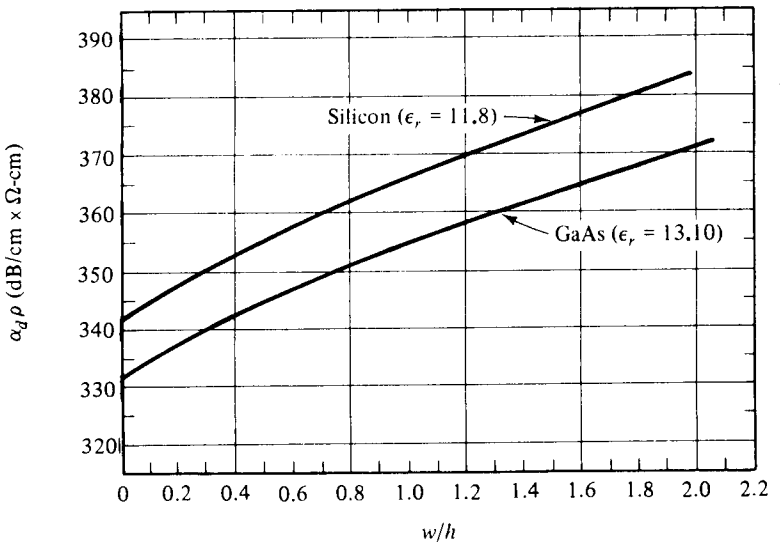


Figure 11-1-6 Dielectric attenuation factor of microstrip as a function of w/h for silicon and gallium arsenide substrates. (*After R. A. Pucel et al. [10]; reprinted by permission of IEEE, Inc.*)

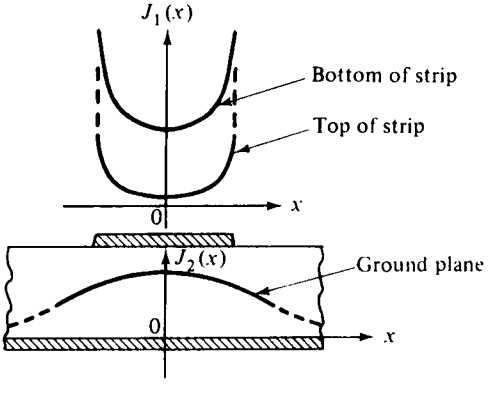


Figure 11-1-7 Current distribution on microstrip conductors. (*After R. A. Pucel et al. [10]; reprinted by permission of IEEE, Inc.*)

where $R_s = \sqrt{\dfrac{\pi f \mu}{\sigma}}$ is the surface skin resistance in Ω/square,

$$R_s = \frac{1}{\delta \sigma} \text{ is } \Omega/\text{square}$$

$$\delta = \sqrt{\frac{1}{\pi f \mu \sigma}} \text{ is the skin depth in cm}$$

For a narrow microstrip line with $w/h < 1$, however, Eq. (11-1-21) is not applicable. The reason is that the current distribution in the conductor is not uniform, as assumed. Pucel and his coworkers [10, 11] derived the following three formulas from the results of Wheeler's work [3]:

$$\frac{\alpha_c Z_0 h}{R_s} = \frac{8.68}{2\pi}\left[1 - \left(\frac{w'}{4h}\right)^2\right]\left[1 + \frac{h}{w'} + \frac{h}{\pi w'}\left(\ln\frac{4\pi w}{t} + \frac{t}{w}\right)\right]$$

$$\text{for } \frac{w}{h} \leq \frac{1}{2\pi} \quad (11\text{-}1\text{-}22)$$

$$\frac{\alpha_c Z_0 h}{R_s} = \frac{8.68}{2\pi}\left[1 - \left(\frac{w'}{4h}\right)^2\right]\left[1 + \frac{h}{w'} + \frac{h}{w'}\left(\ln\frac{2h}{t} - \frac{t}{h}\right)\right]$$

$$\text{for } \frac{1}{2\pi} < \frac{w}{h} \leq 2 \quad (11\text{-}1\text{-}23)$$

and

$$\frac{\alpha_c Z_0 h}{R_s} = \frac{8.68}{\left\{\frac{w'}{h} + \frac{2}{\pi}\ln\left[2\pi e\left(\frac{w'}{2h} + 0.94\right)\right]\right\}^2}\left[\frac{w'}{h} + \frac{w'/(\pi h)}{\frac{w'}{2h} + 0.94}\right] \times \left[1 + \frac{h}{w'} + \frac{h}{\pi w'}\left(\ln\frac{2h}{t} - \frac{t}{h}\right)\right] \quad \text{for } 2 \leq \frac{w}{h} \quad (11\text{-}1\text{-}24)$$

where α_c is expressed in dB/cm and

$$e = 2.718$$

$$w' = w + \Delta w \quad (11\text{-}1\text{-}25)$$

$$\Delta w = \frac{t}{\pi}\left(\ln\frac{4\pi w}{t} + 1\right) \quad \text{for } \frac{2t}{h} < \frac{w}{h} \leq \frac{\pi}{2} \quad (11\text{-}1\text{-}26)$$

$$\Delta w = \frac{t}{\pi}\left(\ln\frac{2h}{t} + 1\right) \quad \text{for } \frac{w}{h} \geq \frac{\pi}{2} \quad (11\text{-}1\text{-}27)$$

The values of α_c obtained from solving Eqs. (11-1-22) through (11-1-24) are plotted in Fig. 11-1-8. For purposes of comparison, values of α_c based on Assadourian and Rimai's Eq. (11-1-21) are also shown.

Radiation losses. In addition to the conductor and dielectric losses, microstrip line also has radiation losses. The radiation loss depends on the substrate's thickness and dielectric constant, as well as its geometry. Lewin [12] has calculated the radiation loss for several discontinuities using the following approximations:

1. TEM transmission
2. Uniform dielectric in the neighborhood of the strip, equal in magnitude to an effective value
3. Neglect of radiation from the transverse electric (TE) field component parallel to the strip
4. Substrate thickness much less than the free-space wavelength

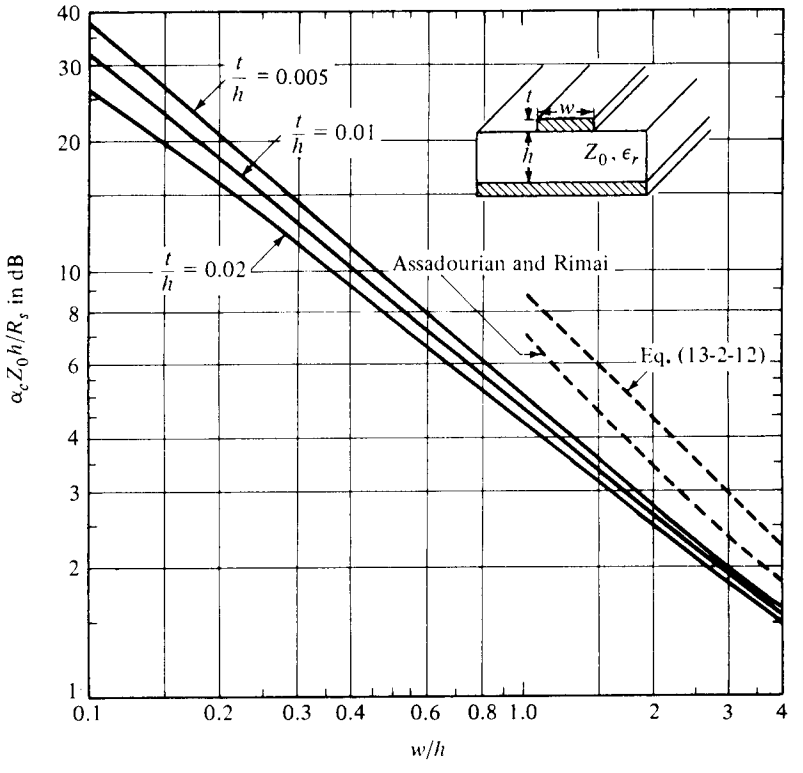


Figure 11-1-8 Theoretical conductor attenuation factor of microstrip as a function of w/h. (*After R. A. Pucel et al. [10]; reprinted by permission of IEEE, Inc.*)

Lewin's results show that the ratio of radiated power to total dissipated power for an open-circuited microstrip line is

$$\frac{P_{\text{rad}}}{P_t} = 240\pi^2 \left(\frac{h}{\lambda_0}\right)^2 \frac{F(\epsilon_{re})}{Z_0} \tag{11-1-28}$$

where $F(\epsilon_{re})$ is a radiation factor given by

$$F(\epsilon_{re}) = \frac{\epsilon_{re} + 1}{\epsilon_{re}} - \frac{\epsilon_{re} - 1}{2\epsilon_{re}\sqrt{\epsilon_{re}}} \ln \frac{\sqrt{\epsilon_{re}} + 1}{\sqrt{\epsilon_{re}} - 1} \tag{11-1-29}$$

in which ϵ_{re} is the effective dielectric constant and $\lambda_0 = c/f$ is the free-space wavelength.

The radiation factor decreases with increasing substrate dielectric constant. So, alternatively, Eq. (11-1-28) can be expressed as

$$\frac{P_{\text{rad}}}{P_t} = \frac{R_r}{Z_0} \tag{11-1-30}$$

where R_r is the radiation resistance of an open-circuited microstrip and is given by

$$R_r = 240\pi^2 \left(\frac{h}{\lambda_0}\right)^2 F(\epsilon_{re}) \tag{11-1-31}$$

The ratio of the radiation resistance R_r to the real part of the characteristic impedance Z_0 of the microstrip line is equal to a small fraction of the power radiated from a single open-circuit discontinuity. In view of Eq. (11-1-28), the radiation loss decreases when the characteristic impedance increases. For lower dielectric-constant substrates, radiation is significant at higher impedance levels. For higher dielectric-constant substrates, radiation becomes significant until very low impedance levels are reached.

11-1-3 Quality Factor Q of Microstrip Lines

Many microwave integrated circuits require very high quality resonant circuits. The quality factor Q of a microstrip line is very high, but it is limited by the radiation losses of the substrates and with low dielectric constant. Recall that for uniform current distribution in the microstrip line, the ohmic attenuation constant of a wide microstrip line is given by Eq. (11-1-21) as

$$\alpha_c = \frac{8.686 R_s}{Z_0 w} \qquad \text{dB/cm}$$

and that the characteristic impedance of a wide microstrip line, as shown in Eq. (11-1-9), is

$$Z_0 = \frac{h}{w}\sqrt{\frac{\mu}{\epsilon}} = \frac{377}{\sqrt{\epsilon_r}}\frac{h}{w} \qquad \Omega$$

The wavelength in the microstrip line is

$$\lambda_g = \frac{30}{f\sqrt{\epsilon_r}} \qquad \text{cm} \tag{11-1-32}$$

where f is the frequency in GHz.

Since Q_c is related to the conductor attenuation constant by

$$Q_c = \frac{27.3}{\alpha_c} \tag{11-1-33}$$

where α_c is in dB/λ_g, Q_c of a wide microstrip line is expressed as

$$Q_c = 39.5\left(\frac{h}{R_s}\right) f_{\text{GHz}} \tag{11-1-34}$$

where h is measured in cm and R_s is expressed as

$$R_s = \sqrt{\frac{\pi f \mu}{\sigma}} = 2\pi\sqrt{\frac{f_{\text{GHz}}}{\sigma}} \qquad \Omega/\text{square.} \tag{11-1-35}$$

Finally, the quality factor Q_c of a wide microstrip line is

$$Q_c = 0.63h\sqrt{\sigma f_{\text{GHz}}} \tag{11-1-36}$$

where α is the conductivity of the dielectric substrate board in $\mho/\text{m}$.

For a copper strip, $\alpha = 5.8 \times 10^7\ \mho/\text{m}$ and Q_c becomes

$$Q_{\text{Cu}} = 4780h\sqrt{f_{\text{GHz}}} \tag{11-1-37}$$

For 25-mil alumina at 10 GHz, the maximum Q_c achievable from wide microstrip lines is 954 [13].

Similarly, a quality factor Q_d is related to the dielectric attenuation constant:

$$Q_d = \frac{27.3}{\alpha_d} \tag{11-1-38}$$

where α_d is in dB/λ_g.

Substituting Eq. (11-1-20) into Eq. (11-1-38) yields

$$Q_d = \frac{\lambda_0}{\sqrt{\epsilon_{re}}\tan\theta} \simeq \frac{1}{\tan\theta} \tag{11-1-39}$$

where λ_0 is the free-space wavelength in cm. Note that the Q_d for the dielectric attenuation constant of a microstrip line is approximately the reciprocal of the dielectric loss tangent θ and is relatively constant with frequency.

11-2 PARALLEL STRIP LINES

A parallel strip line consists of two perfectly parallel strips separated by a perfect dielectric slab of uniform thickness, as shown in Fig. 11-2-1. The plate width is w, the separation distance is d, and the relative dielectric constant of the slab is ϵ_{rd}.

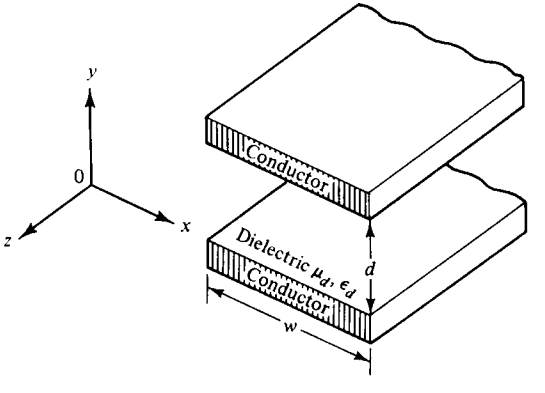


Figure 11-2-1 Schematic diagram of a parallel strip line.

11-2-1 Distributed Parameters

In a microwave integrated circuit a strip line can be easily fabricated on a dielectric substrate by using printed-circuit techniques. A parallel stripline is similar to a two-conductor transmission line, so it can support a quasi-TEM mode. Consider a TEM-mode wave propagating in the positive z direction in a lossless strip line ($R = G = 0$). The electric field is in the y direction, and the magnetic field is in the x direction. If the width w is much larger than the separation distance d, the fringing capacitance is negligible. Thus the equation for the inductance along the two conducting strips can be written as

$$L = \frac{\mu_c d}{w} \qquad \text{H/m} \tag{11-2-1}$$

where μ_c is the permeability of the conductor. The capacitance between the two conducting strips can be expressed as

$$C = \frac{\epsilon_d w}{d} \qquad \text{F/m} \tag{11-2-2}$$

where ϵ_d is the permittivity of the dielectric slab.

If the two parallel strips have some surface resistance and the dielectric substrate has some shunt conductance, however, the parallel stripline would have some losses. The series resistance for both strips is given by

$$R = \frac{2R_s}{w} = \frac{2}{w}\sqrt{\frac{\pi f \mu_c}{\sigma_c}} \qquad \Omega/\text{m} \tag{11-2-3}$$

where $R_s = \sqrt{(\pi f \mu_c)/\sigma_c}$ is the conductor surface resistance in Ω/square and σ_c is the conductor conductivity in $\mho$/m. The shunt conductance of the strip line is

$$G = \frac{\sigma_d w}{d} \qquad \mho/\text{m} \tag{11-2-4}$$

where σ_d is the conductivity of the dielectric substrate.

11-2-2 Characteristic Impedance

The characteristic impedance of a lossless parallel strip line is

$$Z_0 = \sqrt{\frac{L}{C}} = \frac{d}{w}\sqrt{\frac{\mu_d}{\epsilon_d}} = \frac{377}{\sqrt{\epsilon_{rd}}}\frac{d}{w} \qquad \text{for } w \gg d \tag{11-2-5}$$

The phase velocity along a parallel strip line is

$$v_p = \frac{\omega}{\beta} = \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{\mu_d \epsilon_d}} = \frac{c}{\sqrt{\epsilon_{rd}}} \qquad \text{m/s} \qquad \text{for } \mu_c = \mu_0 \tag{11-2-6}$$

The characteristic impedance of a lossy parallel strip line at microwave frequencies ($R \ll \omega L$ and $G \ll \omega C$) can be approximated as

$$Z_0 \simeq \sqrt{\frac{L}{C}} = \frac{377}{\sqrt{\epsilon_{rd}}}\frac{d}{w} \qquad \text{for } w \gg d \tag{11-2-7}$$

11-2-3 Attenuation Losses

The propagation constant of a parallel strip line at microwave frequencies can be expressed by

$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)} \qquad \text{for } R \ll \omega L \quad \text{and} \quad G \ll \omega C$$
$$\simeq \frac{1}{2}\left(R\sqrt{\frac{C}{L}} + G\sqrt{\frac{L}{C}}\right) + j\omega\sqrt{LC} \tag{11-2-8}$$

Thus the attenuation and phase constants are

$$\alpha = \frac{1}{2}\left(R\sqrt{\frac{C}{L}} + G\sqrt{\frac{L}{C}}\right) \qquad \text{Np/m} \tag{11-2-9}$$

and

$$\beta = \omega\sqrt{LC} \qquad \text{rad/m} \tag{11-2-10}$$

Substitution of the distributed parameters of a parallel strip line into Eq.(11-2-9) yields the attenuation constants for the conductor and dielectric losses:

$$\alpha_c = \frac{1}{2}R\sqrt{\frac{C}{L}} = \frac{1}{d}\sqrt{\frac{\pi f \epsilon_d}{\sigma_c}} \qquad \text{Np/m} \tag{11-2-11}$$

and

$$\alpha_d = \frac{1}{2}G\sqrt{\frac{L}{C}} = \frac{188\sigma_d}{\sqrt{\epsilon_{rd}}} \qquad \text{Np/m} \tag{11-2-12}$$

Example 11-2-1: Characteristics of a Parallel Strip Line

A lossless parallel strip line has a conducting strip width w. The substrate dielectric separating the two conducting strips has a relative dielectric constant ϵ_{rd} of 6 (beryllia or beryllium oxide BeO) and a thickness d of 4 mm.

Calculate:

a. The required width w of the conducting strip in order to have a characteristic impedance of 50 Ω

b. The strip-line capacitance

c. The strip-line inductance

d. The phase velocity of the wave in the parallel strip line

Solution

a. From Eq. (11-2-5) the width of the conducting strip is

$$w = \frac{377}{\sqrt{\epsilon_{rd}}}\frac{d}{Z_0} = \frac{377}{\sqrt{6}}\frac{4 \times 10^{-3}}{50}$$

$$= 12.31 \times 10^{-3} \text{ m}$$

b. The strip-line capacitance is

$$C = \frac{\epsilon_d w}{d} = \frac{8.854 \times 10^{-12} \times 6 \times 12.31 \times 101^{-3}}{4 \times 10^{-3}}$$

$$= 163.50 \text{ pF/m}$$

c. The strip-line inductance is

$$L = \frac{\mu_c d}{w} = \frac{4\pi \times 10^{-7} \times 4 \times 10^{-3}}{12.31 \times 10^{-3}}$$

$$= 0.41 \ \mu\text{H/m}$$

d. The phase velocity is

$$v_p = \frac{c}{\sqrt{\epsilon_{rd}}} = \frac{3 \times 10^8}{\sqrt{6}}$$

$$= 1.22 \times 10^8 \text{ m/s}$$

11-3 COPLANAR STRIP LINES

A coplanar trip line consists of two conducting strips on one substrate surface with one strip grounded, as shown in Fig. 11-3-1. The coplanar strip line has advantages over the conventional parallel strip line (see Section 11-2) because its two strips are on the same substrate surface for convenient connections. In microwave integrated circuits (MICs) the wire bonds have always presented reliability and reproducibility problems. The coplanar strip lines eliminate the difficulties involved in connecting the shunt elements between the hot and ground strips. As a result, reliability is increased, reproducibility is enhanced, and production cost is decreased.

The characteristic impedance of a coplanar strip line is

$$Z_0 = \frac{2 P_{\text{avg}}}{I_0^2} \tag{11-3-1}$$

where I_0 is the total peak current in one strip and P_{avg} is the average power flowing in the positive z direction. The average flowing power can be expressed as

$$P_{\text{avg}} = \tfrac{1}{2}\text{Re} \iint (\mathbf{E} \times \mathbf{H}^*) \cdot \mathbf{u}_z \, dx \, dy \tag{11-3-2}$$

where $\mathbf{E}_x$ = electric field intensity in the positive x direction
$\mathbf{H}_y$ = magnetic field intensity in the positive y direction
$*$ = conjugate

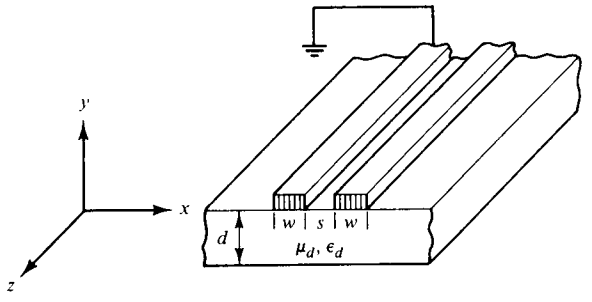


Figure 11-3-1 Schematic diagram of a coplanar strip line.

Example 11-3-1: Characteristic Impedance of a Coplanar Strip Line

A coplanar strip line carries an average power of 250 mW and a peak current of 100 mA. Determine the characteristic impedance of the coplanar strip line.

Solution From Eq. (11-3-1), the characteristic impedance of the coplanar strip line is

$$Z_0 = \frac{2 \times 250 \times 10^{-3}}{(100 \times 10^{-3})^2} = 50\ \Omega$$

11-4 SHIELDED STRIP LINES

A partially shielded strip line has its strip conductor embedded in a dielectric medium, and its top and bottom ground planes have no connection, as shown in Fig. 11-4-1.

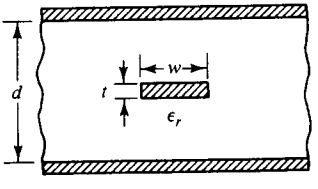


Figure 11-4-1 Partially shielded strip line.

The characteristic impedance for a wide strip ($w/d \gg 0.35$) [14] is

$$Z_0 = \frac{94.15}{\sqrt{\epsilon_r}} \left(\frac{w}{d} K + \frac{C_f}{8.854\epsilon_r} \right)^{-1} \tag{11-4-1}$$

where $K = \dfrac{1}{1 - t/d}$

t = the strip thickness

d = the distance between the two ground planes

$C_f = \dfrac{8.854\epsilon_r}{\pi}[2K \ln (K + 1) - (K - 1) \ln (K^2 - 1)]$ and is the fringe capacitance in pF/m

Figure 11-4-2 shows the characteristic impedance $\mathbf{Z}_0$ for a partially shielded strip line, with the t/d radio as a parameter.

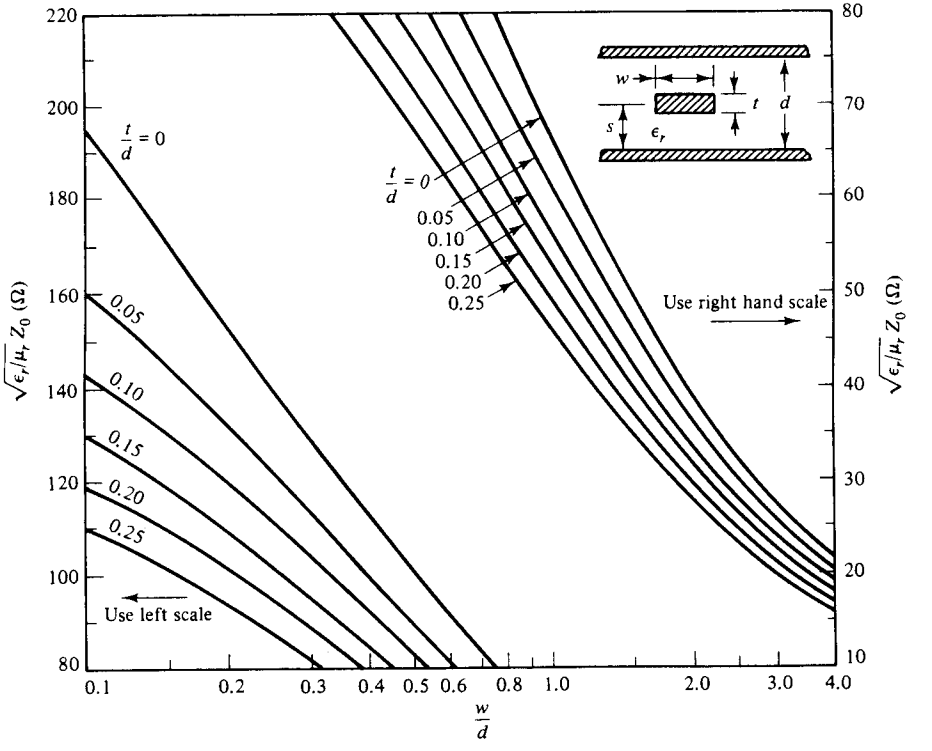


Figure 11-4-2 Characteristic impedance $\mathbf{Z}_0$ of a partially shielded strip line with the t/d ratio as a parameter. (*After S. Cohn [14]; reprinted by permission of IEEE, Inc.*)

Example 11-4-1: Characteristic Impedance of a Shielded Strip Line

A shielded strip line has the following parameters:

Dielectric constant of the insulator (polystyrene):	$\epsilon_r = 2.56$
Strip width:	$w = 25$ mils
Strip thickness:	$t = 14$ mils
Shield depth:	$d = 70$ mils

Calculate:

a. The K factor
b. The fringe capacitance
c. The characteristic impedance of the line.

Solution

a. Using Eq. (11-4-1), the K factor is obtained:

$$K = \left(1 - \frac{t}{d}\right)^{-1} = \left(\frac{1 - 14}{70}\right)^{-1} = 1.25$$

b. From Eq. (11-4-1), the fringe capacitance is

$$C_f = \frac{8.854 \times 2.56}{3.1416}[2 \times 1.25 \ln (1.25 + 1) - (1.25 - 1) \ln (1.25^2 - 1)]$$

$$= 15.61 \text{ pF/m}.$$

c. The characteristic impedance from Eq. (11-4-1) is

$$Z_0 = \frac{94.15}{\sqrt{2.56}}\left[\frac{25}{70}(1.25) + \frac{15.61}{8.854 \times 2.56}\right]^{-1}$$

$$= 50.29\ \Omega$$

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PROBLEMS

Microstrip Lines

11-1. A microstrip line has the following parameters:

$\epsilon_r = 5.23$ and is the relative dielectric constant of the fiberglass board material
$h = 0.8$ mils
$t = 2.8$ mils
$w = 10$ mils

Write a FORTRAN program to complete the characteristic impedance Z_0 of the line. Use a READ statement to read in the input values, the F10.5 format for numerical outputs, and the Hollerith format for character outputs.

11-2. Since modes on microstrip lines are only quasi-transverse electric and magnetic (TEM), the theory of TEM-coupled lines applies only approximately. From the basic theory of a lossless line, show that the inductance L and capacitance C of a microstrip line are

$$L = \frac{Z_0}{v} = \frac{Z_0\sqrt{\epsilon_r}}{c}$$

and

$$C = \frac{1}{Z_0 v} = \frac{\sqrt{\epsilon_r}}{Z_0 c}$$

where Z_0 = characteristic impedance of the microstrip line
v = wave velocity in the microstrip line
$c = 3 \times 10^8$ m/s, the velocity of light in vacuum
ϵ_r = relative dielectric constant of the board material

11-3. A microstrip line is constructed of a perfect conductor and a lossless dielectric board. The relative dielectric constant of the fiberglass-epoxy board is 5.23, and the line characteristic impedance is 50 Ω. Calculate the line inductance and the line capacitance.

11-4. A microstrip line is constructed of a copper conductor and nylon phenolic board. The relative dielectric constant of the board material is 4.19, measured at 25 GHz, and its thickness is 0.4836 mm (19 mils). The line width is 0.635 mm (25 mils), and the line thickness is 0.071 mm (2.8 mils). Calculate the

a. Characteristic impedance Z_0 of the microstrip line
b. Dielectric filling factor q
c. Dielectric attenuation constant α_d
d. Surface skin resistivity R_s of the copper conductor at 25 GHz
e. Conductor attenuation constant α_c

11-5. A microstrip line is made of a copper conductor 0.254 mm (10 mils) wide on a G-10 fiberglass-epoxy board 0.20 mm (8 mils) in height. The relative dielectric constant ϵ_r of the board material is 4.8, measured at 25 GHz. The microstrip line 0.035-mm (1.4 mils) thick is to be used for 10 GHz. Determine the
a. Characteristic impedance Z_0 of the microstrip line
b. Surface resistivity R_s of the copper conductor
c. Conductor attenuation constant α_c
d. Dielectric attenuation constant α_d
e. Quality factors Q_c and Q_d

Parallel Striplines

11-6. A gold parallel stripline has the following parameters:

Relative dielectric constant of teflon:	$\epsilon_{rd} = 2.1$
Strip width:	$w = 26$ mm
Separation distance:	$d = 5$ mm
Conductivity of gold:	$\sigma_c = 4.1 \times 10^7$ ℧/m
Frequency:	$f = 10$ GHz

Determine the
a. Surface resistance of the gold strip
b. Characteristic impedance of the strip line
c. Phase velocity

11-7. A gold parallel strip line has the following parameters:

Relative dielectric constant of polyethylene:	$\epsilon_{rd} = 2.25$
Strip width:	$w = 25$ mm
Separation distance:	$d = 5$ mm

Calculate the
a. Characteristic impedance of the strip line
b. Strip-line capacitance
c. Strip-line inductance
d. Phase velocity

Coplanar Strip Lines

11-8. A 50-Ω coplanar strip line has the following parameters:

Relative dielectric constant of alumina:	$\epsilon_{rd} = 10$
Strip width:	$w = 4$ mm
Strip thickness:	$t = 1$ mm

TEM-mode field intensities:

$$E_y = 3.16 \times 10^3 \sin\left(\frac{\pi x}{w}\right) e^{-j\beta z}$$

$$H_x = 63.20 \sin\left(\frac{\pi x}{w}\right) e^{-j\beta z}$$

Find the
a. Average power flow
b. Peak current in one strip

11-9. A shielded stripline has the following parameters:

Relative dielectric constant of the insulator polyethylene:	$\epsilon_{rd} = 2.25$
Strip width:	$w = 2$ mm
Strip thickness:	$t = 0.5$ mm
Shield depth:	$d = 4$ mm

Calculate the
a. K factor
b. Fringe capacitance
c. Characteristic impedance

11-10. A shielded strip line is made of a gold strip in a polystyrene dielectric insulator and has the following parameters:

Relative dielectric constant of polystyrene:	$\epsilon_{rd} = 2.56$
Strip width:	$w = 0.7$ mm
Strip thickness:	$t = 1.4$ mm
Shield depth:	$d = 3.5$ mm

Determine the
a. K factor
b. Fringe capacitance
c. Characteristic impedance

Chapter 12

Monolithic Microwave Integrated Circuits

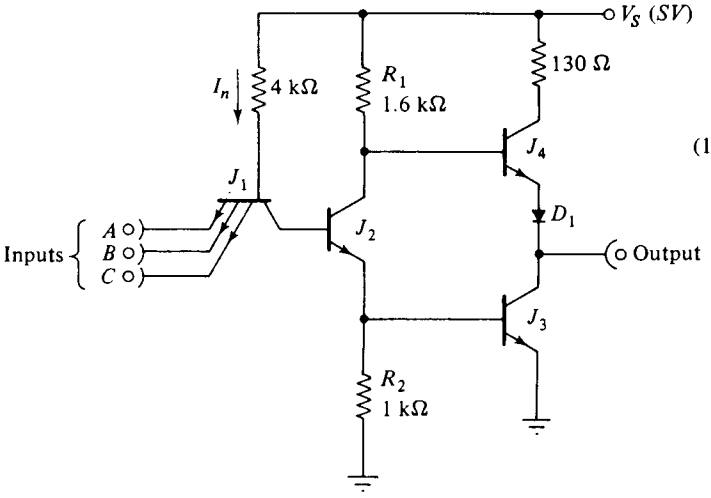
12-0 INTRODUCTION

Integrated circuits are a combination of active and passive elements that are manufactured by successive diffusion or ion implantation processes on a semiconductor substrate. The active elements are generally silicon planar chips. The passive elements are either thin or thick film components. In thin films, a thin film of conducting (resistor) or nonconducting (capacitor) material is deposited on a passive insulated substrate, such as ceramic, glass, or silicon dioxide, by vacuum deposition. Thick film refers to films more than several thousand angstroms (Å) thick. Such films are used almost exclusively to form resistors, and the pattern is usually defined by silk-screening.

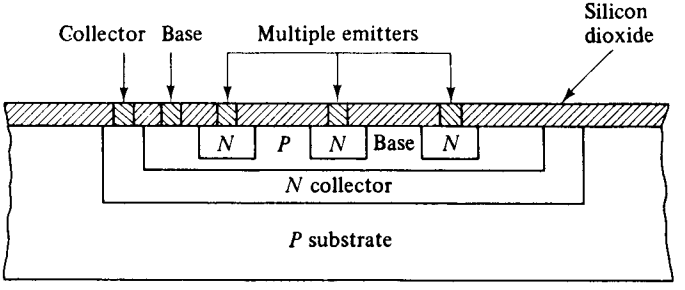
The integrated-circuit (IC) complexity has advanced from small-scale integration (SSI) for up to 100 components per chip, to medium-scale integration (MSI) for up to 1000 components per chip, to large-scale integration (LSI) for up to 10^5 components per chip, and finally the very large-scale integration (VLSI) for more than 1 million components per chip. Recently, the integrated circuit has advanced to the ultralarge-scale integration (ULSI) stage. For example, a 32-bit microprocessor chip contains more than 0.15×10^6 components, and a 1-megabit dynamic random-access memory (DRAM) chip contains more than 2.2×10^6 components. In this chapter, we discuss the integrated circuit devices.

Electronic circuits can be classified into three categories according to circuit technology as shown in Fig. 12-0-1.

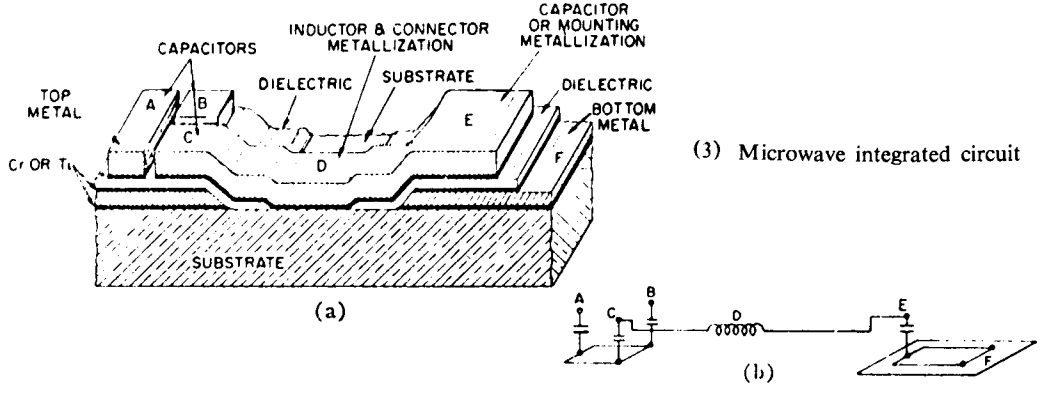
1. Discrete circuit (DC): The conventional electrical or electronic circuit, in which the elements are separately manufactured and then connected together



(1) Discrete circuit where elements are separately made



(2) Integrated circuit for J_1 of (1)



(3) Microwave integrated circuit

Figure 12-0-1 Discrete circuit, integrated circuit and microwave integrated circuit. (*From M. Caulton et al. [1]; reprinted by permission of IEEE, Inc.*)

by conducting wires, is now referred to as a *discrete circuit*. The word *discrete* means separately distinct.

2. Integrated circuit (IC): The integrated circuit consists of a single-crystal chip of semiconductor, typically 50 × 50 mils in cross section, containing both active and passive elements and their interconnections.
3. Monolithic microwave integrated circuit (MMIC): The word *monolithic* is derived from the Greek *monos* (single) and *lithos* (stone). Thus a monolithic integrated circuit is built on a single crystal. Such circuits are produced by the processes of epitaxial growth, masked impurity diffusion, oxidation growth, and oxide etching. Monolithic integrated circuits, like conventional integrated circuits, can be made in monolithic or hybrid form. However, MMICs are quite different from the conventional ICs. The conventional ICs contain very high packing densities, whereas the packing density of a typical MMIC is quite low. An MMIC whose elements are formed on an insulating substrate, such as glass or ceramic, is called a *film integrated circuit*. An MMIC, which consists of a combination of two or more integrated circuit types, such as monolithic or film, or one IC type together with discrete elements, is referred to as a *hybrid integrated circuit*.

Monolithic microwave integrated circuits offer the following advantages over discrete circuits:

1. Low cost (because of the large quantities processed)
2. Small size
3. Light weight
4. High reliability (all components are fabricated simultaneously, and there are no soldered joints)
5. Improved reproducibility
6. Improved performance

MMICs are suitable for space and military applications because they meet the requirements for shock, temperature conditions, and severe vibration. A major factor in the success of MMICs has been the advances in the development of microwave solid-state devices as described previously. In this chapter the basic materials and processes necessary for fabrication of MMICs are described. Three general types of circuits can be utilized for hybrid MMICs: distributed microstrip lines, lumped-element (inductors and capacitors) circuits, and thin-film circuits. These three types are discussed in Section 4.

12-1 MATERIALS

The basic materials for monolithic microwave integrated circuits, in general, are subdivided into four categories:

1. Substrate materials—alumina, beryllia, ferrite/garnet, GaAs, glass, rutile, and sapphire
2. Conductor materials—aluminum, copper, gold, and silver
3. Dielectric films—Al_2O_3, SiO, SiO_2, Si_3N_4, and Ta_2O_5
4. Resistive films—Cr, Cr-SiO, NiCr, Ta, and Ti

12-1-1 Substrate Materials

A substrate of monolithic microwave integrated circuits is a piece of substance on which electronic devices are built. The ideal substrate materials should have the following characteristics [2]:

1. High dielectric constant (9 or higher)
2. Low dissipation factor or loss tangent
3. Dielectric constant should remain constant over the frequency range of interest and over the temperature range of interest
4. High purity and constant thickness
5. High surface smoothness
6. High resistivity and dielectric strength
7. High thermal conductivity

Table 12-1-1 lists the properties of some popular substrates that have been used for MMICs [3,4]. The selection of a substrate material also depends on the expected circuit dissipation, the circuit function, and the type of circuit to be used.

TABLE 12-1-1 PROPERTIES OF SUBSTRATES

Material	$\tan\theta \times 10^4$ at 10 GHz	Relative dielectric constant (ϵ_r)	Thermal conductivity K (W/cm°C)	Applications
Alumina	2	10	0.3	Microstrip, suspended substrate
Beryllia	1	6	2.5	Compound substrated
Ferrite/garnet	2	13–16	0.03	Microstrip, coplanar, compound substrate
GaAs	16	13	0.03	High frequency, microstrip, monolithic MIC
Glass	4	5	0.01	Lumped element
Rutile	4	100	0.02	Microstrip
Sapphire	1	9.3–11.7	0.4	Microstrip, lumped element

Source: From H. Sobol [4]; reprinted by permission of IEEE, Inc.

12-1-2 Conductor Materials

The ideal conductor materials for monolithic microwave integrated circuits should have the following properties [2]:

1. High conductivity
2. Low temperature coefficient of resistance
3. Good adhesion to the substrate
4. Good etchability and solderability
5. Easily deposited or electroplated

Table 12-1-2 shows the properties of some widely used conductor materials for microcircuits [4]. These materials not only have excellent conductivity, but they can also be deposited by a number of methods and are capable of being photoetched. They are used to form both the conductor pattern and the bottom ground plane. The conductor thickness should be equal to at least four skin depths, to include 98% of the current density. It can be seen from Table 12-1-2 that good electrical conductors have poor substrate adhesion, whereas poor electrical conductors have good substrate adhesion. Aluminum has relatively good conductivity and good adhesion. It is possible to obtain good adhesion with high-conductivity materials by using a very thin film of one of the poorer conductors between the substrate and the good conductor. Some typical combinations are Cr-Au, Cr-Cu, and Ta-Au. A typical adhesion layer may have a surface resistivity ranging from 500 to 1000 Ω/square without loss. The choice of conductors is usually determined by compatibility with other materials required in the circuit and the processes required. For small losses, the conductors should be of the order of three to five skin depths in thickness. That is, thick films of

TABLE 12-1-2 PROPERTIES OF CONDUCTORS

Material	Skin depth δ at GHZ (μm)	Surface resistivity (Ω/sq $\times 10^{-7}\sqrt{f}$)	Coefficient of thermal expansion (α_t/°C $\times 10^6$)	Adherence to dielectric film or substrate	Method of deposition
Ag	1.4	2.5	21	Poor	Evaporation, screening
Cu	1.5	2.6	18	Very poor	Evaporation, plating
Au	1.7	3.0	15	Very poor	Evaporation, plating
Al	1.9	3.3	26	Very good	Evaporation
W	2.6	4.7	4.6	Good	sputtering, vapor phase, electron-beam evaporation
Mo	2.7	4.7	6.0	Good	Electron-beam evaporation, sputtering
Cr	2.7	4.7	9.0	Good	Evaporation
Ta	4.0	7.2	6.6	Very good	Electron-beam sputtering

Source: After H. Sobol [4]; reprinted by permission of IEEE, Inc.

the good conductor (about 10 μm thick) are required. Films of this thickness can be achieved by evaporation or plating or by any of the standard thick-film processes.

12-1-3 Dielectric Materials

Dielectric materials are used in monolithic microwave integrated circuits for blockers, capacitors, and some couple-line structures. The properties of dielectric materials should be

1. Reproducibility
2. Capability of withstanding high voltages
3. Ability to undergo processes without developing pin holes
4. Low RF dielectric loss

Some of the dielectrics used in microcircuits are shown in Table 12-1-3; SiO, SiO_2, and Ta_2O_5 are the most commonly used. Thin-film SiO_2 with high-dielectric Q can be obtained by growing the pyrolitic deposition of SiO_2 from silane and then densifying it by heat treatment. SiO_2 can also be deposited by sputtering. With proper processing, SiO_2 capacitors with Qs in excess of 100 have been fabricated with good success. Capacitors fabricated with SiO_2 films have capacitances in the range of 0.02 to 0.05 pF/square mil. Thin-film SiO is not very stable and can be used only in noncritical applications, such as bypass capacitors. In power microwave integrated circuits, capacitors may require breakdown voltages in excess of 200 volts. Such capacitors can be achieved with films on the order of 0.5 to 1.0 μm thick with low probability of pin holes or shorts.

TABLE 12-1-3 PROPERTIES OF DIELECTRIC MATERIALS

Material	Method of deposition	Relative dielectric constant (ϵ_r)	Dielectric strength (V/cm)	Microwave Q
SiO	Evaporation	6–8	4×10^5	30
SiO_2	Deposition	4	10^7	100–1000
Si_3N_4	Vapor phase,	7.6	10^7	
	sputtering	6.5	10^7	
Al_2O_3	Anodization, evaporation	7–10	4×10^6	
Ta_2O_5	Anodization, sputtering	22–25	6×10^6	100

Source: After H. Sobol [4]; reprinted by permission of IEEE Inc.

12-1-4 Resistive Materials

Resistive materials are used in monolithic microwave integrated circuits for bias networks, terminations, and attenuators. The properties required for a good microwave resistor are similar to those required for low-frequency resistors and should be [5]

1. Good stability
2. Low temperature coefficient of resistance (TCR)
3. Adequate dissipation capability
4. Sheet resistivities in the range of 10 to 1000 Ω per square

Table 12-1-4 lists some of the thin-film resistive materials used in monolithic integrated circuits. Evaporated nichrome and tantalum nitride are the most widely used materials. The exact temperature coefficient of resistance achieved depends on film formation conditions. Thick-film resistors may be utilized in circuits incorporating chip components. The thickness of the thick film is in the range of 1 to 500 μm. The term *thick film* refers to the process used, not to the film thickness. Thick-film techniques involve silk-screening through a mask, such as the printing and screening of silver or gold in a glass frit, which is applied on the ceramic and fired at 850° C. Microwave thick-film metals are sometimes several micrometers thick, thicker than those of low-frequency integrated circuits.

TABLE 12-1-4 PROPERTIES OF RESISTIVE MATERIALS

Material	Method of deposition	Resistivity (Ω/square)	TCR (%/°C)	Stability
Cr	Evaporation	10–1000	−0.100–+0.10	Poor
NiCr	Evaporation	40–400	+0.002–+0.10	Good
Ta	Sputtering	5–100	−0.010–+0.01	Excellent
Cr-SiO	Evaporation or cermet	~600	−0.005–−0.02	Fair
Ti	Evaporation	5–2000	−0.100–+0.10	Fair

Source: From H. Sobol [4]; reprinted by permission of IEEE, Inc.

12-2 MONOLITHIC MICROWAVE INTEGRATED-CIRCUIT GROWTH

Like lower-frequency integrated circuits, monolithic microwave integrated circuits (MMICs) can be made in monolithic or hybrid form. In a monolithic circuit, active devices are grown on or in a semiconducting substrate, and passive elements are either deposited on the substrate or grown in it. In the hybrid circuit active devices are attached to a glass, ceramic, or substrate, which contains the passive circuitry. Monolithic integrated circuits have been successful in digital and linear applications in which all required circuit components can be simultaneously fabricated. In most cases, the same device, such as bipolar or metal-oxide-semiconductor (MOS) transistors, can be used for amplifiers, diodes, resistors, and capacitors with no loss in performance. Many digital circuits used in computers require large arrays of identical devices. Thus the conventional ICs contain very high packing densities. On the other hand, very few applications of microwave integrated circuits require densely packed arrays of identical devices, and there is little opportunity to utilize active devices for passive components.

Monolithic technology is not well suited to microwave integrated circuits because the processing difficulties, low yields, and poor performance have seriously limited their applications. To date, the hybrid form of technology is used almost exclusively for microwave integrated circuits in the frequency range of 1 to 15 GHz. Hybrid MMICs are fabricated on a high-quality ceramic, glass, or ferrite substrate. The passive circuit elements are deposited on the substrate, and active devices are mounted on the substrate and connected to the passive circuit. The active devices may be utilized in chip form, in chip carriers, or in small plastic packages. The resistivity of microwave integrated circuits should be much greater than 1000 Ω–cm for good circuit performance.

12-2-1 MMIC Fabrication Techniques

Monolithic microwave integrated circuits (MMICs) can be fabricated by using different techniques such as diffusion and ion implantation, oxidation and film deposition, epitaxial growth, lithography, etching and photoresist, and deposition.

Diffusion and ion implantation. Diffusion and ion implantation are the two processes used in controlling amounts of dopants in semiconductor device fabrications. The process of diffusion consists of diffusing impurities into a pure material in order to alter the basic electronic characteristics of the pure material. Ion implantation is used to dope the substrate crystal with high-energy ion impurities. Both processes are used to dope selectively the semiconductor substrate to produce either an *n*- or *p*-type layer. Until 1970, selective doping was performed mainly by the diffusion method at elevated temperatures. Since 1970, many doping operations have been conducted by ion implantation. In this process the dopant ions are implanted into the semiconductor by using a high-energy ion beam. The advantages of the ion-implantation method are precise control of the total amount of dopants, the improvement of reproducibility, and reduced processing temperature. Both diffusion and ion implantation can be used for fabricating discrete and integrated devices because these processes are generally complementary to one another.

Oxidation and film deposition. To fabricate discrete and integrated devices or circuits many different types of thin films are used. There are four groups of thin films:

1. Thermal oxides
2. Dielectric layers
3. Polycrystalline silicon
4. Metal films

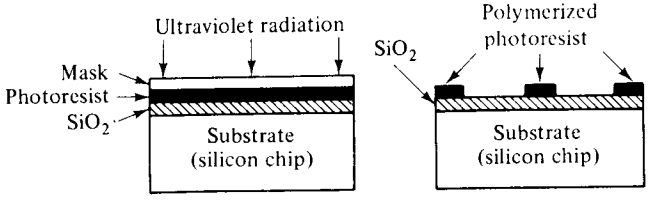
Epitaxial growth. In epitaxy technology, single-crystal semiconductor layers grow on a single-crystal semiconductor substrate. The word *epitaxy* comes from the Greek *epi* (on) and *taxis* (arrangement). The epitaxial process offers an important means of controlling the doping profiles so that device and circuit performances can be optimized. There are three types of epitaxy.

1. Vapor-phase epitaxy (VPE) is the most important technique for silicon and GaAs devices.
2. Molecular-beam epitaxy (MBE) is a process involving the reaction of one or more thermal beams of atoms or molecules with a crystalline surface under ultrahigh vacuum conditions ($\sim 10^{-1}$ torr). MBE can achieve precise control in both chemical composition and doping profiles. Single-crystal multilayer structures with dimensions of the order of atomic layers can be made by the MBE method.
3. Liquid-phase epitaxy (LPE) is the growth of epitaxial layers on crystalline substrates by direct precipitation from the liquid phase. This process is particularly useful for growing GaAs and related III–V compounds. LPE is suited to grow thin epitaxial layers (≥ 0.2 μm) because it has a slow growth rate. It is also useful to grow multilayered structures in which precise doping and composition controls are required.

Lithography. Lithography is the process of transferring patterns of geometric shapes on a mask to a thin layer of radiation-sensitive material, which is known as *resist*, for covering the surface of a semiconductor wafer. The resist patterns defined by the lithographic process are not permanent elements of the final device but only replicas of circuit features. There are four types of lithography technology:

1. Electron-beam lithography
2. Ion-beam lithography
3. Optical lithography
4. X-ray lithography

Etching and photoresist. In the processes of making MICs, a selective removal of SiO_2 is required in order to form openings through which impurities can be diffused. The photoetching method used for this removal is shown in Fig. 12-2-1.



(a) Masking and exposure to ultraviolet radiation

(b) Photoresist

Figure 12-2-1 Photoetching process.

During the photolithographic process the substrate is coated with a uniform film of Kodak photoresist (KPR), which is a photosensitive emulsion. A mask for the desired openings is placed over the photoresist, and ultraviolet light exposes the photoresist through the mask as shown in Fig. 12-2-1(a). A polymerized photoresist is developed, and the unpolymerized portions are dissolved by using trichloroethylene after the mask is removed; see Fig. 12-2-1(b). The SiO_2, which is not covered by the photoresist, can be removed by hydrofluoric acid. The thick-film

process usually involves the printing and silk-screening of silver or gold through a metal mask in a glass frit, which is applied on the ceramic and fired at 850° C. After firing, the initial layer may be covered with gold.

Deposition. Three methods—vacuum evaporation, electron-beam evaporation, and dc sputtering—are commonly used for making MMICs.

Vacuum Evaporation. Here the impurity material to be evaporated is placed in a metallic boat through which a high current is passed. The substrate with a mask on it and the heated boat are located in a glass tube in which a high vacuum at a pressure of 10^{-6} to 10^{-8} torr is maintained. The substrate is heated slightly while the heat is evaporating the impurities, and the impurity vapor deposits itself on the substrate, forming a polycrystalline layer on it.

Electron-Beam Evaporation. In another method of evaporating the impurity a narrow beam of electrons is generated to scan the substrate in the boat in order to vaporize the impurity.

dc Sputtering. The third method of vacuum deposition is known as dc sputtering or cathode sputtering. In a vacuum, the crucible containing the impurity is used as the cathode and the substrate as the anode of a diode. A slight trace of argon gas is introduced into the vacuum. When the applied voltage between cathode and anode is high enough, a glow discharge of argon gas is formed. The positive argon ions are accelerated toward the cathode, where they dislodge atoms of the impurity. The impurity atoms have enough energy to reach the substrate and adhere to it.

12-2-2 Fabrication Example

For example, the photoresist technique can be used to remove the oxide layer in related areas. As shown in Fig. 12-2-2, the fabrication procedures include the following:

1. Deposition. An oxide layer is deposited on the semiconductor material, and then a photoresist layer is deposited to cover the oxide on top of the semiconductor chip.
2. Mask. Ultraviolet light is used to shine through a precision photographic mask to the photoresist.
3. Chemical etching. Chemical etching with hydrofluoric acid is used to remove the selected oxide region.
4. Etching. The photoresist is finally dissolved with an organic solvent in the oxide leaving the desired opening.

12-3 MOSFET FABRICATION

In recent years, the metal-oxide-semiconductor field-effect transistor (MOSFET) has superseded the bipolar junction transistor in many electronic applications. This is because the structure of the MOSFET is simple and its cost is low. The MOSFET is the

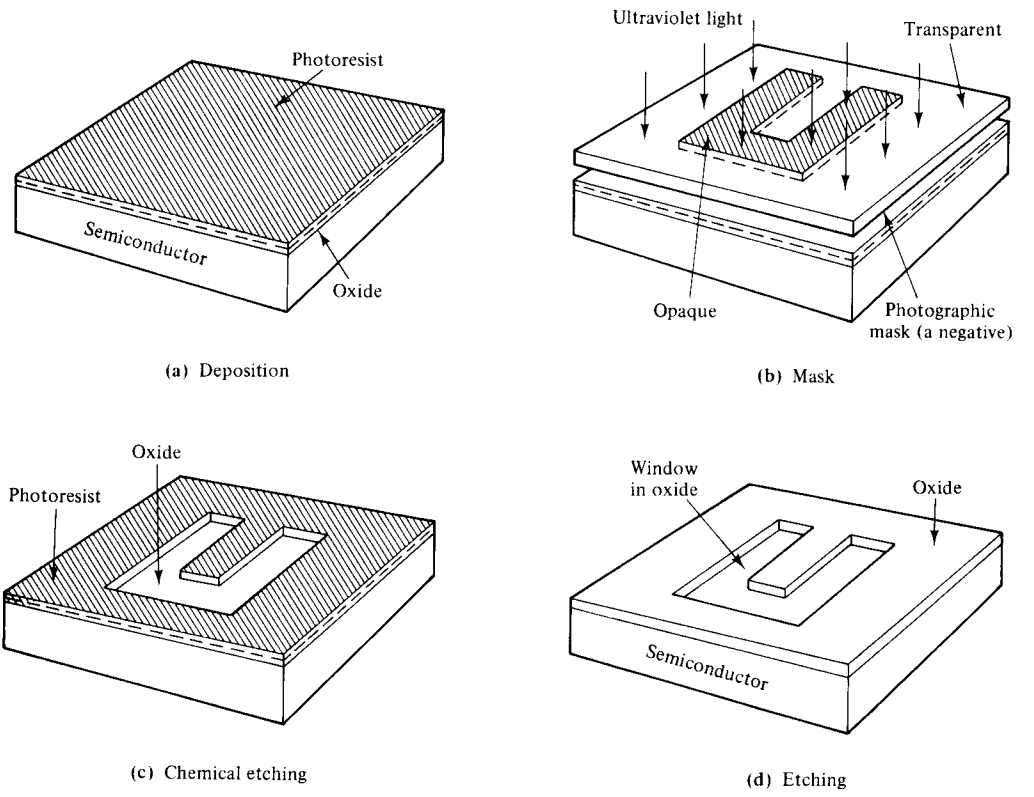


Figure 12-2-2 Illustration of photoresist technique. (*After P. R. Nanavati [6]; courtesy of Intext Educational Publishers.*)

most important device for very large-scale integrated circuits (VLSICs) such as microprocessors and semiconductor memories. Its basic fabrication processes can be described in three areas: MOSFET formation, NMOS growth, and CMOS development.

12-3-1 MOSFET Formation

MOSFETs can be fabricated by using the following steps as shown in Fig. 12-3-1.

1. Oxidation: Select the p-type substrate and form a SiO_2 layer on the surface.
2. Diffusion: Open two windows by using the photoresist technique and diffuse an n^+-layer through the windows.
3. Etching: Remove the center oxide region by the photoetching technique.
4. Oxidation: Again expose the entire surface to dry oxygen so that the SiO_2 covers the top surface.
5. Deposition: Deposit phosphorous glass over the surface to cover the oxide layer.

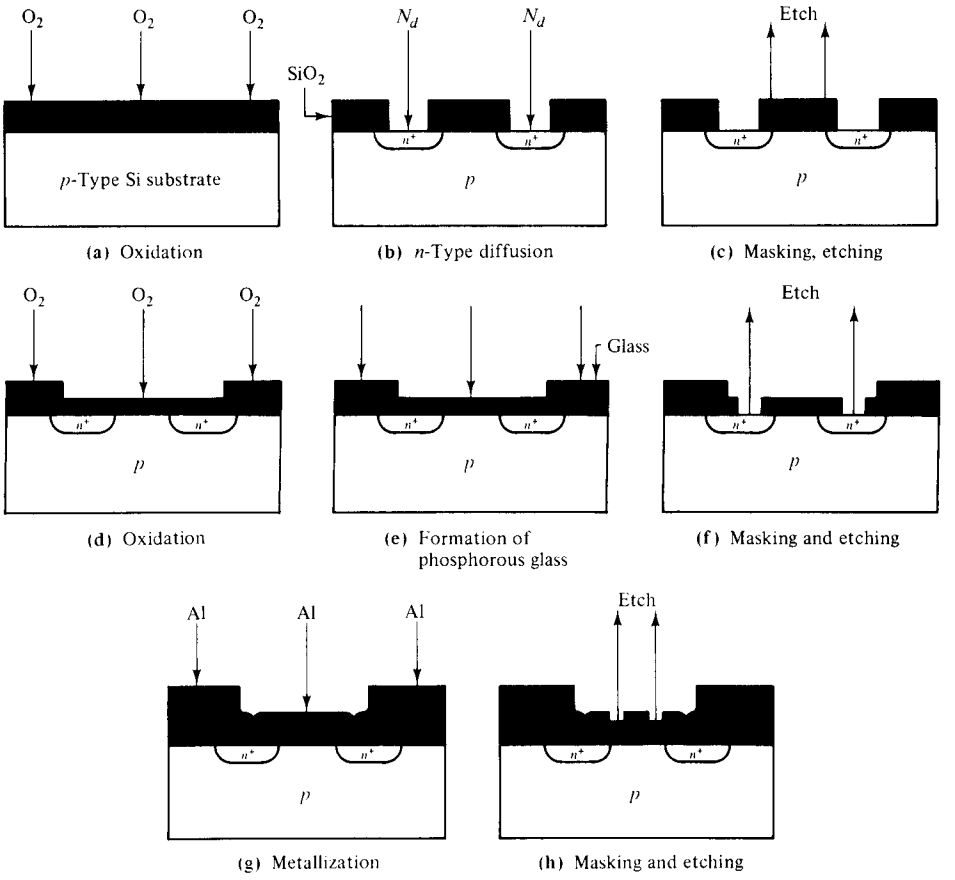


Figure 12-3-1 Fabrication steps for making MOSFETs. (*After P. R. Nanavati [6]; courtesy of Intext Educational Publishers.*)

6. Etching: Open two windows above the two n^+-type diffused regions by using the photoetching method.
7. Metallization: Now see that aluminum metallization is carried out over the entire surface of the device.
8. Etching: Finally, etch away the unwanted metal and attach the metal contacts to the diffused gate, drain, and source regions.

It can be seen that there is only one diffusion process in the fabrication of a MOSFET compared to the three required for the bipolar junction transistor. Therefore, MOSFET fabrication is more efficient and less expensive than the BJT. These attributes make MOSFET integrated circuits attractive.

12-3-2 NMOS Growth

The n-channel MOS (NMOS) logic gate was discussed in Section 6-5-1, and its fabrication processes are described as shown in Fig. 12-3-2.

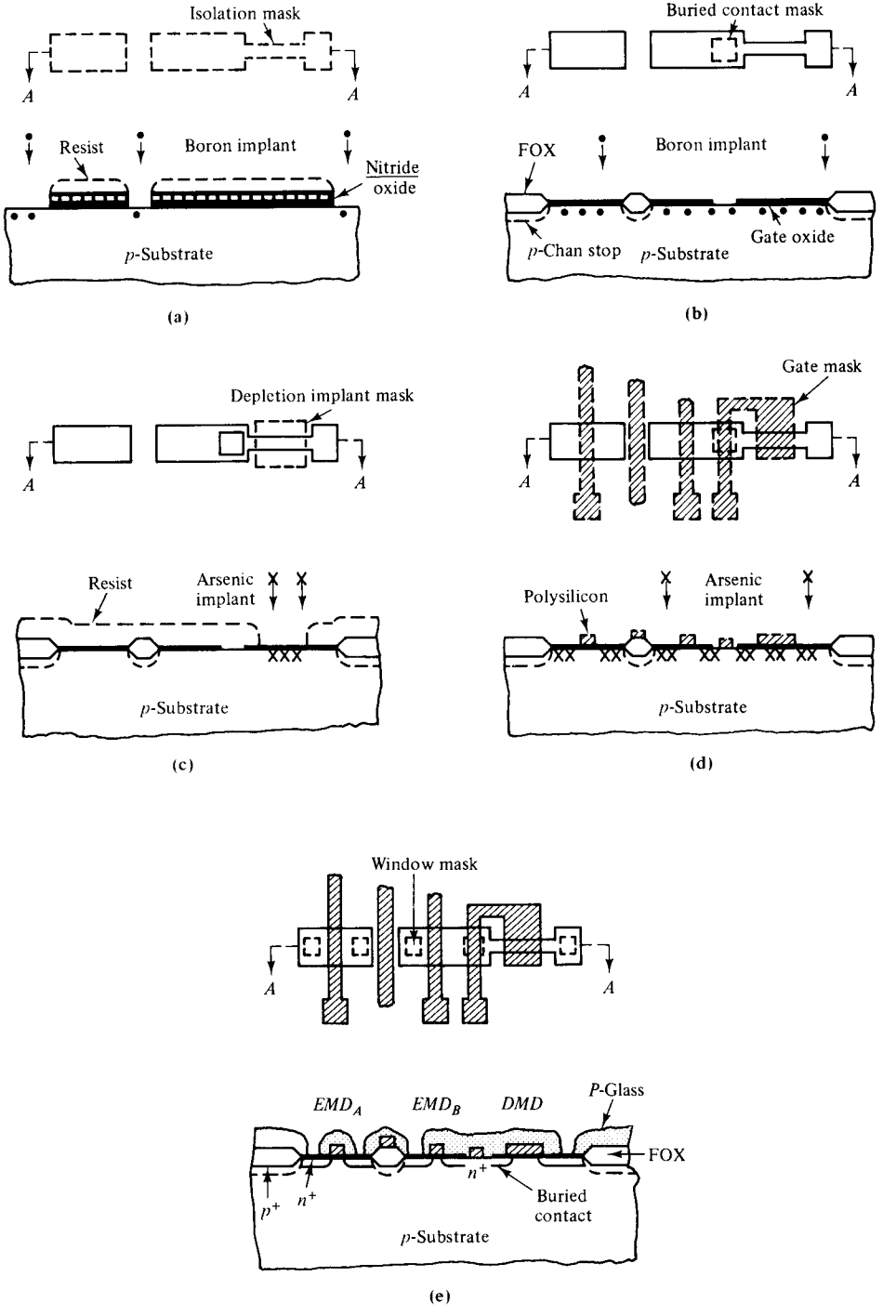


Figure 12-3-2 NMOS fabrication processes. (*After L. C. Parrillo [7]; reprinted by permission of AT&T Bell Laboratories.*)

1. Deposition and implantation: The starting p-type substrate is lightly doped and then an oxide (SiO_2) layer is grown on the top of the substrate. A silicon-nitride (Si_3N_4) layer is deposited on the oxide surface. An isolation mask is used to define the active areas covered by $SiO_2 - Si_3N_4$, and the isolation or field areas are etched by plasma or reactive ion etching.
2. Implantation: Boron ions are implanted as the channel stop to prevent inversion under the field oxide (FOX). The wafer is then put in an oxidation furnace to grow a thick layer of FOX.
3. Implantation: After the nitride-oxide layers are cleaned, a thin gate oxide (about 20 nm thick) is formed. Using the photoresist to mask the enhancement-mode device (EMD), an n-channel implant is made to form the depletion-mode device (DMD).
4. Deposition: The polysilicon is deposited and patterned as the gates. The gates are also used as the self-aligned mask for source and drain arsenic implantation.
5. Metallization: Metal films are evaporated and etched to produce the electrode contacts.

12-3-3 CMOS Development

The CMOS device was described in Section 6-5-2, and its fabrication processes are explained as follows (see Fig. 12-3-3).

1. Epitaxy: The starting material is a lightly doped n epitaxy over a heavily doped n^+ substrate.
   Deposition: A composite layer of SiO_2 (pad) and SiN_4 (nitride) is defined, and silicon is exposed over the intended n-tub region. Phosphorus is implanted as the n-tub dopant at low energy, and enters the exposed silicon, but is masked from the adjacent region by the Si_3N_4 layer.
2. Implantation: The wafers are then selectively oxidized over the n-tub regions. The nitride is stripped and boron is implanted for the p-tub.
3. Oxidation: The boron enters the silicon through the thin pad oxide but is masked from the n tub by the thick SiO_2 layer there. All oxides are then stripped and the two tubs are driven in.
4. Deposition: n^+ polysilicon is deposited and defined, and the source and drain regions are implanted.
5. Implantation: Phosphorus is selectively implanted into the n-channel source and drain regions at a higher dose so that it overcompensates the existing boron.
6. Deposition and metallization: A phosphorus glass layer is then deposited. After windows are dry-etched in the P-glass, aluminum metallization is defined using dry etching.

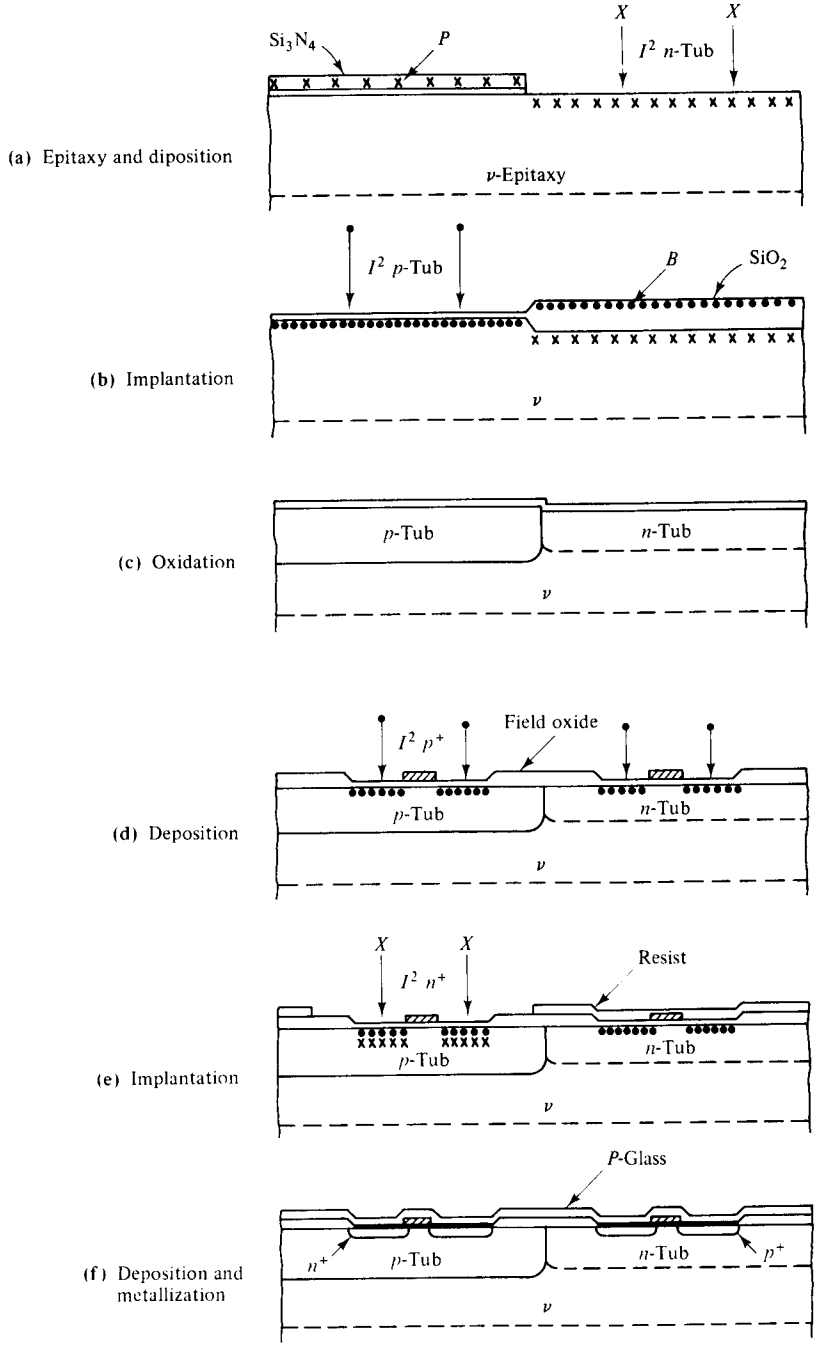


Figure 12-3-3 CMOS fabrication. (*After L. C. Parrillo [7]; reprinted by permission of the Bell Laboratories.*)

12-3-4 Memory Construction

As discussed in Section 6-5-3, there are seven types of memory devices depending on their different structures. Their basic functions are to store in, read out, and write out data. The fabrication processes of a memory are complicated. In this section, some basic fabrication techniques are described.

The *random access memory* (RAM) device is the most basic memory, and it can be subdivided into *static RAM* (SRAM) and *dynamic RAM* (DRAM). Among memory chips, the RAM device has the highest component density per chip. In a RAM any bit of information in a matrix of bits can be accessed independently. Individual rows of memory bits are accessed by a conductive word line which may be a diffusion, polysilicon, or metal line. Similarly, individual columns of bits in the matrix are accessed by a bit line. The acronym RAM is generally used to refer to randomly addressable memories into which data can be written and retrieved indefinitely. The *read-only-memory* (ROM), however, stores data permanently but cannot accept new information. Static RAMs retain their data indefinitely unless the power to the circuit is interrupted. Dynamic RAMs require that the charge (data) stored in each memory cell be "refleshed" periodically to retain the stored data. The fabrication processes of memory devices are described as follows:

1. SRAM cell with transistor load
2. SRAM cell with resistor load
3. DRAM cell with storage capacitor
4. DRAM cell with double-level polysilicon layer

SRAM cell with transistor load. Figure 12-3-4 shows the structure for a single static RAM cell. Figure 12-3-4(b) shows a layout for the SRAM cell. The width-to-channel-length ratio of the depletion-mode load transistor (1/5) is adjusted to provide enough current drive to meet the speed requirements of the cell without causing excessive steady-state (quiescent) power consumption. To minimize the cell area, buried contacts (diffusion to polysilicon contact) are required. Figure 12-3-4(a) shows a six-transistor (n-channel) cell, which uses a cross-coupled inverter pair (flip-flop, T_1 to T_4) to store 1 bit of information. The numbers next to the transistors indicate the relative width-to-channel-length ratios. A pair of access transistors (T_4 and T_5) transmits data into and out of the cell when the word and bit lines are simultaneously activated. The loads for the flip-flop are depletion-mode transistors (T_1 and T_2) with their sources and gates tied together as a NAND circuit. The data (logic 1 or 0) are retained in the cell by the positive feedback existing in the flip-flop circuit. When the gate of T_4 is at a high potential, its drain voltage is low ($\ll V_T$). This voltage, in return, is fed to the gate of T_3, and keeps T_3 off. The drain of T_3 is then tied to the high potential of T_1 (which is always on), so is the gate of T_4. This state of the cell defines a logic 1, which is retained unless new data are entered.

SRAM cell with resistor load. When the depletion-mode load transistors are replaced by high-valued resistors, the structure becomes a *resistor MOS* (RMOS) as shown in Fig. 12-3-5.

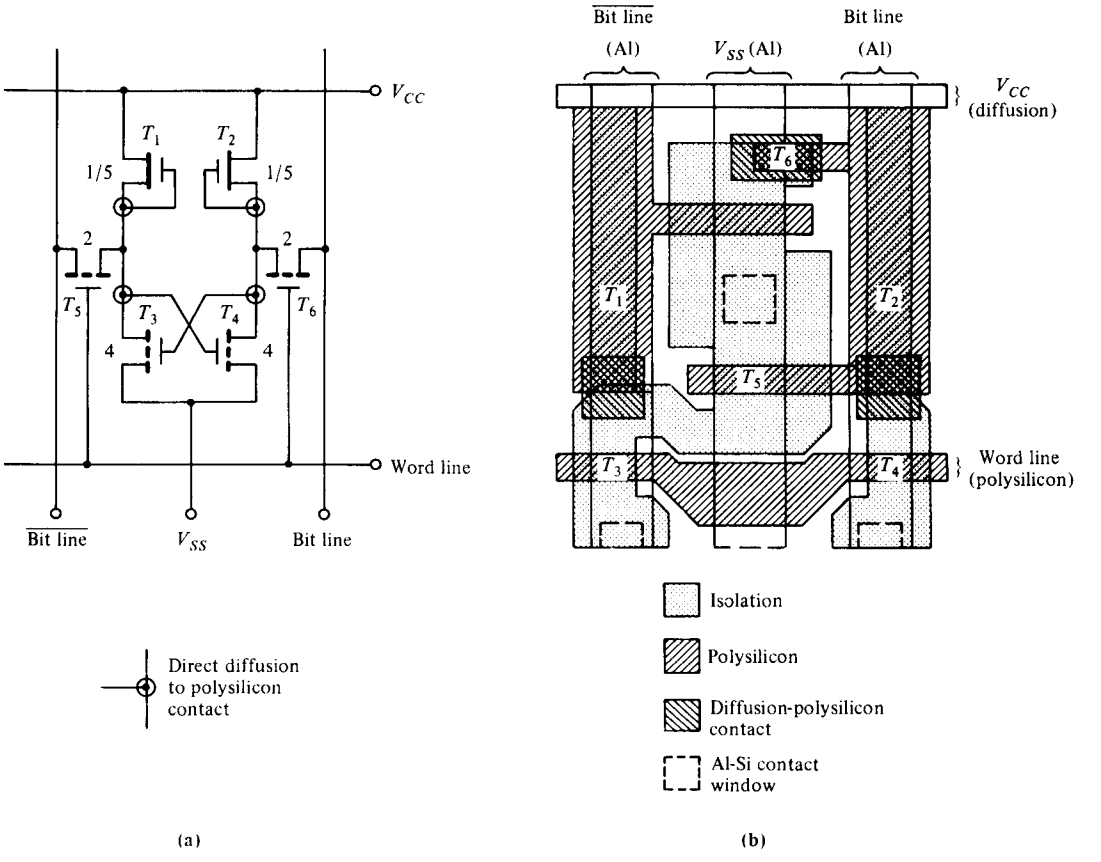


Figure 12-3-4 Structure of a single SRAM cell. (*After R. W. Hunt [8]; reprinted by permission of John Wiley & Sons.*)

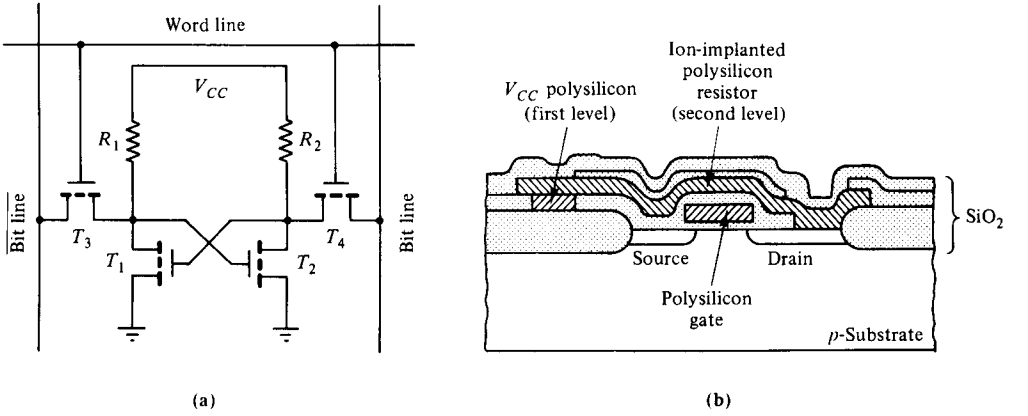


Figure 12-3-5 SRAM cell with resistor load. (*After L. C. Parrillo [7] and T. Ohzone et al. [9]; reprinted by permission of the Bell Lab.*)

High-valued resistors reduce the power consumption, and they can be made in a relatively small space by using polysilicon which has been ion-implanted to provide the proper resistance. The polysilicon resistors (R_1 and R_2) can be made in the same single layer of polysilicon (gate and interconnect) by masking the polysilicon resistor regions from the high-impurity doping used in the gate and interconnect portions of the polysilicon level. Using this type of fabrication process, SRAM-cell areas can be reduced to half the cell area required in conventional transistor load cells. Figure 12-3-5(a) shows the circuit diagram of a SRAM cell with polysilicon resistor load (R_1 and R_2), and (b) the device' cross section. The first-level polysilicon is used for gate and routing power supply V_{CC}. The second-level polysilicon is used for resistor load directly over an active transistor. The connection to the drain and V_{CC} is made directly from an implanted polysilicon resistor.

DRAM cell with storage capacitor. Since a SRAM device consists of a large number of static RAM cells, it can dissipate a great deal of electrical power. For these reasons large memory chips use dynamic RAM cells that require only one transistor and one storage capacitor per bit of information. Figure 12-3-6 shows the diagrams of a basic SRAM cell with storage capacitor.

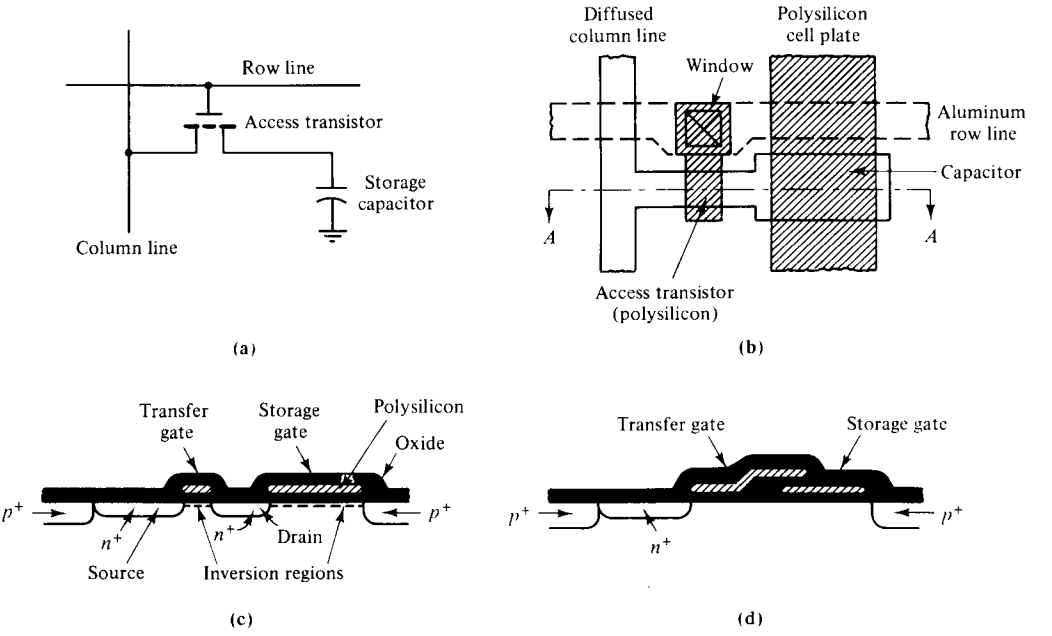


Figure 12-3-6 Diagrams of DRAM cell with storage capacitor. (*After L. C. Parrillo [7] and R. W. Hunt [8]; reprinted by permission of the Bell Laboratories.*)

Figure 12-3-6(a) shows the DRAM cell layout. A diffusion process forms the bit line (source/drain) and also the source of the access transistor. The capacitance of the diffused bit line (or the junction capacitance) and its resistance can be limiting factors for the DRAM performance. In order to minimize these parasitic effects, it is necessary to use $MoSi_2$ for word lines and Al for bit lines in fabricating advanced

memory chips such as the 256-kilobit DRAM. To increase the charge-storage capacity, the use of thinner gate insulators with higher dielectric contacts (e.g., Si_3N_4 and Ta_2O_5 with dielectric constants of 8 and 22, respectively) are being explored. When word and bit lines are simultaneously addressed (or activated to a high voltage), the access transistor is turned on and the charge is transferred into the storage capacitor if it had no initial charge (stored "zero"); little charge is transferred to the storage capacitor if it had been fully charged initially (stored "one"). The amount of charge that the bit line must supply to the storage capacitor is measured by the sensing circuitry, and this information is used to interpret whether a "zero" or "one" has been stored in the cell. The sense circuitry then stores full charge in the capacitor if the charge was there originally, or it fully depletes the capacitor if little charge existed originally. The information in the cell is thus "refleshed" after it is read.

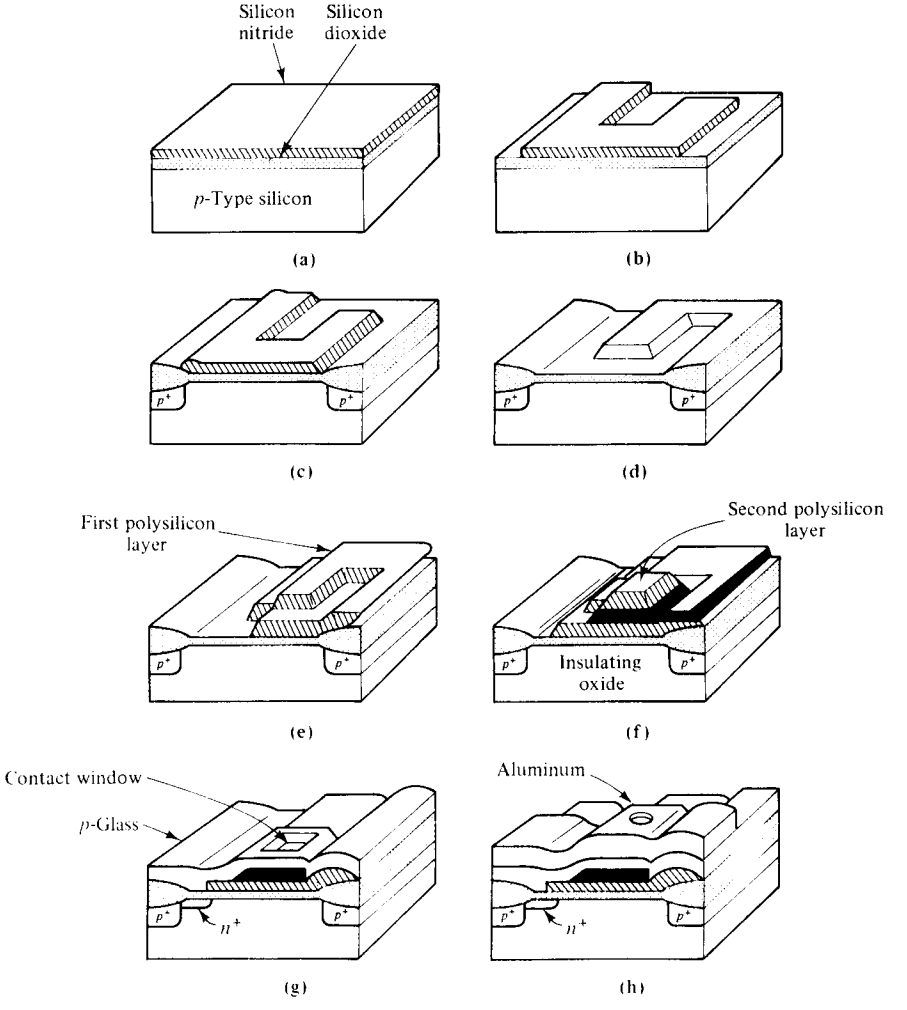


Figure 12-3-7 Diagrams of double-level polysilicon DRAM cell. (*After L. C. Parrillo [7] and W. G. Oldham [10] ; reprinted by permission of the Bell Lab.*)

DRAM cell with double-level polysilicon layers. Figure 12-3-7 shows three-dimensional diagrams of the fabrication processes for the double-level polysilicon DRAM cell. Fabrication processes for the double-level polysilicon DRAM cell follow:

1. Oxidation: The first step is to perform selective oxidation of silicon using silicon nitride-pad oxide layers as the oxidation mask in Fig. 12-3-7(a), (b), and (c).
2. Etching: The silicon nitride-pad oxide layers are then removed in a selective etchant that does not attack silicon, and the first gate oxide is grown [Fig. 12-3-7(d)].
3. Deposition: The first-level polysilicon layer is deposited and patterned as shown in Fig. 12-3-7(e).
4. Oxidation and deposition: The second gate oxide is grown and the second-level polysilicon is deposited and patterned as shown in Fig. 12-3-7(f).
5. Implantation: The exposed gate oxide region is implanted with an n-type dopant. A thick layer of silicon dioxide (P-glass) is deposited next, and the contact windows are opened in the oxide to reach the second-level polysilicon as shown in Fig 12-3-7(g).
6. Deposition: Finally, a layer of aluminum is deposited and patterned as shown in Fig. 12-3-7(h). A protective coating of silicon nitride can be deposited on the wafer to seal it from contaminations.

12-4 THIN-FILM FORMATION

The choice of lumped or distributed elements for amplifier matching networks depends on the operating frequency. When the frequency is up to X band, its wavelength is very short, and a smaller lumped element exhibits a negligible phase shift. Because of the advanced thin-film technology, the size of lumped elements can be greatly reduced and their operating frequencies can reach up to 20 GHz. Beyond that distributed elements are preferred. In monolithic microwave integrated circuits (MMICs), lumped resistors are very useful in thin-film resistive terminations for couplers, lumped capacitors are absolutely essential for bias bypass applications, and planar inductors are extremely useful for matching purposes, especially at lower microwave frequencies where stub inductors are physically too large [11].

12-4-1 Planar Resistor Film

A planar resistor consists of a thin resistive film deposited on an insulating substrate. Thin-film resistor materials are aluminum, copper, gold, nichrome, titanium, tantalium, and so forth, and their resistivity ranges from 30 to 1000 ohms per square. The planar resistors are essential for terminations for hybrid couplers, power combiners or dividers, and bias-voltage circuits. Some design considerations should be aimed to include the following:

1. the sheet resistivity available
2. the thermal stability or temperature coefficient of the resistive material
3. the thermal resistance of the load
4. the frequency bandwidth

Planar resistors can be grouped into semiconductor films, deposited metal films, and cermets.

Planar resistors based on semiconductors can be fabricated by forming an isolated band of conducting epitaxial film on the substrate by mesa etching or by isolation implant of the surrounding conducting film. Another way is by implanting a high-resistivity region within the semi-insulating substrate. Metal-film resistors are formed by evaporating a metal layer over the substrate and forming the desired pattern by photolithography. Cermet resistors are formed from films consisting of a mixture of metal and a dielectric. Figure 12-4-1 shows several examples of planar resistor design.

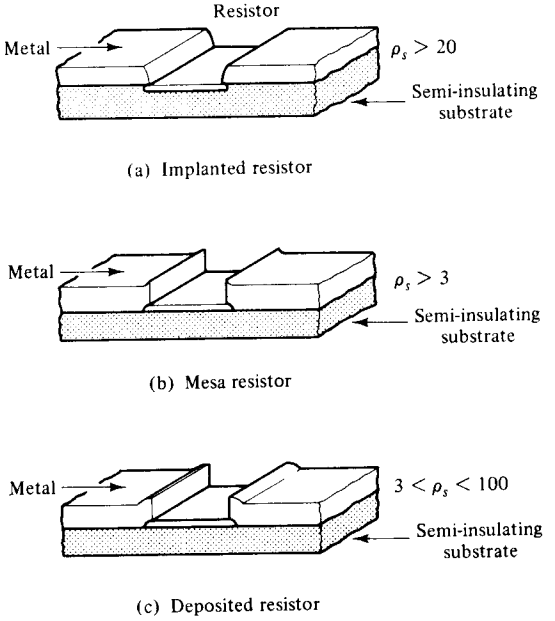


Figure 12-4-1 Configurations of planar resistors.

The resistance of a planar resistor, as shown in Fig. 12-4-2, can be expressed as

$$R = \frac{\ell \rho_s}{wt} \qquad \text{ohms} \tag{12-4-1}$$

where ℓ = length of the resistive film
w = width of the film
ρ_s = sheet resistivity of the film in ohm-meter
t = film thickness in meters

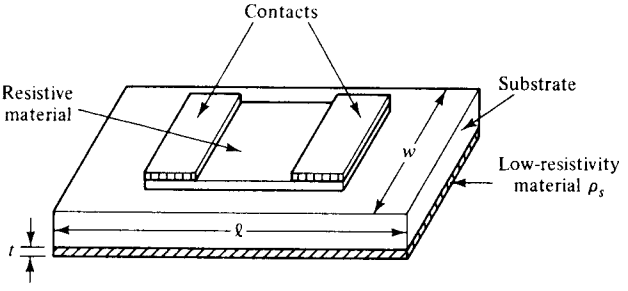


Figure 12-4-2 Thin film resistor.

When units of length ℓ and width w are chosen to have equal magnitude, the result is in a square. Therefore, the resistance R in ohms per square is independent of the dimension of the square.

Example 12-4-1: Resistance of a Planar Resistor

A planar resistor has the following parameters:

Resistive film thickness:	$t = 0.1\ \mu m$
Resistive film length:	$\ell = 10$ mm
Resistive film width:	$w = 10$ mm
Sheet resistivity of gold film:	$\rho_s = 2.44 \times 10^{-8}\ \Omega$–m

Calculate the planar resistance.

Solution The planar resistance is

$$R = \frac{10 \times 2.44 \times 10^{-8}}{10 \times 1 \times 10^{-7}} = 0.244\ \Omega/\text{square}$$

12-4-2 Planar Inductor Film

Planar inductors for monolithic circuits can be realized in a number of configurations some of which are shown in Fig. 12-4-3.

Typical inductance values for monolithic circuits range from 0.5 to 10 nH. The equations of inductance are different for different configurations.

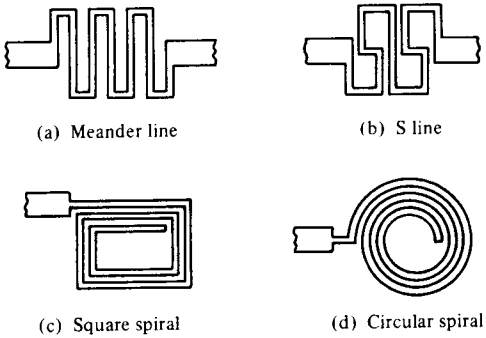


Figure 12-4-3 Configurations of planar inductors.

Ribbon inductor. The inductance of a ribbon inductor can be expressed as [12]:

$$L = 5.08 \times 10^{-3}\ell\left[\ell n\left(\frac{\ell}{w+t}\right) + 1.19 + 0.022\left(\frac{w+t}{\ell}\right)\right] \quad \text{nH/mil} \qquad (12\text{-}4\text{-}2)$$

where ℓ = ribbon length in mils
t = ribbon thickness in mils
w = ribbon width in mils

Round-wire inductor. The inductance of a round-wire inductor is given by

$$L = 5.08 \times 10^{-3}\ell[\ell n(\ell/d) + 0.386] \quad \text{nH/mil} \qquad (12\text{-}4\text{-}3)$$

where d = wire diameter in mils
ℓ = wire length in mils

Circular spiral inductor. The inductance of a circular spiral inductor is expressed as

$$L = 0.03125\, n^2 d_o \quad \text{nH/mil} \qquad (12\text{-}4\text{-}4)$$

where $d_o = 5d_i = 2.5n(w + s)$ in mils
n = number of turns
s = separation in mils
w = film width in mils

Figure 12-4-4 shows the schematic diagram of a circular spiral inductor.

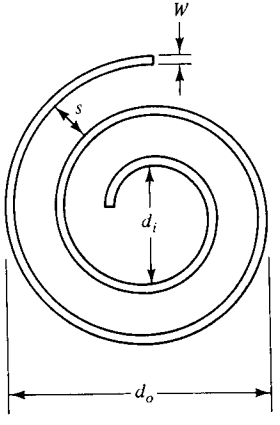


Figure 12-4-4 Circular spiral inductor.

Circular loop inductor. The inductance of a single-turn flat circular loop inductor is given by

$$L = 5.08 \times 10^{-3}\ell\left[\ell n\left(\frac{t}{w+t}\right) - 1.76\right] \quad \text{nH/mil} \qquad (12\text{-}4\text{-}5)$$

Square spiral inductor. The inductance of a square spiral inductor can be written as

$$L = 8.5\, A^{\frac{1}{2}}\, n^{5/3} \qquad \text{nH} \tag{12-4-6}$$

where A = surface area in cm^2
n = number of turns

Example 12-4-2: Calculation of a Planar Circular Spiral Inductor

A circular spiral inductor has the following parameters:

Number of turns:	$n = 5$
Separation:	$s = 100$ mils
Film width:	$w = 50$ mils

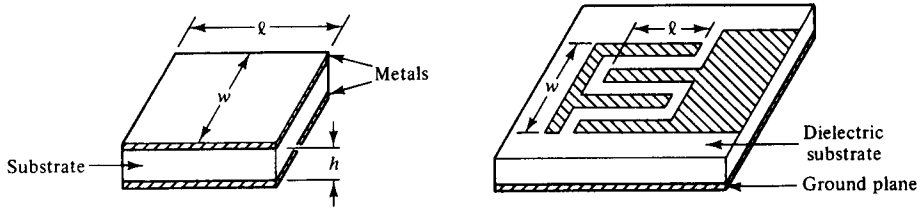
Compute the inductance.

Solution The inductance is

$$L = 0.03125\,(5)^2 \times 2.5\,(5)(50 + 100)$$
$$= 1464.84 \quad \text{nH/mil}$$

12-4-3 Planar Capacitor Film

Two types of planar capacitors commonly used for MMICs are the metal-oxide-metal capacitor and the interdigitated capacitor, as shown in Fig. 12-4-5.



(a) Metal-oxide-metal capacitor (b) Interdigitated capacitor

Figure 12-4-5 Schematic diagrams of planar capacitors.

Metal-oxide-metal capacitor. The metal-oxide-metal capacitor has three layers; the middle dielectric layer is sandwiched by the top and bottom electrode layers as shown in Fig. 12-4-5(a). The capacitance can be expressed as

$$C = \epsilon_o \epsilon_r \frac{\ell w}{h} \qquad \text{farads} \tag{12-4-7}$$

where $\epsilon_o = 8.854 \times 10^{-12}$ F/m
ϵ_r = relative dielectric constant of the dielectric material
ℓ = metal length
w = metal width
h = height of the dielectric material

Interdigitated capacitor. The interdigitated capacitor consists of a single-layer structure, and it can be fabricated easily on substrates as microstrip lines with values between 0.1 and 15 pF as shown in Fig. 12-4-5(b). The capacitance can be approximated as [13]

$$C = \frac{\epsilon_r + 1}{w} \ell[(N - 3)A_1 + A_2] \qquad \text{pF/cm} \qquad (12\text{-}4\text{-}8)$$

where N = number of fingers
$A_1 = 0.089$ pF/cm is the contribution of the interior finger for $h > w$
$A_2 = 0.10$ pF/cm is the contribution of the two external fingers for $h > w$
ℓ = finger length in cm
w = finger-base width in cm

Example 12-4-3: Computations of a Planar Capacitor

An interdigitated capacitor fabricated on a GaAs substrate has the following parameters:

Number of fingers:	$N = 8$
Relative dielectric constant of GaAs:	$\epsilon_r = 13.10$
Substrate height:	$h = 0.254$ cm
Finger length:	$\ell = 0.00254$ cm
Finger-base width:	$w = 0.051$ cm

Compute the capacitance.

Solution The capacitance is

$$C = \frac{13.10 + 1}{0.051} \times 0.00254x[(8 - 3) \times 0.089 + 0.10]$$

$$= 0.380 \text{ pF/cm}$$

12-5 HYBRID INTEGRATED-CIRCUIT FABRICATION

In the hybrid integrated circuit (HIC), semiconductor devices and passive circuit elements are formed on a dielectric substrate. The passive circuits are either distributed elements or lumped elements or a combination of both. The distributed and lumped elements are formed by using a thin- or thick-film process. The distributed circuit elements are generally single-layer metallization. The lumped elements are either fabricated by using multilevel deposition and plating techniques or are attached to the substrate in chip form. Hybrid integrated circuits have been used almost exclusively in the frequency range of 1 to 20 GHz for satellite communications, phased-array radar systems, electronic warfare measures, and other commercial or military electronic systems because they can offer higher reliability, greater reproducibility, better performance, smaller size, and lower cost than conventional electronic circuits or systems.

Hybrid integrated circuits can be classified into two types: hybrid IC and miniature hybrid IC.

1. Hybrid IC: This type uses the distributed circuit elements that are fabricated on a substrate using a single-layer metallization technique. Other circuit elements such as resistors, inductors, capacitors, and semiconductor devices are added to the substrate.
2. Miniature hybrid IC: The miniature hybrid IC uses multilevel elements. All passive elements such as resistors, inductors, and capacitors are deposited on the substrate; the semiconductor devices are attached to the substrate.

Hybrid ICs use a single-layer metallization technique to form the circuit components on a substrate. There are two techniques—plate-through and etchback—for fabricating the hybrid integrated circuits.

Plate-through technique. The plate-through technique begins with a substrate coated with a thin layer of evaporated metal. The second step is to form a thick photoresist as shown in Fig. 12-5-1(a).

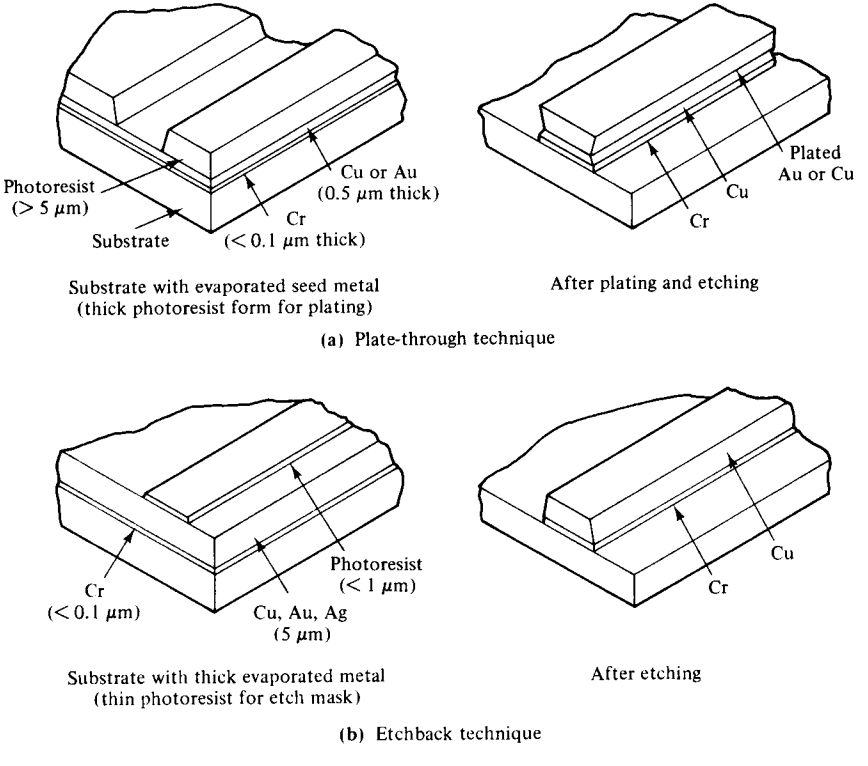


Figure 12-5-1 Fabrication of hybrid ICs. (*After M. Kumar and I. J. Bahl [13]; reprinted by permission of John Wiley & Sons.*)

The thickness of the photoresist is similar to the thickness of the final metal film required. After defining a pattern in the photoresist, the second layer is plated up to the desired thickness with precise definition, and only in the areas where metal is required. Finally, the photoresist layer is removed, and the thin seed metal is etched with very little undercut from the undesired areas.

Etchback technique. The etchback technique utilizes a thick metal layer obtained completely by evaporation or by a combination of a thin evaporated layer and a thick plated layer as shown in Fig. 12-5-1(b). A thin photoresist layer is used as a mask to define the circuit pattern. Finally, the unwanted areas of the metal are etched away. This technique results in thicker conductors than the plate-through technique.

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Assignment: 1

Write a program in matlab/C to compute the characteristic impedance Z0 of a microstrip line with the following parameters: epsilon(r)=4.4, h=1.6mm, metal thickness t=4 micron, width of microstrip line w=3mm

Materials

List the basic materials for MMICs.

List the basic characteristics required for an ideal substrate material.

List the basic properties provided by ideal conductor, dielectric, and resistive materials used in MMICs.

MMIC Growth

Describe the MMIC techniques.

Explain the photoresist process.

MOSFET Fabrication

Describe the basic fabrication processes for MOSFETs.

Explain the NMOS growth.

Analyze the CMOS formation.

Describe the memory construction.

Thin-Film Formation

- Describe the resistor-film growth.
- Explain the inductor-film formation.
- Discuss the capacitor-film development.

Hybrid MMICs

- Discuss the discrete, integrated, and monolithic microwave integrated circuits.
- Analyze the hybrid MMICs.
- Describe the hybrid IC techniques.