VLSI Design (BEC-41)
(Unit-2, Lecture-8)

Presented By:

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MOS Combinational Circuit

Different Logic Families

Static CMOS Design

- Complementary CMOS
- Ratioed Logic
- Pass-Transistor Logic

Dynamic CMOS Design

- Domino logic
- NORA logic
- Zipper CMOS Circuits

MOS Combinational Circuit

Complementary CMOS

- The complementary CMOS circuit style falls under a broad class of logic circuits called static circuits in which at every point in time (except during the switching transients), each gate output is connected to either V_{DD} or V_{SS} via a low-resistance path.
- Also, the outputs of the gates assume at all times the value of the Boolean function implemented by the circuit (ignoring, once again, the transient effects during switching periods).
- A static CMOS gate is a combination of two networks, called the pull-up network (PUN) and the pull-down network(PDN). The figure shows a generic N input logic gate where all inputs are distributed to both the pull-up and pull-down networks.

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Complementary CMOS

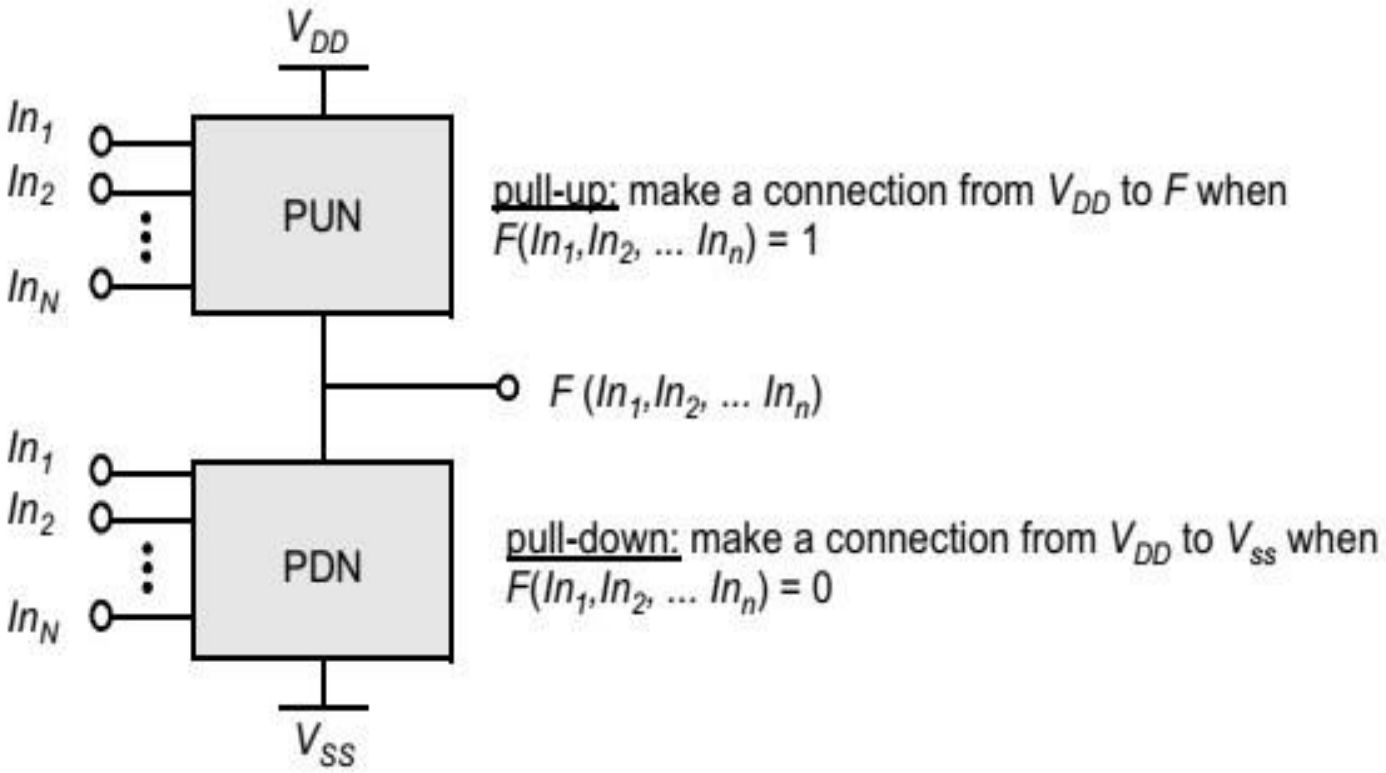

Fig. Complementary logic gate as a combination of a PUN (pull-up network) and a PDN (pull-down network)

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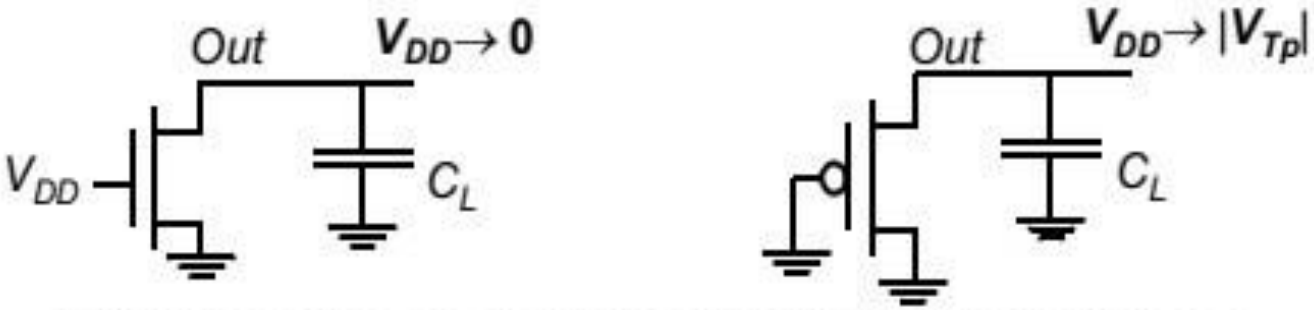
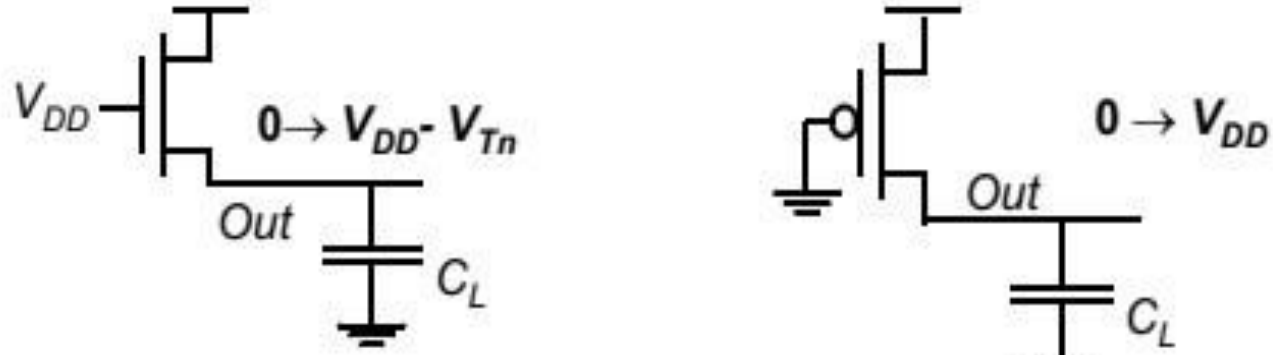


(a) pulling down a node using NMOS and PMOS switches



(b) pulling down a node using NMOS and PMOS switches

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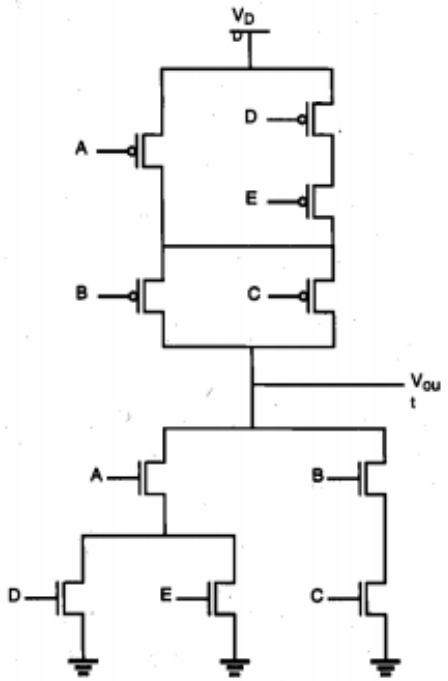
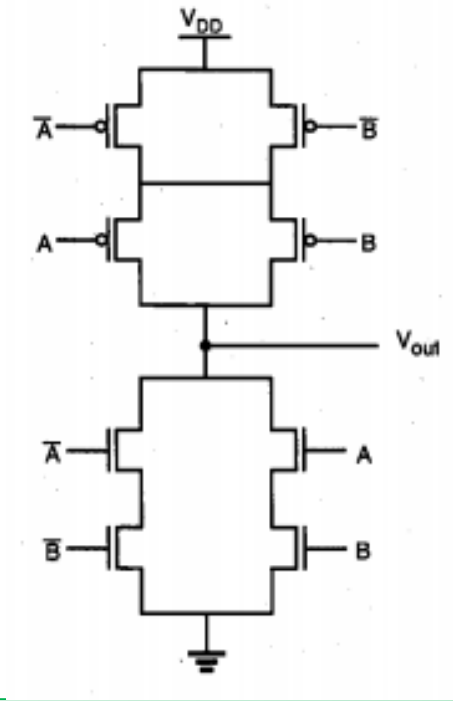
Complementary CMOS

- Consider the following Boolean function as an examples:

$$Z=\overline{A(D+E)+BC} \qquad V_{OUT}=\overline{AB+\overline{A}\overline{B}}$$





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Ratioed Logic

- Ratioed logic is an attempt to reduce the number of transistors required to implement a given logic function, at the cost of reduced robustness and extra power dissipation.
- The purpose of the PUN in complementary CMOS is to provide a conditional path between VDD and the output when the PDN is turned off.
- In ratioed logic, the entire PUN is replaced with a single unconditional load device that pulls up the output for a high output.
- Instead of a combination of active pull-down and pull-up networks, such a gate consists of an NMOS pull-down network that realizes the logic function, and a simple load device.

MOS Combinational Circuit

Ratioed Logic

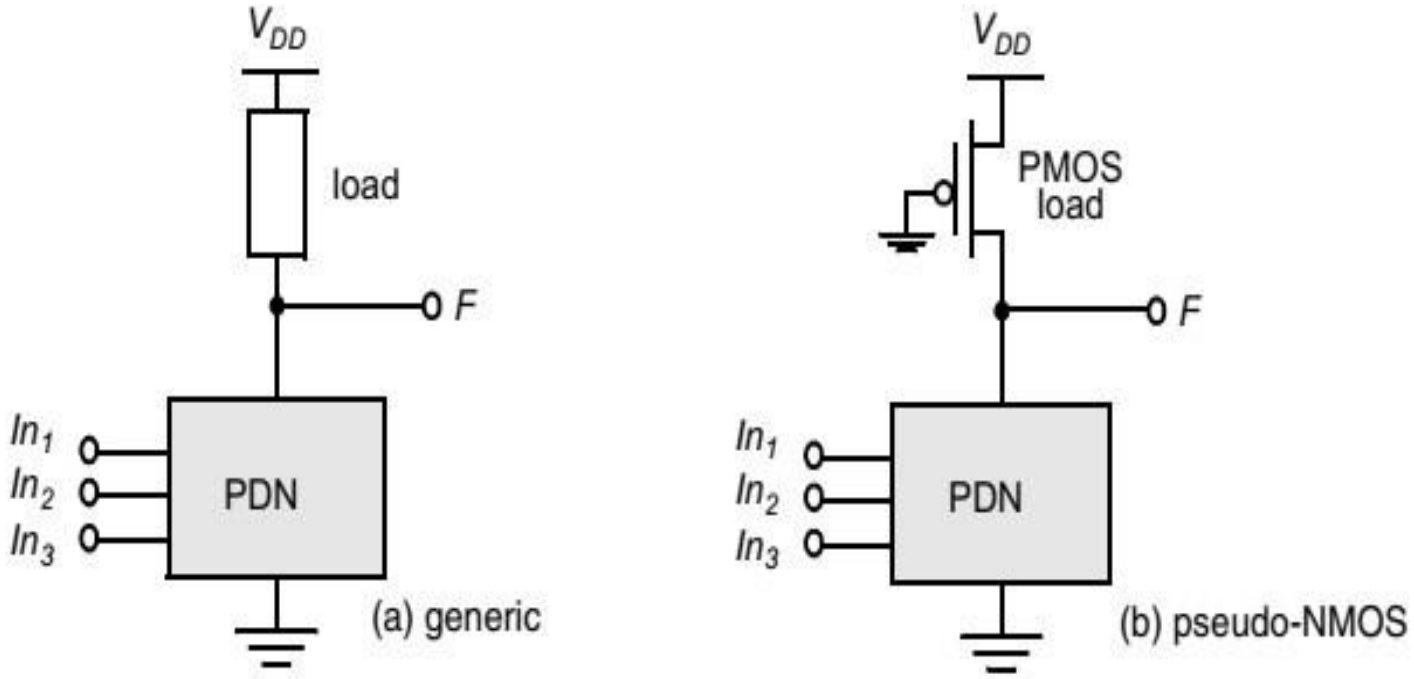

Fig. Ratioed logic gate.

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Ratioed Logic

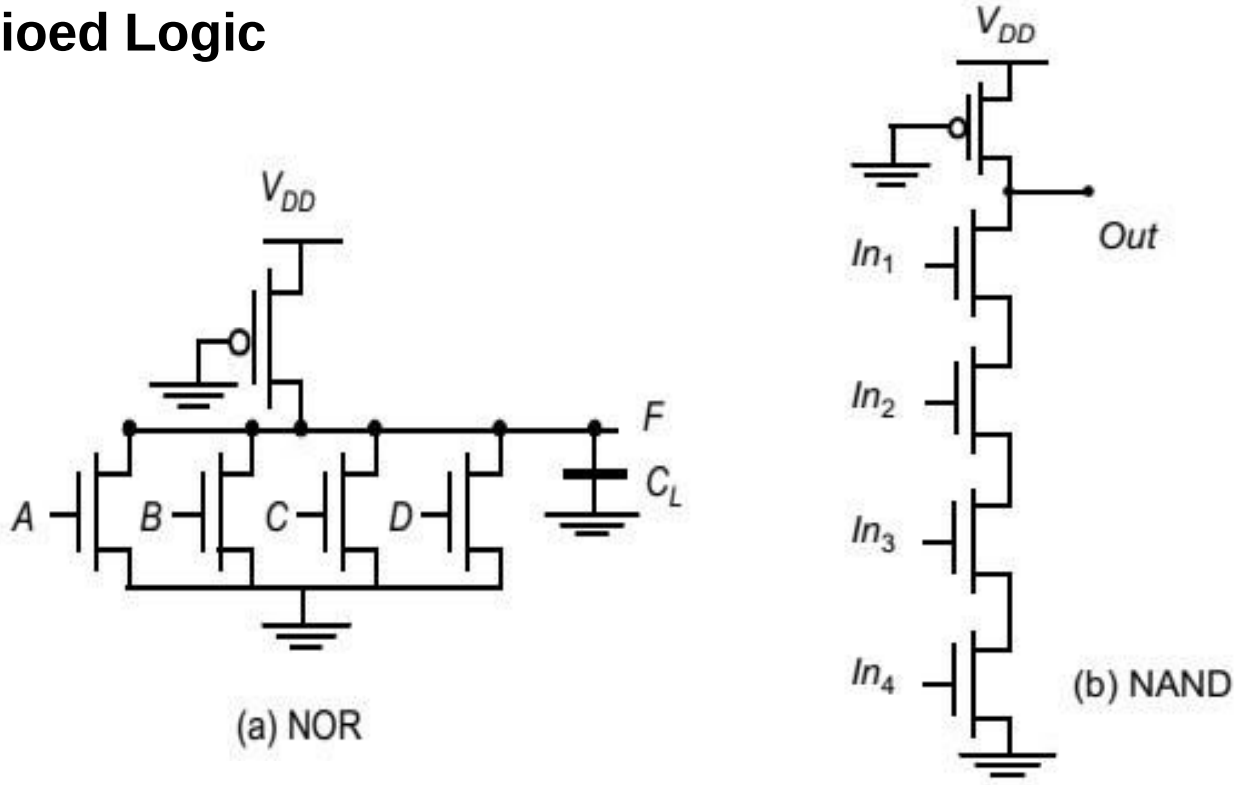
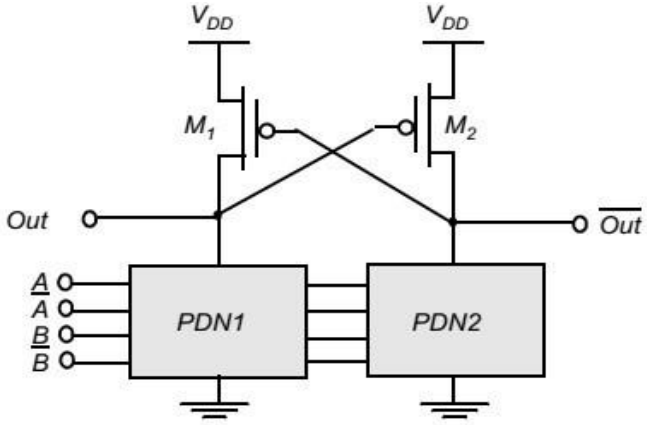


Fig.. Four-input pseudo-NMOS NOR and NAND gates

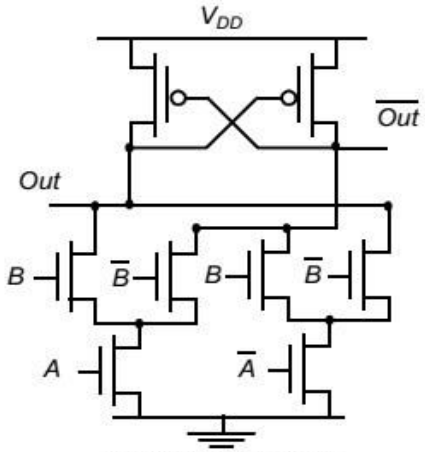
MOS Combinational Circuit

DCVSL logic gate

- To create a ratioed logic style that completely eliminates static currents and provides rail-to-rail swing. Such a gate combines two concepts: differential logic and positive feedback.
- A differential gate requires that each input is provided in complementary format, and produces complementary outputs in turn.
- The feedback mechanism ensures that the load device is turned off when not needed. Example of such a logic family, called Differential Cascode Voltage Switch Logic (or DCVSL).



(a) Basic principle



(b) XOR-XNOR gate