7.5 MOSFET [5]

Recall that the reverse bias of the gate is varied to deplete the channel in JFETs. This type of operation is called depletion-mode operation. A depletion-type device is a device that uses an input voltage to reduce the size of the channel to control the amount of current. An enhancement-type device is a device that uses an input voltage to increase the size of the channel to control the amount of current. JFETs can operate only in depletion mode. There are two types of MOSFETS: depletion-type MOSFETs or D-MOSFETs, and enhancement-type MOSFETs, or E-MOSFETs. There are two types of channel: n-channel and p-channel. We will use the n-channel MOSFETs to describe the basic operation, as shown in Figure 7.29, and 7.30. The p-channel MOSFETs is the same, except the voltage polarities are opposite those of the n-channel.

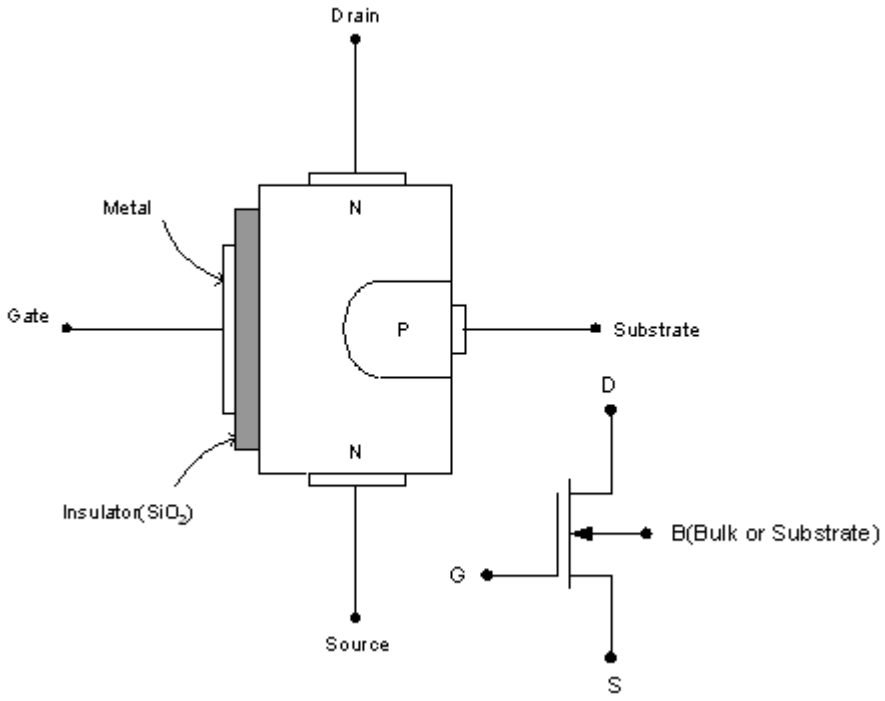


Figure 7.29 N-Channel depletion-type MOSFET

Here,

- The channel already exists.
- An input voltage to the gate will increase or decrease the channel size.

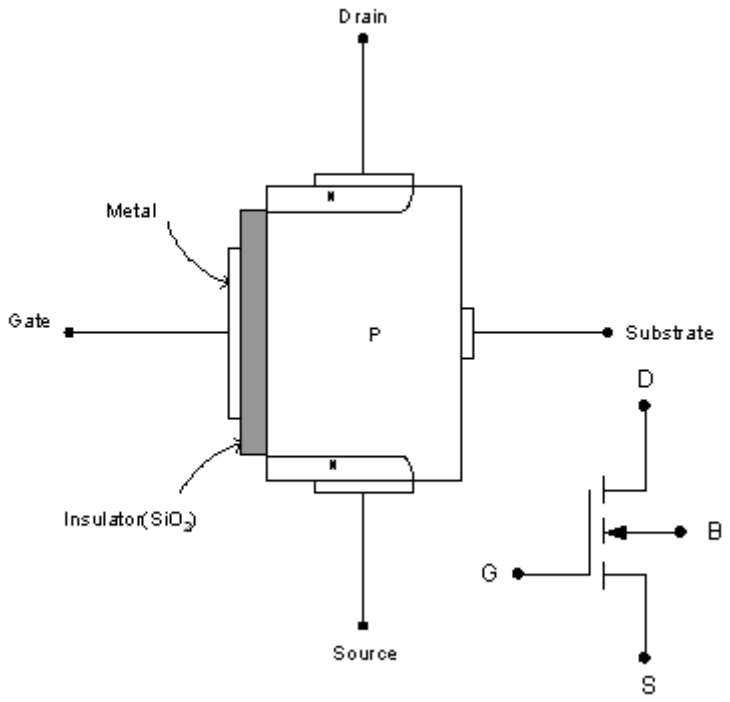


Figure 7.30 N-Channel enhancement-type MOSFET(NMOS)

Here,

- The device has no channel.
- An input voltage to the gate will form a channel.

7.6 Depletion MOSFET (D-MOSFET) [5]

The first type of MOSFET is the depletion MOSFET (D-MOSFET), and Figure 7.31 illustrates its basic structure. The drain and source are diffused into the substrate material and then connected by a narrow channel adjacent to the insulated gate. Both n-channel and p-channel devices are shown in the figure. We will use the n-channel device to describe the basic operation. The p-channel operation is the same, except the voltage polarities are opposite those of the n-channel.

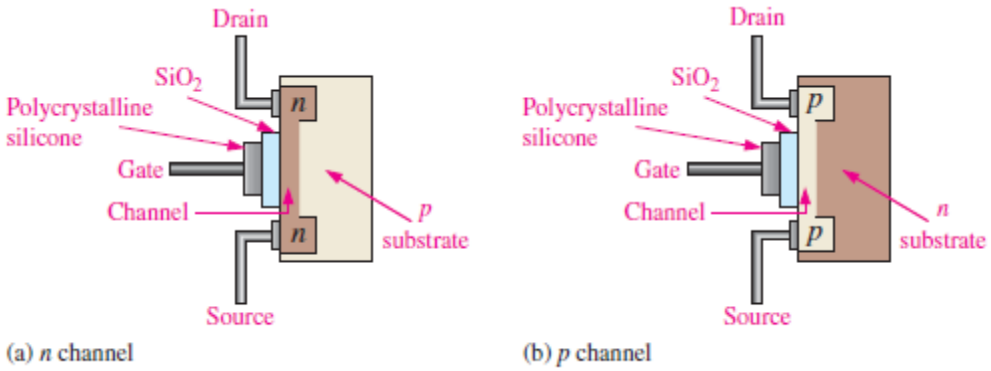


Figure 7.31 Representation of the basic structure of D-MOSFETs. [5]

The D-MOSFET can be operated in either of two modes—the depletion mode or the enhancement mode — and is sometimes called a depletion/enhancement MOSFET. Since the gate is insulated from the channel, either a positive or a negative gate voltage can be applied. The n-channel MOSFET operates in the depletion mode when a negative gate-to-source voltage is applied and in the enhancement mode when a positive gate-to-source voltage is applied. These devices are generally operated in the depletion mode.

Depletion Mode:

Visualize the gate as one plate of a parallel-plate capacitor and the channel as the other plate. The silicon dioxide insulating layer is the dielectric. With a negative gate voltage, the negative charges on the gate repel conduction electrons from the channel, leaving positive ions in their place. Thereby, the n channel is depleted of some of its electrons, thus decreasing the channel conductivity. The greater the negative voltage on the gate, the greater the depletion of n-channel electrons. At a sufficiently negative gate-to-source voltage, $V_{GS(off)}$, the channel is totally depleted and the drain current is zero. This depletion mode is illustrated in Figure 7.32 (a). Like the n-channel JFET, the n-channel D-MOSFET conducts drain current for gate-to-source voltages between $V_{GS(off)}$ and zero. In addition, the D-MOSFET conducts for values of V_{GS} above zero.

Enhancement Mode:

With a positive gate voltage, more conduction electrons are attracted into the channel, thus increasing (enhancing) the channel conductivity, as illustrated in Figure 7.32 (b).

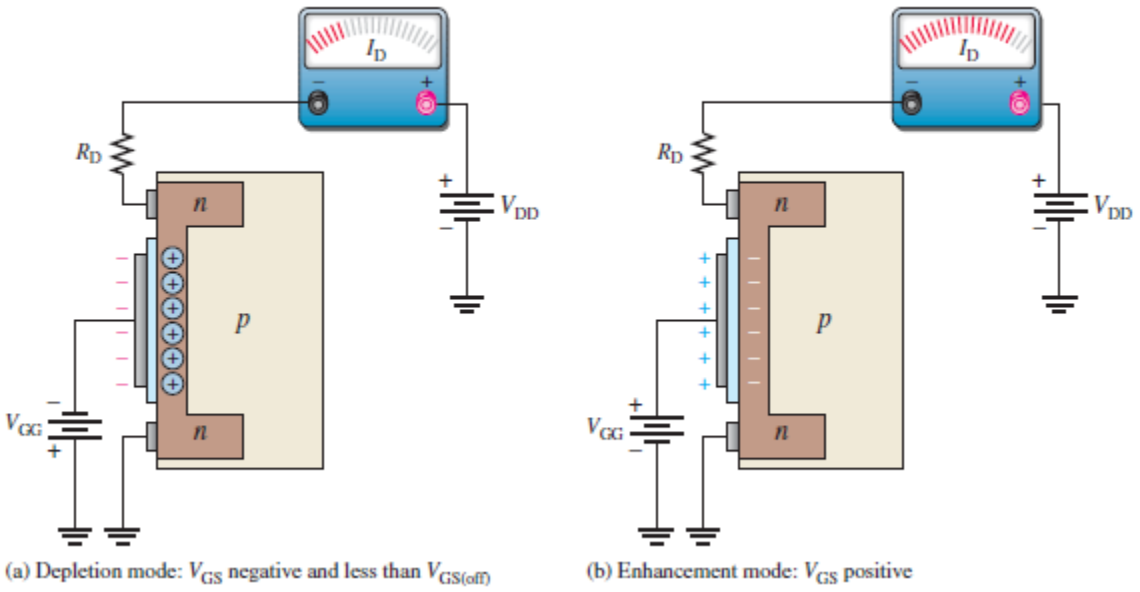


Figure 7.32 Operation of n-channel D-MOSFET. [5]

D-MOSFET Symbols:

The schematic symbols for both the n-channel and the p channel depletion MOSFETs are shown in Figure 7.33. The substrate, indicated by the arrow, is normally (but not always) connected internally to the source.

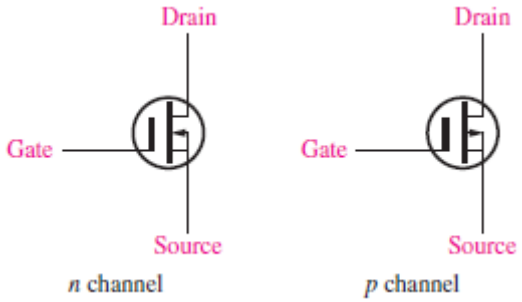
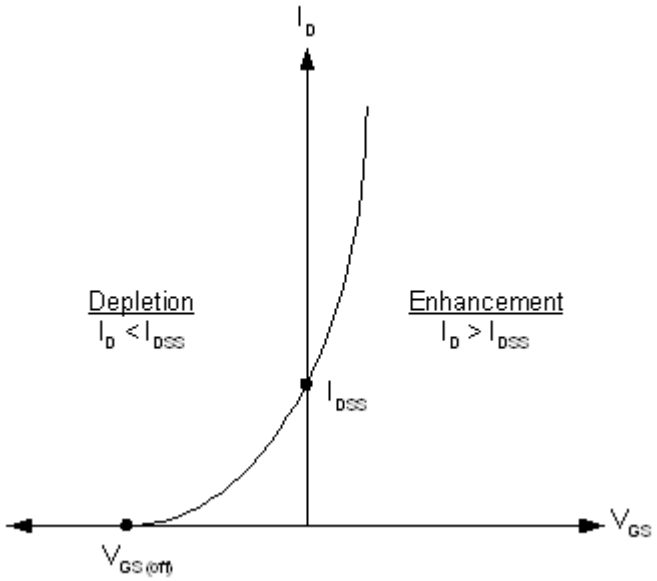


Figure 7.33 D-MOSFET schematic symbols. [5]

D-MOSFET Transfer Characteristic:

The D-MOSFET has the same transconductance curve and equation as the JFET.



$$I_D = I_{DSS}(1-\frac{V_{GS}}{V_{GS(off)}})^2$$

Figure 7.34 Transconductance curve of D-MOSFET.

Example 11: For a certain D-MOSFET, I_{DSS} = 10 mA and $V_{GS(off)}$ = – 8 V. (a) Calculate I_D at V_{GS} = – 3 V. (b) Calculate I_D at V_{GS} = +3 V.

Solution:

The device has a negative $V_{GS(off)}$; therefore, it is an n-channel D-MOSFET.

(a) at $V_{GS} = -3V$

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_{GS(off)}}\right)^2 = (10\text{ mA})\left[1-\left(\frac{-3\text{ V}}{-8\text{ V}}\right)\right]^2 = 3.91\text{ mA}$$

(b) at $V_{GS} = +3V$

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_{GS(off)}}\right)^2 = (10\text{ mA})\left[1-\left(\frac{3\text{ V}}{-8\text{ V}}\right)\right]^2 = 18.9\text{ mA}$$

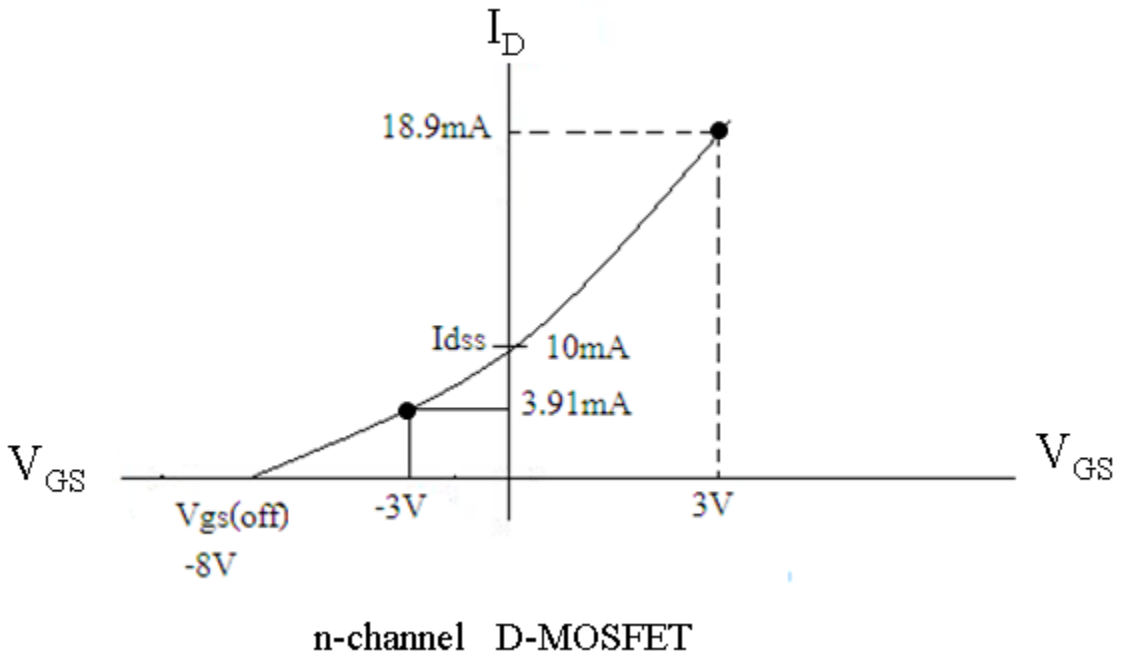


Figure 7.35 For Example 11.

Example 12: For a certain D-MOSFET, I_{DSS} = 18 mA and $V_{GS(off)}$ = +10 V. (a) Is this an n-channel or p-channel? (b) Calculate I_D at V_{GS} = +4 V. (c) Calculate I_D at V_{GS} = -4 V.

Solution:

(a) The device has a positive $V_{GS(off)}$. Therefore, it is a p-channel D-MOSFET.

(b) at $V_{GS} = +4V$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 = (18\text{ mA})\left[1 - \left(\frac{4\text{ V}}{10\text{ V}}\right)\right]^2 = 6.48\text{ mA}$$

(c) at $V_{GS} = -4V$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 = (18\text{ mA})\left[1 - \left(\frac{-4\text{ V}}{10\text{ V}}\right)\right]^2 = 35.28\text{ mA}$$

7.7 D-MOSFET Biasing Circuits [2]

Recall that D-MOSFETs can be operated with either positive or negative values of V_{GS}. A simple bias method is to set V_{GS} = 0 V. A MOSFET with zero bias is shown is Figure 7.36.

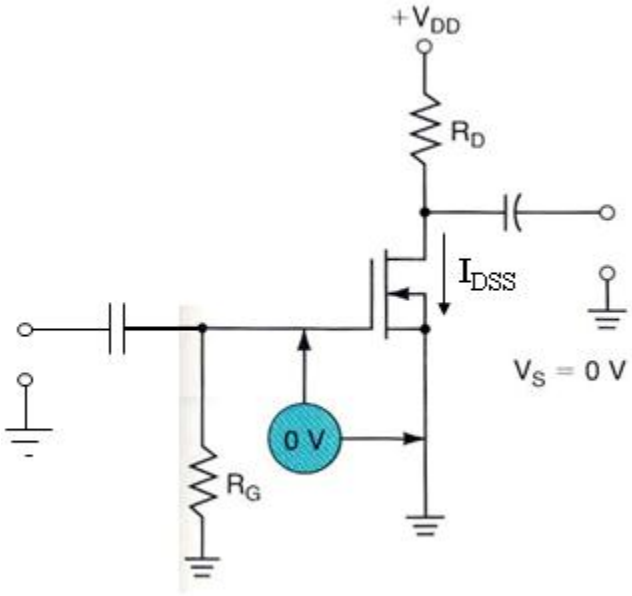


Figure 7.36 A zero-biased D-MOSFET. [2]

The drain-to-source voltage is expressed as:

$$V_{DS} = V_{DD} - I_{DSS}R_D$$

Example 13: Determine the drain-to-source in the circuit of figure 19. Assume $V_{GS(off)}$ = -8 V, I_{DSS} = 12 mA, V_{DD} = 18 V, R_D = 620 Ω and R_G = 10 M Ω.

Solution:

$$\begin{aligned} V_{DS} &= V_{DD} - I_{DSS}R_D \\ &= 18 - (12\text{ mA})(620\,\Omega) \\ &= 10.56\text{ V} \end{aligned}$$

7.8 Enhancement MOSFET (E-MOSFET) [5]

The E-MOSFET operates only in the enhancement mode and has no depletion mode. It differs in construction from the D-MOSFET in that it has no structural channel. Notice in Figure 7.37(a) that the substrate extends completely to the SiO_2 layer. For an n-channel device, a positive gate voltage above a threshold value induces a channel by creating a thin layer of negative charges in the substrate region adjacent to the SiO_2 layer, as shown in Figure 7.37(b). The conductivity of the channel is enhanced by increasing the gate-to-source voltage and thus pulling more electrons into the channel area. For any gate voltage below the threshold value, there is no channel.

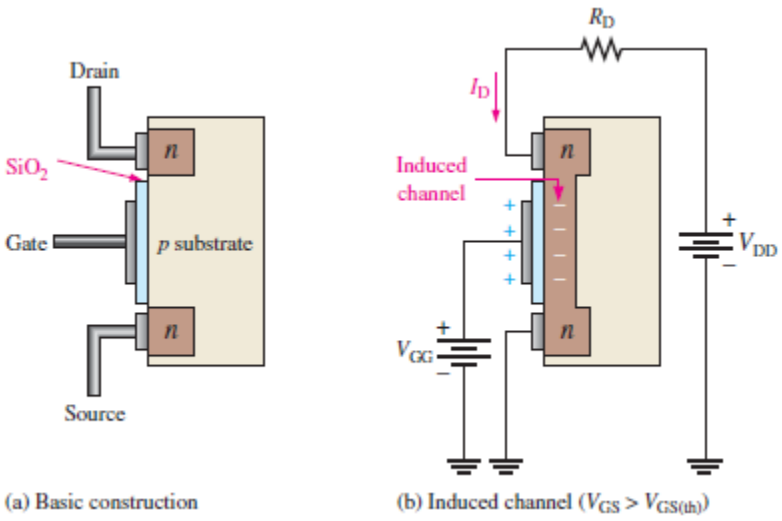


Figure 7.37 The basic E-MOSFET construction and operation (n-channel). [5]

The schematic symbols for the n-channel and p-channel E-MOSFETs are shown in Figure 7.38. The broken lines symbolize the absence of a physical channel. An inward-pointing substrate arrow is for n channel, and an outward-pointing arrow is for p channel.

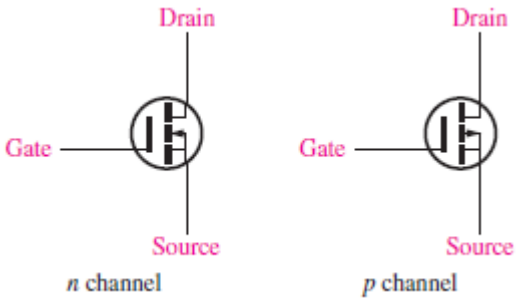


Figure 7.38 E-MOSFET symbols. [5]

E-MOSFET Transfer Characteristic:

The E-MOSFET uses only channel enhancement. Therefore, an n-channel device requires a positive gate-to-source voltage, and a p-channel device requires a negative gate-to-source voltage. Figure 7.39 shows the general transfer characteristic curves for both types of E-MOSFETs. As you can see, there is no drain current when $V_{GS} = 0$. Therefore, the E-MOSFET does not have a significant I_{DSS} parameter, as do the JFET and the D-MOSFET. Notice also that there is ideally no drain current until V_{GS} reaches a certain nonzero value called the threshold voltage, $V_{GS(th)}$.

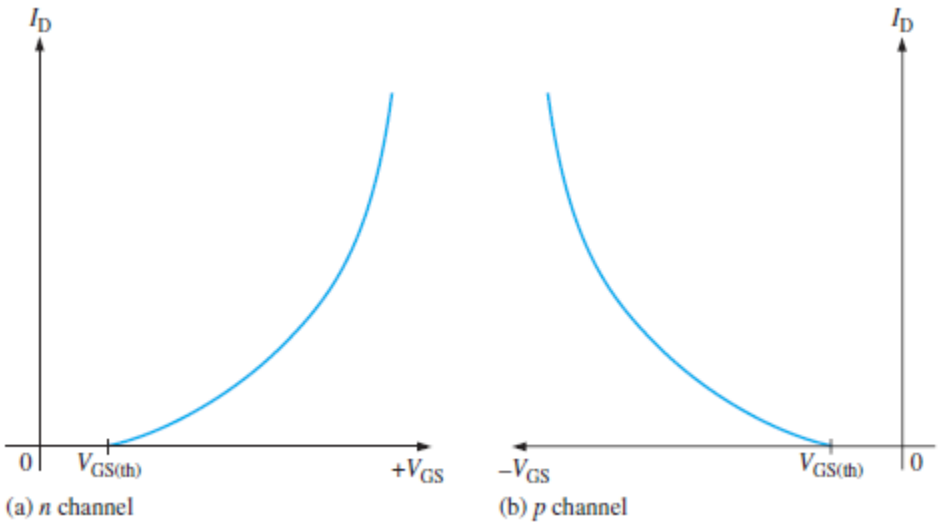


Figure 7.39 E-MOSFET general transfer characteristic curves. [5]

The value of I_D at a given value of V_{GS}, can be determined by

$$I_D = k\left(V_{GS} - V_{GS(th)}\right)^2$$

$$\text{where} \quad k = \frac{I_{D(on)}}{\left(V_{GS(on)} - V_{GS(th)}\right)^2}$$

Example 14: For a 2N7008 E-MOSFET with $I_{D(on)}$ = 500 mA at $V_{GS(on)}$ = 10 V and $V_{GS(th)}$ = 1 V. Determine the drain current for V_{GS} = 5 V.

Solution:

$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(th)})^2} = \frac{500\text{mA}}{(10\text{ V} - 1\text{ V})^2} = 6.17\text{ mA/V}^2$$

Next, using the value of k, calculate I_D for V_{GS} = 5V

$$I_D = k(V_{GS} - V_{GS(th)})^2 = (6.17\text{ mA/V}^2)(5\text{ V} - 1\text{ V})^2 = 98.7\text{ mA}$$

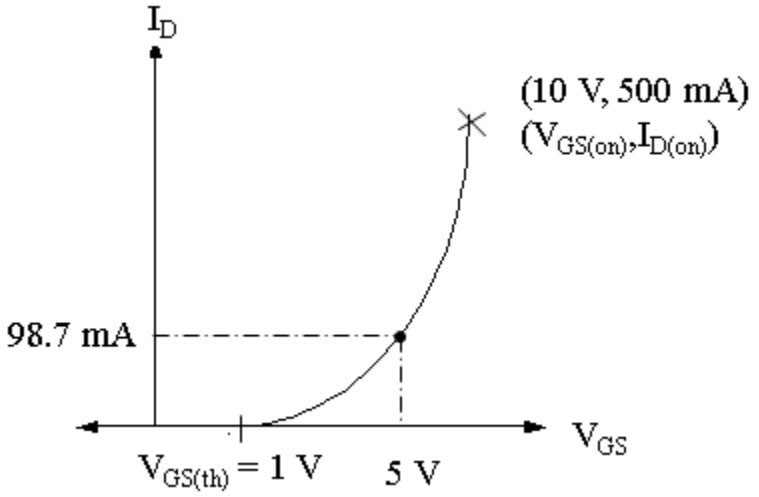


Figure 7.40 For Example 14.

7.9 E-MOSFET Biasing Circuits [5]

Recall that D-MOSFETs must have a V_{GS} greater than the threshold value, $V_{GS(th)}$, so zero bias cannot be used. Figure 7.41 shows voltage-divider bias circuit of an E-MOSFET. In the voltage-divider, the purpose is to make the gate voltage more positive than the source by an amount exceeding $V_{GS(th)}$. Equations for the analysis of the voltage-divider bias become:

$$V_{GS} = \left(\frac{R_2}{R_1 + R_2}\right)V_{DD}, \qquad V_{DS} = V_{DD} - I_D R_D$$

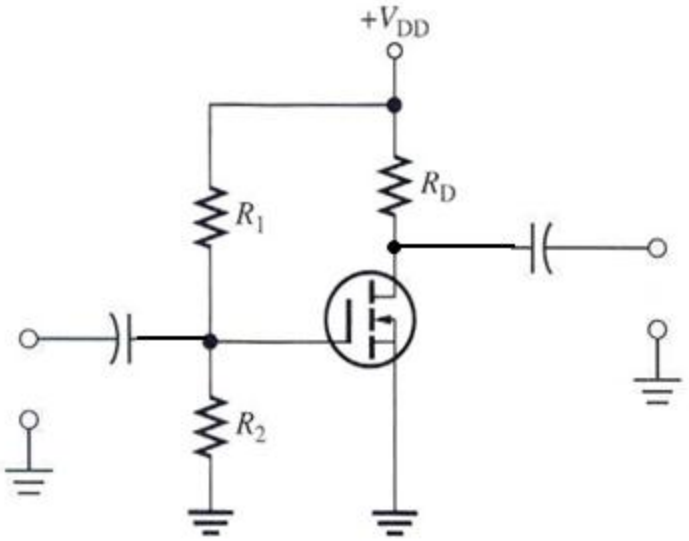


Figure 7.41 Voltage-divider bias of n-channel E-MOSFET. [5]

Figure 7.42 shows drain-feedback bias circuit of an n-channel E-MOSFET. In the drain-feedback bias circuit, the purpose is also to make the gate voltage more positive than the source by an amount exceeding $V_{GS(th)}$. In the drain-feedback bias circuit, there is a negligible gate current and, therefore, no voltage drop across R_G. This makes $V_{GS} = V_{DS}$

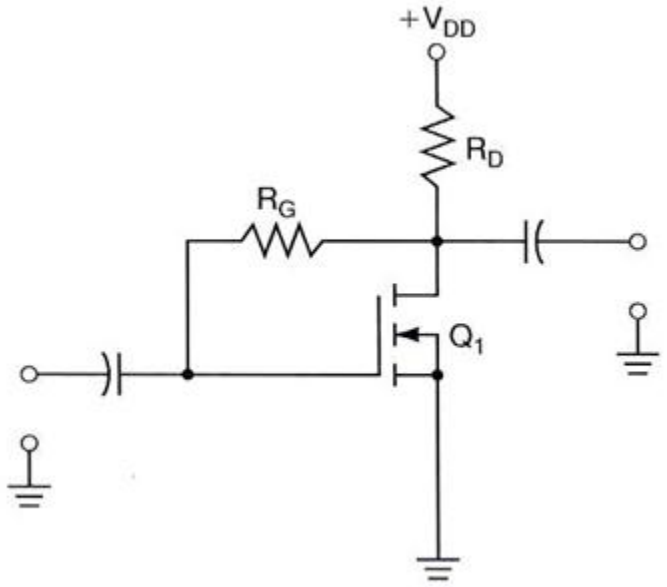


Figure 7.42 Drain-feedback bias of n-channel E-MOSFET. [5]

Example 15: Determine V_{GS} and V_{DS} for the E-MOSFET circuit. Assume this MOSFET has $I_{D(on)}$ = 200 mA at V_{GS} = 4 V and $V_{GS(th)}$ = 2 V.

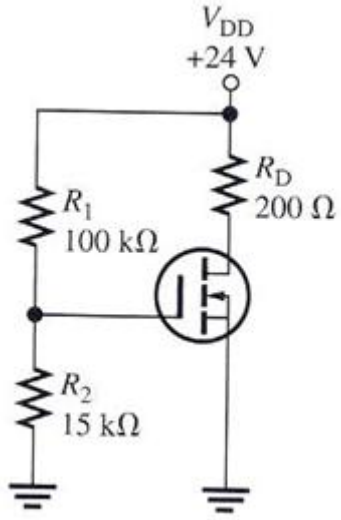


Figure 7.43 For Example 15. [5]

Solution:

$$V_{GS} = \left(\frac{R_2}{R_1 + R_2}\right)V_{DD} = \left(\frac{15\ \text{k}\Omega}{15\ \text{k}\Omega + 100\ \text{k}\Omega}\right) \times 24\ \text{V}$$

$$= 3.13\ \text{V}$$

$$k = \frac{I_{D(on)}}{\left(V_{GS(on)} - V_{GS(th)}\right)^2} = \frac{200\ \text{mA}}{(4\ \text{V} - 2\ \text{V})^2} = 50\ \text{mA/V}^2$$

$$I_D = k\left(V_{GS} - V_{GS(th)}\right)^2 = (50\ \text{mA/V}^2)(3.13\ \text{V} - 2\ \text{V})^2 = 63.8\ \text{mA}$$

$$V_{DS} = V_{DD} - I_D R_D = 24 - (63.8\,\text{mA})(200\,\Omega)$$

$$= 11.2\ \text{V}$$

Therefore, Q-point is at I_D = 63.8 mA and V_{GS} = 3.13 V.

Example 16: Determine the amount of drain current for the circuit shown in Figure 7.44. The MOSFET has a $V_{GS(th)} = 3$ V.

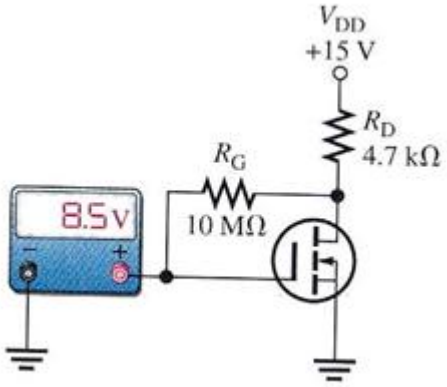


Figure 7.44 For Example 16. [5]

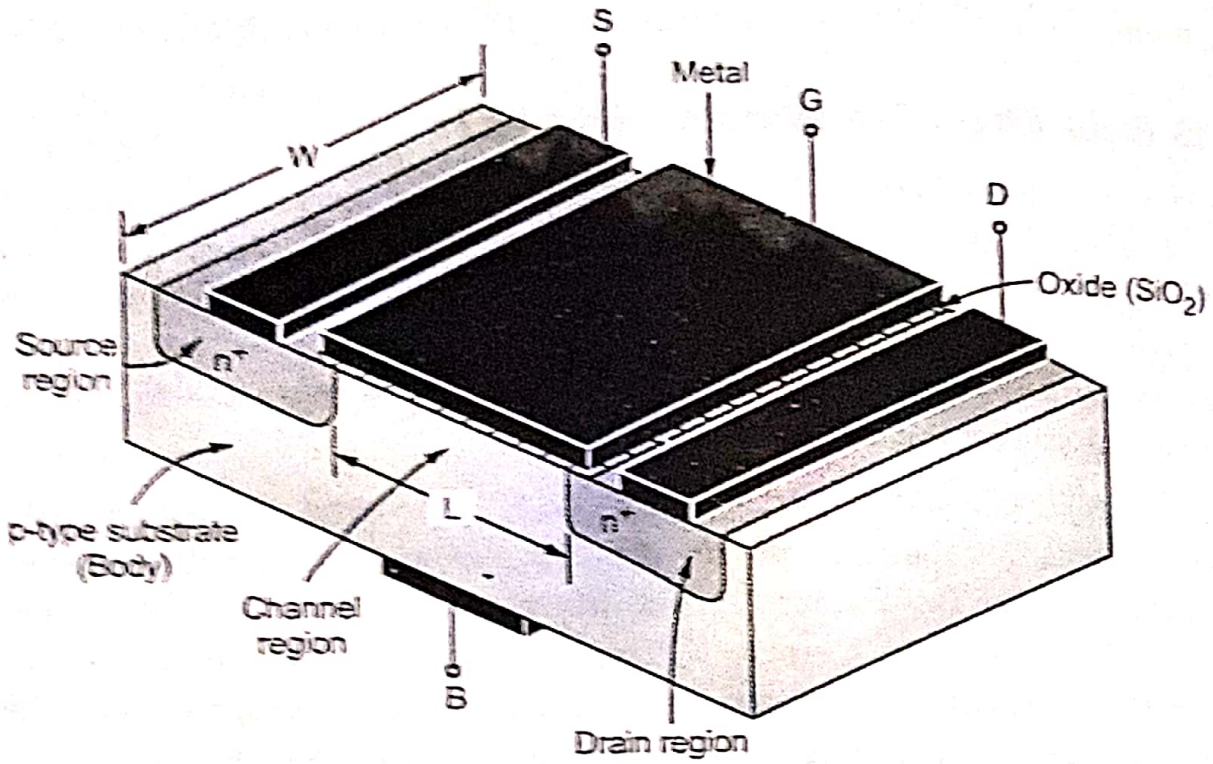
Solution:

The meter indicates $V_{GS} = 8.5$ V

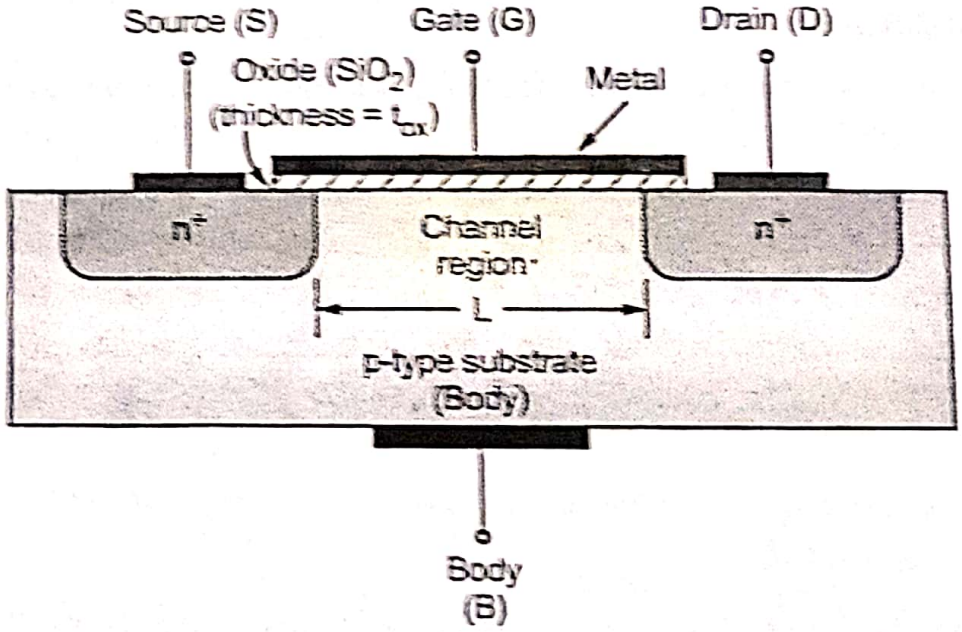
Here, $V_{DS} = V_{GS} = 8.5$ V

Therefore

$$I_D = \frac{V_{DD} - V_{DS}}{R_D} = \frac{15 - 8.5 \text{ V}}{4.7 \text{ k}\Omega} = 1.38 \text{ mA}$$



(a) Perspective view



(b) Cross-sectional view

Fig. 4.8 Physical structure of enhancement-type n-channel MOSFET

As both source and drain regions are of the same type and substrate being of opposite type, MOSFET is basically a symmetrical device, which can be operated w the source and drain interchanged and this will have no effect on the dev characteristics.

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4.6.2 Operation of MOSFET

With no bias voltage applied between gate and source, no drain current can flow as there is no passage for charge particles to flow from source to drain. Hence MOSFET is called **Normally OFF device** when a voltage V_{DS} is applied. In this condition, the resistance of the path between the drain and source is extremely high, of the order of $10^{12}\ \Omega$. To make this device conduct the current between drain and source, a channel for the flow of free charge carriers, is to be created by the application of proper D.C. voltage between gate and source.

We have seen that between the gate, a conducting electrode, and the body of MOSFET, which is a semiconductor; there is an insulator due to SiO_2. This forms a parallel-plate capacitor.

Capacitance of parallel-plate capacitor $= \dfrac{\varepsilon\,(\text{Area})}{\text{width}}$

Then

for oxide capacitance,

$$C = \frac{\varepsilon(\text{Area})}{t_{ox}}$$

where t_{ox} = thickness of oxide coating

Denoting the gate-oxide capacitance per unit area by C_{ox}; we have

$$C_{ox} = \frac{\varepsilon}{t_{ox}}$$ where ε is the permittivity of the insulator used.

Relative permitivity, ε_r, of SiO_2 is 3.9.

Then

$$\varepsilon = \varepsilon_r\,\varepsilon_o = 3.9 \times 8.854 \times 10^{-12}\ \text{F/m}$$

If the thickness of SiO_2 layer is 10 nm; then

$$C_{ox} = \frac{3.9 \times 8.854 \times 10^{-12}}{10 \times 10^{-9}}\ (\text{F/m}^2)$$

$$C_{ox} = 3.453 \times 10^{-3}\ (\text{F/m}^2)$$

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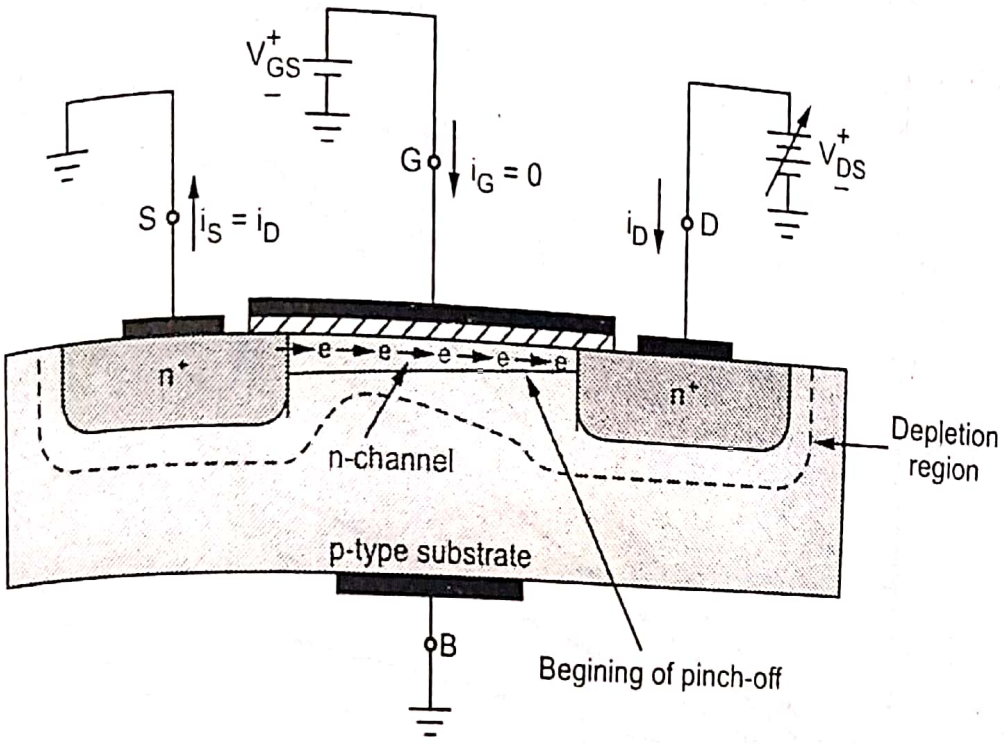

(c) Channel induction with increased V_{DS},

Fig. 4.9 (c)

electrons can go from source to drain through this layer and thus the drain current flows when the drain is made positive with respect to the source. As the channel is formed by the negatively charged electrons, the device is known as **n-channel MOSFET**. The threshold voltage for this device, V_{Th} is positive. The value of V_{Th} is controlled when the device is fabricated.

The magnitude of the drain current, i_D, depends upon the concentration of electrons in the channel which is determined by the magnitude of the voltage V_{GS}.

When $V_{GS} = V_{Th}$, the channel is just induced and the drain current just starts to flow. As V_{GS} exceeds, V_{Th}, more electrons are attracted into the channel and the drain current increases. Thus the current i_D is proportional to $[V_{GS} - V_{Th}]$, when V_{DS} applied is small. The Fig. 4.10, shows a graph of i_D versus V_{DS} for various values of V_{GS}.

It is seen that, when V_{DS} is small, the MOSFET operates as a linear resistance whose value is dependent on V_{GS}. Its value reduces as V_{GS} exceeds V_{Th}.

Thus we see that, a channel has to be created in order to make MOSFET conduct. When V_{GS} is increased above the threshold voltage V_{Th}, the channel enhances, hence the device is called **enhancement type MOSFET.**

Now let us study the situation as V_{DS} is increased. To study this, we will assume that V_{GS} is kept constant at a value greater than V_{Th}.

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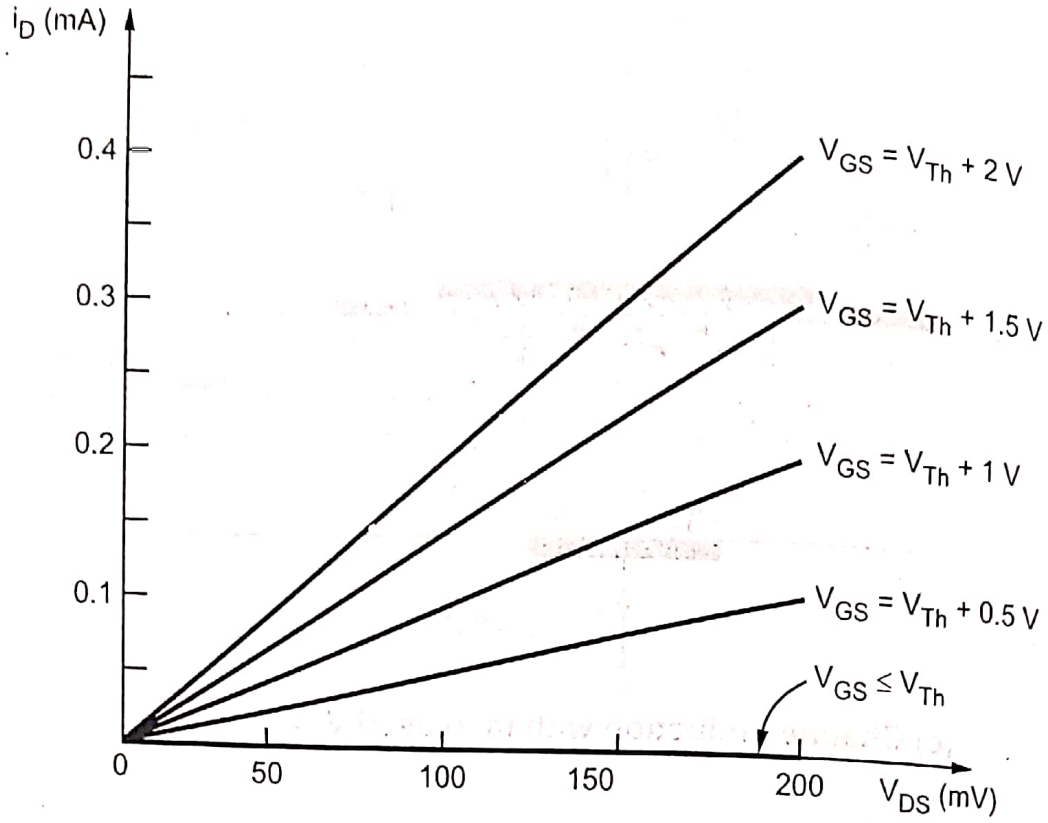

Fig. 4.10 The i_D Vs V_{DS} characteristics of the MOSFET

As we go from source to drain, the voltage (measured w.r.t. source) increases from 0 to V_{DS}. Due to this, channel does not have uniform depth; but the channel becomes tapered, as shown in the Fig. 4.9 (c). As V_{DS} is increased, the channel tapers more and more. The drain current can no more increase with V_{DS} but becomes constant. The volt ampere characteristic is shown in Fig. 4.11.

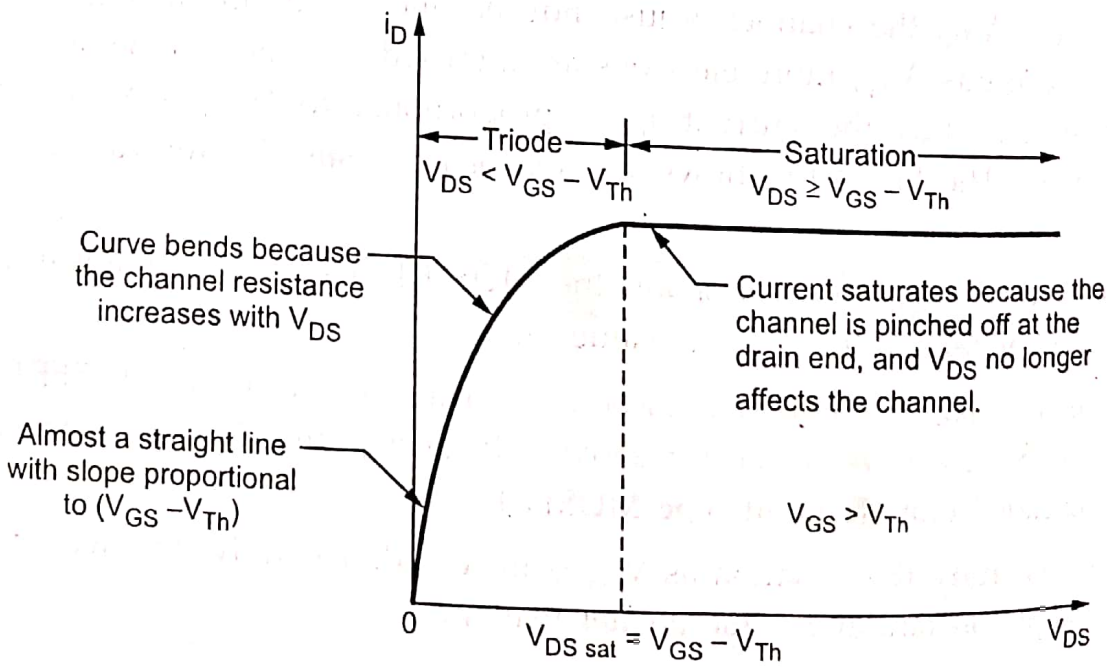

Fig. 4.11 i_D versus V_{DS} characteristics

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The I-V characteristic is seen to be divided into two regions. Triode region and saturation region.

The voltage V_{DS} at which saturation occurs is denoted by $V_{DS\,sat}$ and

$$V_{DS\,sat} = V_{GS} - V_{Th}$$

If V_{DS} is less than $(V_{GS} - V_{Th})$, device operates in triode region, where i_D changes with V_{DS}.

When V_{DS} is equal to or greater than $(V_{GS} - V_{Th})$, device enters saturation region where i_D remains practically constant.

4.6.4 Relationship between i_D and V_{DS}

The mathematical equation for the above I-V characteristic is;

$$i_D = k'_n \frac{W}{L}\left[(V_{GS} - V_{Th})V_{DS} - \frac{1}{2}V_{DS}^2\right] \text{ (Triode region)} \quad \ldots(1)$$

$$i_D = \frac{1}{2}k'_n \frac{W}{L}(V_{GS} - V_{Th})^2 \text{ (saturation region)} \quad \ldots(2)$$

Here, $k'_n = \mu_n C_{ox}$

where μ_n is the mobility of the electrons in the channel and C_{ox} is oxide capacitance per unit area. k'_n has the dimensions of A/V^2. Its value is determined by the process technology used to fabricate the n-channel MOSFET. It is also called the **process transconductance parameter.**

Equation (1) and (2) indicate that the drain current is proportional to the ratio of the channel width W to the channel length L. This ratio is called **aspect ratio** of the MOSFET.

The conductance of the channel is proportional to the excess gate voltage, $[V_{GS} - V_{Th}]$, also called the **effective voltage** or the **overdrive voltage**. The current i_D is controlled by this overdrive voltage.

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4.6.5 The p-Channel MOSFET

The p-channel enhancement-type MOSFET (PMOS) uses n-type substrate with both the drain and the source p regions. The principle of operation of this device is same as that of the n-channel device, the only difference being that for PMOS, V_{GS} and V_{DS} are negative, so also V_{Th}. In this device, the drain current enters the source terminal and leaves out from the drain.

NMOS devices are most widely used than PMOS for the following reasons :

1) NMOS devices can be made smaller, thus reducing IC chip size.
2) NMOS devices operate faster.
3) NMOS devices require smaller supply voltage.

However PMOS devices are to be studied as

1) They are still used in discrete circuit design.
2) Both PMOS and NMOS transistors are used in complementary MOS or CMOS circuits.

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4.7 Current - Voltage Characteristics

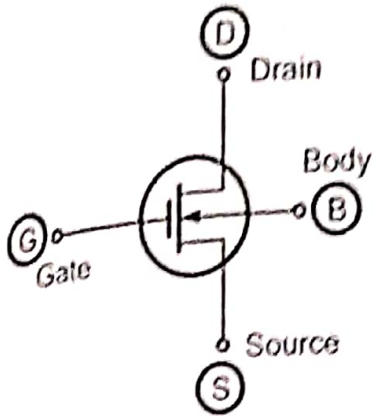


Fig. 4.12

The circuit symbol for the n-channel enhancement type MOSFET is shown in the Fig. 4.12.

The gate, insulated from the body of the device is reflected in the symbol. The arrowhead is on the line showing the body or substrate electrode. For the n-channel device, this arrowhead is inwards.

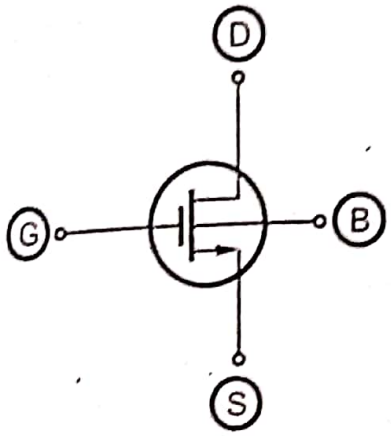


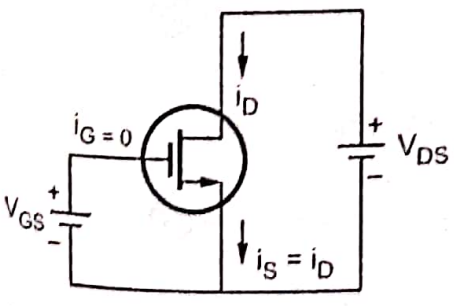
Fig. 4.13

Another symbol used for n-channel MOSFET has arrowhead on the source terminal, as shown in the Fig. 4.13.

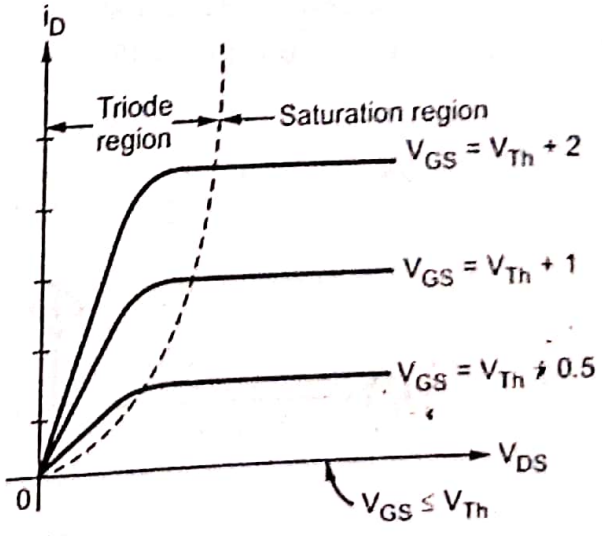
This arrowhead indicates the conventional direction of the drain current flow in the device, which is from drain to source.

4.7.1 The i_D - V_{Ds} Characteristics

The Fig. 4.14 shows an n-channel enhancement type MOSFET to which DC voltages V_{DS} and V_{GS} are applied. The static i_D – V_{DS} characteristics are shown, which form a set of curves plotted keeping V_{GS} constant for each curve.



(a) Circuit



(b) i_D Vs V_{DS} characteristics

Fig. 4.14

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The characteristic is divided in three regions : cutoff region, triode region, and saturation region.

If MOSFET is to be used as an amplifier, it operates in saturation region. To make it work as a switch, it is operated in cutoff and triode regions.

(1) The device cuts off if

$$V_{GS} < V_{Th}$$

(2) The operation in triode region is obtained when

$$V_{DS} < V_{GS} - V_{Th}$$

(3) The operation in saturation region is obtained when

$$V_{GS} \geq V_{Th}$$

and

$$V_{DS} \geq V_{GS} - V_{Th}$$

The boundary between the triode region and the saturation region is characterized by

$$V_{DS} = V_{GS} - V_{Th}$$

In saturation, the drain current is independent of the drain voltage V_{DS} and is controlled by the gate voltage V_{GS}, as given by the equation.

$$i_D = \frac{1}{2} k'_n \frac{W}{L} [V_{GS} - V_{Th}]^2$$

Thus in saturation, MOSFET is basically a **square-law device.**

As in saturation region, the drain current is nearly constant, hence it behaves as an ideal constant current source. Therefore, an equivalent circuit for MOSFET operating in saturation is as shown in the Fig. 4.15.

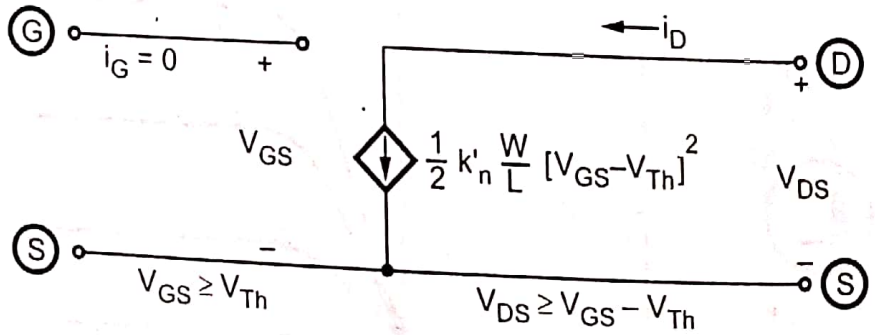

Fig. 4.15

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4.7.2 Characteristics of the p-Channel MOSFET

Similar to NMOSFET, the two circuit symbols used for the p-channel enhancement-type MOSFET are shown in Fig. 4.16.

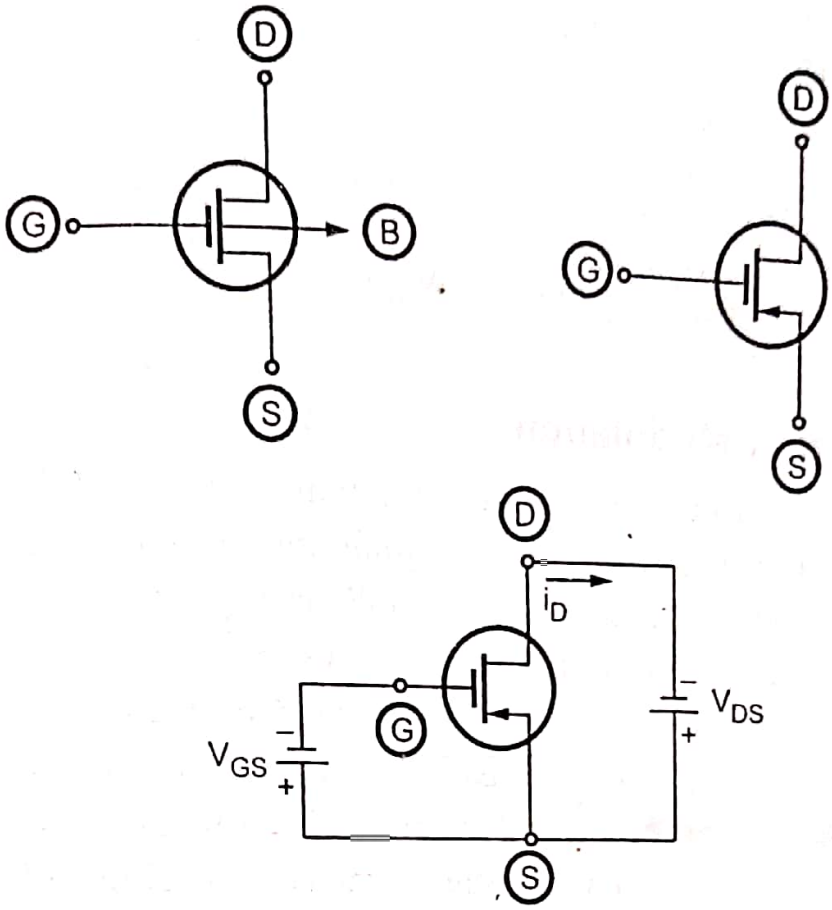

Fig. 4.16

For the normal operation, polarities of the voltages V_{GS} and V_{DS} to be applied are also shown. For the p-channel MOSFET, the threshold voltage V_{Th} is negative. To induce the channel in order that the drain current will flow in the device, we have to apply a gate voltage which is more negative than V_{Th}.

$$V_{GS} \leq V_{Th} \text{ (induced channel)}$$

and apply a drain voltage which is more negative than the source voltage.

Similar to NMOS transistor, the p-channel MOSFET characteristics reveal three regions of operation : cutoff region, triode region, and saturation region.

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Cutoff region is obtained when V_{GS} applied is less negative than V_{Th}.

For operation in triode region,

$$V_{DS} \geq V_{GS} - V_{Th}$$

Then the current i_D in triode region is given by

$$i_D = k'_p \frac{W}{L}\left[(V_{GS} - V_{Th})V_{DS} - \frac{1}{2} V_{DS}^2\right]$$

Here $$k'_p = \mu_p C_{ox}$$

where μ_p is the mobility of the holes.

To operate in saturation,

$$V_{DS} \leq V_{GS} - V_{Th}$$

and

the current i_D is given by

$$i_D = \frac{1}{2} k'_p \frac{W}{L} [V_{GS} - V_{Th}]^2$$

4.7.3 Channel Length Modulation

The Fig. 4.17 shows induced channel at different levels of V_{DS}. In the figure, the thickness of the induced channel layer qualitatively indicates the relative charge density. In Fig. 4.17 (a), applied V_{DS} is small and for this case the relative charge density is constant along the entire channel length. The Fig. 4.17 (b) shows the situation when V_{DS} increases. As the drain voltage increases, the voltage drop across the oxide near the drain terminal decreases, which means that the induced inversion charge density near the drain also decreases. The incremental conductance of the channel at the drain then decreases, which causes the slope of the I_D versus V_{DS} curve to decrease. This effect is shown in the I_D versus curve in the figure.

As V_{DS} increases to the point where the potential difference across the oxide at the drain terminal is equal to V_{Th}, the induced inversion charge density at the drain terminal is zero. This is illustrated in Fig. 4.17 (c). When V_{DS} becomes larger than $V_{DS(sat)}$, the point in the channel at which the inversion charge is just zero moves towards the source terminal. In this case, electrons enter the channel at the source, travel through the channel towards the drain, and then at the point where the charge goes to zero, are injected into the depletion region, where they are swept by the

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E-field to the drain contact. It is observed that as V_{DS} increases beyond $V_{DS(sat)}$ effective channel length decreases, producing the phenomenon called **channel length modulation.**

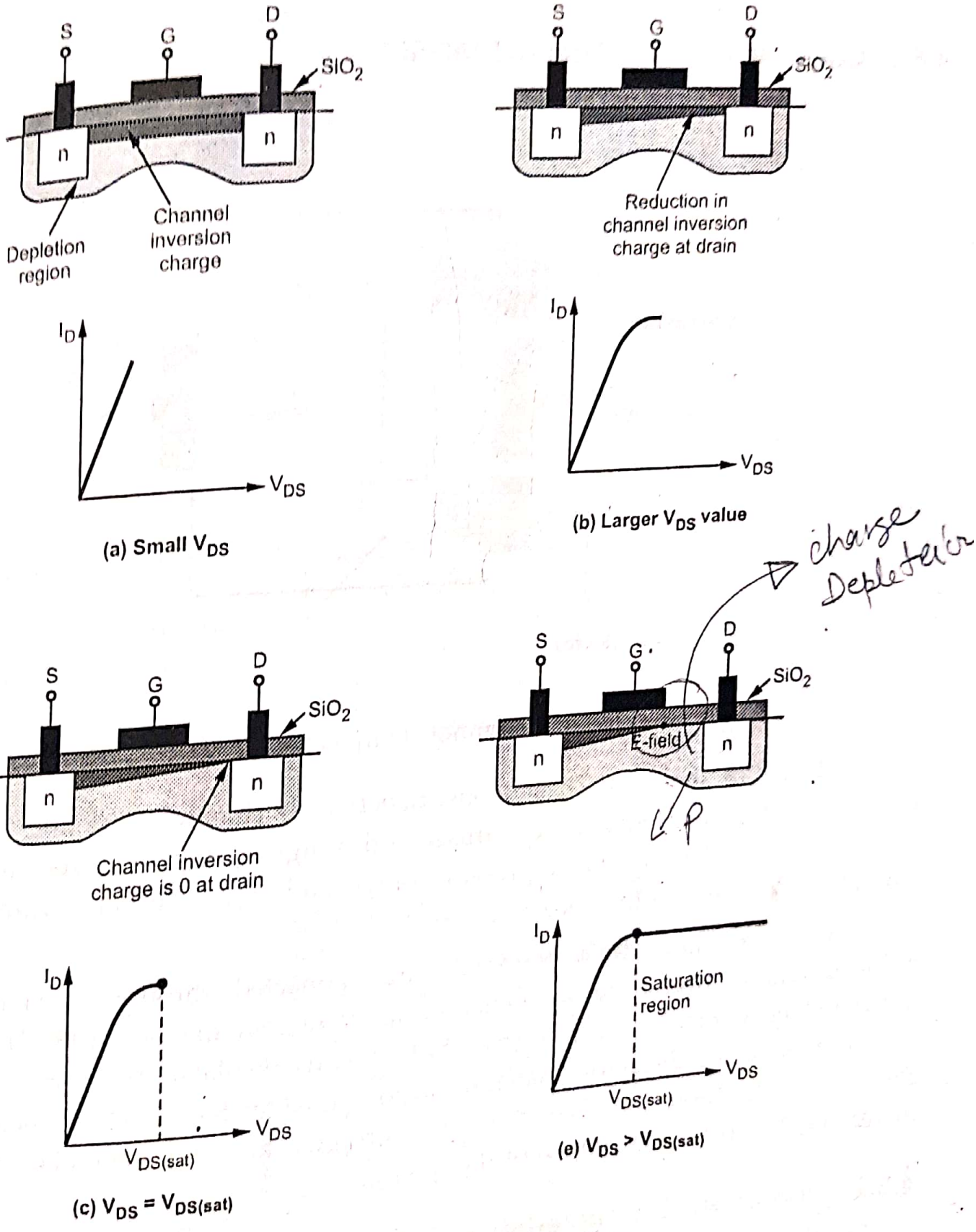

Fig. 4.17 Channel length modulation

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4.10 MOSFET as an Amplifier

As the MOSFET is basically a non-linear device [square-law device], to get linear amplification from such a device, we have to use proper DC biasing so that the device operates at an appropriate V_{GS} and the corresponding drain current I_D. Then the signal voltage to be amplified, v_{gs}, is superimposed on DC bias V_{GS}. When the signal v_{gs} is "small" the corresponding i_D becomes proportional to v_{gs}. This assures linearity in amplification.

The Fig. 4.31 shows the circuit diagram of the most practically used MOSFET amplifier, viz the common-source [CS] amplifier.

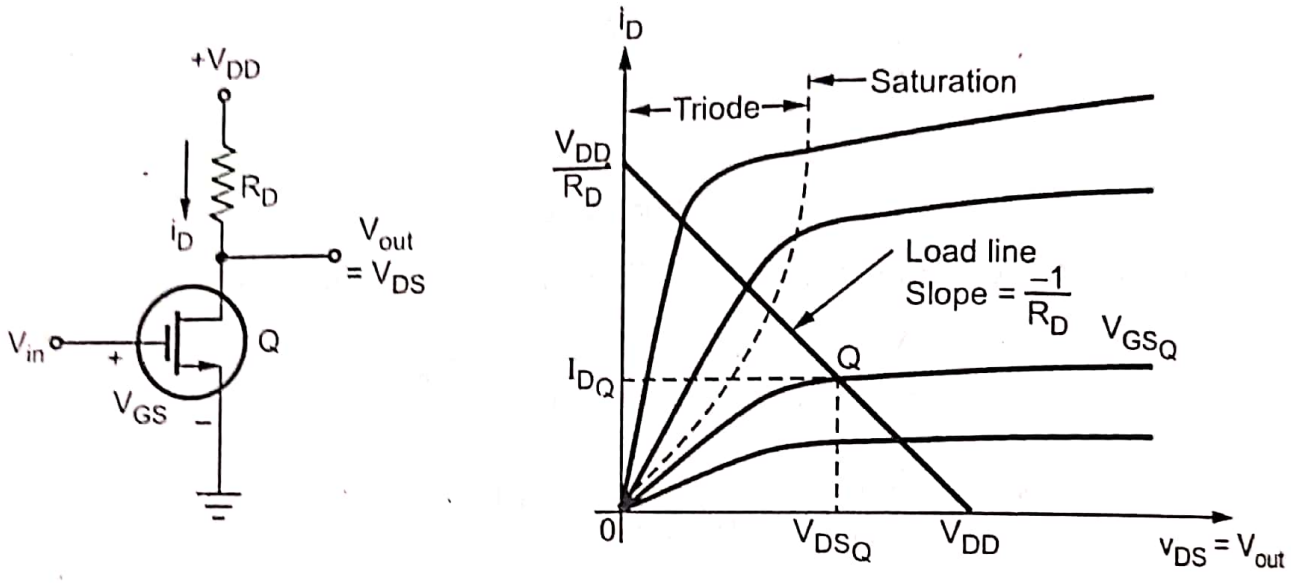

Fig. 4.31

Here, the input is applied between the gate and source and the output is taken between the drain and source. Thus, the source is common between the input and output.

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By KVL

$$V_{DD} = i_D R_D + V_{DS}$$

$$v_{DS} = v_{out} = V_{DD} - i_D R_D$$

$$\therefore \quad i_D = \left[\frac{-1}{R_D}\right] v_{out} + \frac{V_{DD}}{R_D}$$

or

This equation represents a straight line on the $i_D - v_{DS}$ characteristics. The line has the slope $\left[\frac{-1}{R_D}\right]$ hence it is known as the **load line.**

To operate MOSFET as an amplifier it is operated in its saturation region of characteristics. The quiescent operating point is selected to be preferably, the mid-point of the load line. The co-ordinates of the Q-point are $[V_{DSQ}, I_{DQ}]$. The small signal to be amplified is then superimposed on this DC quiescent operating point, Q. The resulting output voltage is proportional to the input signal.

4.11 Biasing in MOS Amplifier Circuits

As seen in previous section, to use MOSFET as an linear amplifier, it should operate in saturation region which is ensured by DC operating quiescent point.

4.11.1 Biasing by Fixing V_{GS}

The most simple way to bias a MOSFET is to fix its gate-to-source voltage V_{GS} as required by the set quiescent operating point. This required DC V_{GS} can be obtained from another suitable DC voltage available in the system, or alternately it can be derived from the power supply voltage V_{DD} using an appropriate resistive voltage divider. However, these methods of biasing are not practically suitable to stabilize the operating point. The reason is as follows :

In saturation region,

$$I_D = \frac{1}{2} [\mu_n C_{ox}] \left(\frac{W}{L}\right) [V_{GS} - V_{Th}]^2$$

Thus values of the threshold voltage, V_{Th}, the oxide capacitance C_{ox}, the transistor aspect ratio $\frac{W}{L}$, vary widely among the devices of the same size and type. This is known as unit-to-unit variation. So if one device is replaced by another of same type, the second device may not be biased properly by the fixed DC V_{GS} used. Further, both V_{Th} and μ_n depend on temperature which make the quiescent drain current I_D temperature dependent.

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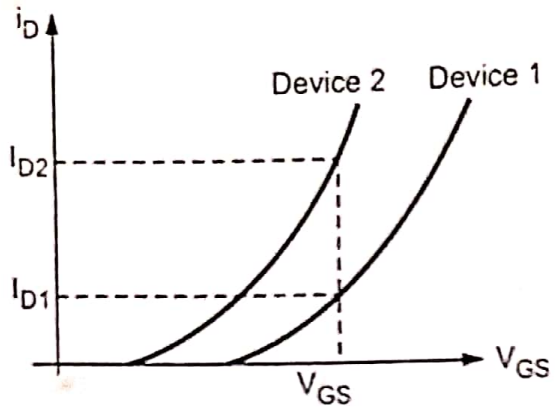

Fig. 4.32

The Fig. 4.32 clarifies that fixed value of V_{GS} is not a good technique of biasing.

In the figure, two transfer characteristics, $i_D - v_{gs}$, are shown for the two devices of the same type. Note that a fixed value of V_{GS} will have two substantially different drain current, I_{D1} and I_{D2}.

4.11.2 Biasing by Fixing V_G and Connecting a Resistance in the Source Terminal

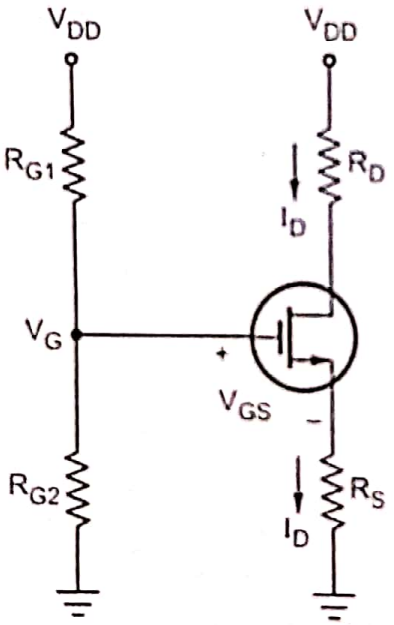

Fig. 4.33

A practically better biasing circuit for discrete MOSFET circuits, shown in the Fig. 4.34, consists of fixing the DC voltage at the gate, V_G, say by using a potential divider and connecting a resistance R_S in the source lead. For this circuit, we can write

$$V_G = V_{GS} + I_D R_S \qquad ...(1)$$

The resistor R_S stabilizes the quiescent operating point Q, viz. I_{DQ}. Let us see how. Suppose I_D increases, the voltage drop $I_D R_S$ will accordingly increase. But as V_G is constant, V_{GS} has to decrease proportionately. This in turn decreases I_D, nullifying the increase that has occured. Thus I_D is stabilized.

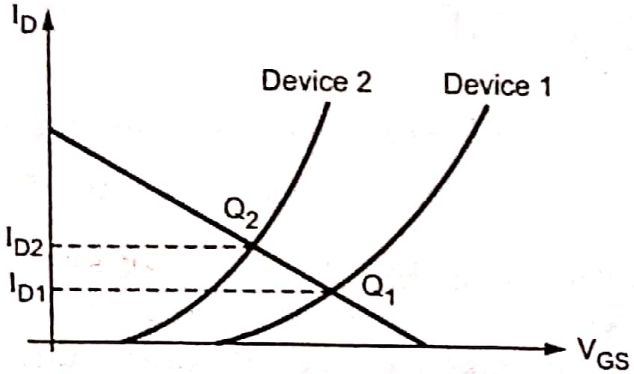

Fig. 4.34 Effect of biasing circuit

The Fig. 4.34 clearly indicates the effectiveness of this biasing circuit. The figure shows $i_D - v_{gs}$ characteristics for two devices of the same type and code number. A straight-line represented by the equation (1) is drawn on the characteristics. This line cuts the characteristics at Q_1 and Q_2. Note that

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compared to fixed bias circuit, here the change in I_D is much smaller. If R_S is made larger the line becomes more horizontal and changes in I_D are still reduced and more stability is obtained.

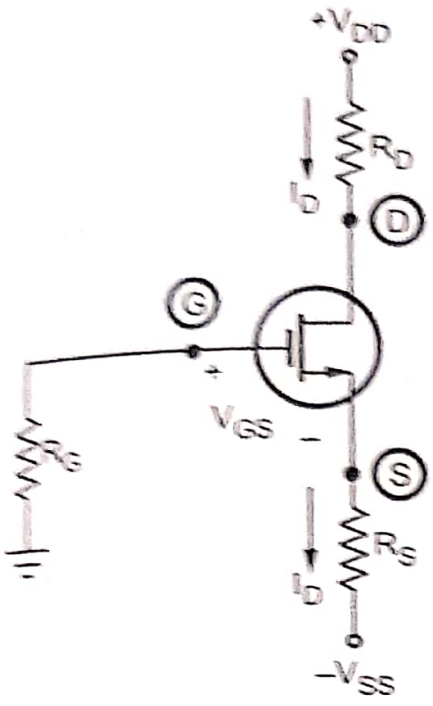

Fig. 4.35

Fig. 4.33 shows a circuit using one power supply V_{DD} and derives the necessary V_G through a voltage divider $[R_{G1}, R_{G2}]$. As gate current is nearly zero, R_{G1} and R_{G2} are selected in MΩ range. This assures a large input resistance to the signal source that may be connected to the gate. The resistor R_D is selected to be reasonably large to get high voltage gain and at the same time, keeping MOSFET in saturation for all times.

The biasing scheme suitable for the circuit using dual power supply is shown in Fig. 4.35.

As the gate current is zero, the gate terminal is at dc ground potential. The source terminal voltage is

$$V_S = I_D R_S - V_{SS}$$

The resistor R_G presents a high input resistance to a signal source which will be connected to the gate for the signal amplification.

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4.11.3 Biasing with a Drain-to-Gate Feedback Resistor

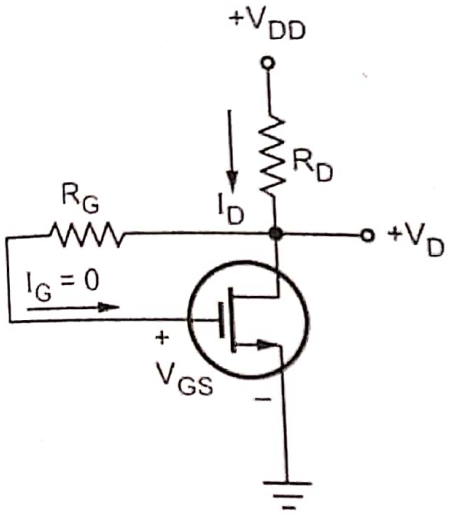

Fig. 4.37

Yet another effective method of biasing a discrete MOSFET circuit is to use a feedback resistor between the drain and the gate, as shown in Fig. 4.37.

The feedback resistor, R_G used is quite large, usually in the MΩ range. Since the gate current $I_G = 0$, the drain and the gate are at same potential for DC purposes. Hence

$$V_{GS} = V_{DS} = V_{DD} - I_D R_D$$

$$V_{DD} = V_{GS} + I_D R_D$$

If I_D increases, $I_D R_D$ will also increase. But as V_{DD} is constant V_{GS} decreases accordingly. This reduces I_D and stabilizes the drain current.

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4.11.4 Biasing with a Constant-Current Source

Biasing a MOSFET circuit using a constant-current source is most pop
MOSFETs used in Integrated circuits. The circuit commonly used is shown
Fig. 4.39.

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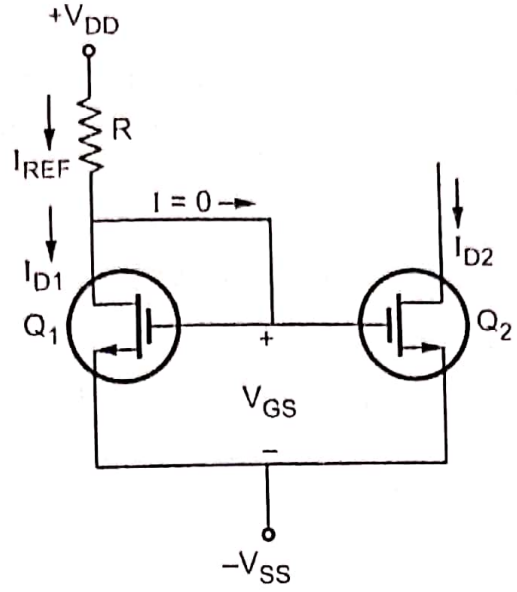

Fig. 4.39

The transistor Q_1 has its drain shorted to gate and so it is operating in saturation region. Then

$$I_{D1} = \frac{1}{2} k'_n \left[\frac{W}{L}\right]_1 [V_{GS} - V_{Th}]^2$$

$I_{REF} = \frac{V_{DD} - V_D}{R}$

$V_D = V_{GS} - V_{SS}$

Since gate current is zero;

$$I_{REF} = I_{D1} = \frac{V_{DD} - V_{GS} - (-V_{SS})}{R}$$

When a desired value of I_{REF} is known alongwith the parameters of Q_1; the required value of R can be obtained from the above equation.

V_{GS} for Q_1 and Q_2 is same. Assuming that Q_2 is working in saturation, which gives

$$I_{D2} = \frac{1}{2} k'_n \left[\frac{W}{L}\right]_2 [V_{GS} - V_{Th}]^2$$

where V_{Th} is assumed to be the same for both Q_1 and Q_2.

Then

$$\frac{I_{D2}}{I_{REF}} = \frac{\left[\frac{W}{L}\right]_2}{\left[\frac{W}{L}\right]_1}$$

Thus I_{D2} is related to I_{REF} by the ratio of the aspect ratios of Q_1 and Q_2.

If $\left[\frac{W}{L}\right]_2 = \left[\frac{W}{L}\right]_1$; then $I_{D2} = I_{REF}$

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Then current I_{REF} generated by Q_1 is repeated in Q_2. Hence the circuit is called **current repeater circuit**. When $I_{D2} = I_{REF}$, we can also say that I_{D2} is mirror image of I_{REF}. Therefore this circuit is also known as **current-mirror**. It is very widely used in the design of IC MOS amplifiers.

4.12 Nonideal Current Voltage Characteristics

Uptill now we have seen the ideal current-voltage (drain) characteristics of MOSFET. In practice, the current-voltage characteristics of MOSFET have five nonideal effects.

These are :

- Finite output resistance
- Body effect
- Subthreshold conduction
- Breakdown effects and
- Temperature effects

4.12.1 Finite Output Resistance

In ideal case, when a MOSFET is biased in the saturation region, the drain current, I_D is independent of drain-to-source voltage, V_{DS}. However, in practice, the I_D is slightly dependent on the drain to source voltage, V_{DS}. This can be observed on I_D versus V_{DS} characteristics where a nonzero slope does exists beyond the saturation point. Refer Fig. 4.40.

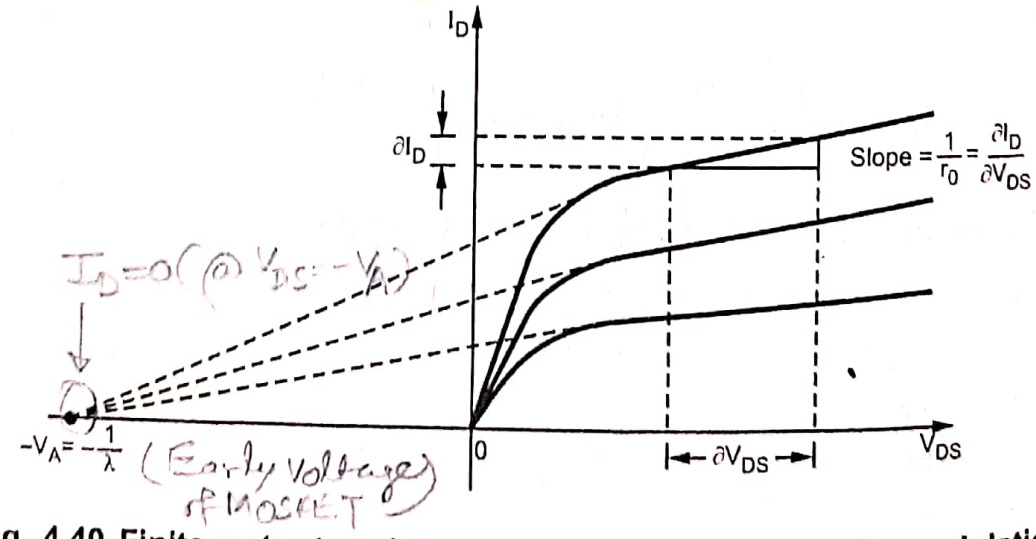

Fig. 4.40 Finite output resistance due to channel length modulation

For $V_{DS} > V_{DS(sat)}$, the actual point in the channel at which the inversion charge goes to zero moves away from the drain terminal. The effective channel length decreases, and hence the slope exists in the saturation region of V-I characteristics.

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This slope of the curve in the saturation region can be described by expressing the I_D versus V_{DS} characteristics in the form, for an n-channel device,

$$I_D = K\left[(V_{GS} - V_T)^2 (1 + \lambda V_{DS})\right] \quad \ldots (1)$$

where λ is a positive quantity called the **channel length modulation parameter.** As shown in the exaggerated view of V-I characteristics, the curves can be extrapolated to get intercept to voltage axis at a point $V_{DS} = -V_A$. The voltage V_A is usually defined as a positive quantity and is similar to the early voltage of a bipolar transistor. The parameter λ and V_A can be related. From equation (1) we have $(1 + \lambda V_{DS}) = 0$ at the extrapolated point where $I_D = 0$. At the point, $V_{DS} = -V_A$. Therefore,

$$1 + \lambda (-V_A) = 0$$

$$\therefore \quad V_A = \frac{1}{\lambda}$$

The output resistance r_o due to the channel length modulation is defined as

$$r_o = \left.\frac{\partial V_{DS}}{\partial I_D}\right|_{V_{GS} = \text{ constant}}$$

From equation (1) we can evaluate the output resistance at the Q point as

$$r_o = \frac{\partial V_{DS}}{\partial I_D} = \frac{V_{DSQ} - (-V_A)}{K\left[(V_{GSQ} - V_T)^2 (1 + \lambda V_{DSQ})\right] - 0}$$

$$= \frac{V_{DSQ} + \frac{1}{\lambda}}{K\left[(V_{GSQ} - V_T)^2 (1 + \lambda V_{DSQ})\right]} \qquad \because V_A = 1/\lambda$$

$$= \frac{\lambda V_{DSQ} + 1}{\lambda K\left[(V_{GSQ} - V_T)^2 (1 + \lambda V_{DSQ})\right]}$$

$$\therefore \quad r_o = \frac{1}{\lambda K\left[(V_{GSQ} - V_T)^2\right]}$$

$$\cong \frac{1}{\lambda I_{DQ}} \qquad \because \quad I_{DQ} \cong K\left[(V_{GSQ} - V_T)^2\right]$$

$$\therefore \quad r_o = \frac{V_A}{I_{DQ}}$$

Key point: *In practice, r_o is not infinite ; it has some finite value and it appears in the small signal equivalent circuit of MOSFET.*

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Key point

1. The equation says that V_T increases due to body effect.

2. The body effect can cause a degradation in circuit performance because of the changing threshold voltage.

4.12.3 Subthreshold Condition

The drain current, I_D in the ideal V-I characteristic is given by

$$I_D = K (V_{GS} - V_T)^2$$

Taking square roots on both sides we have,

$$\sqrt{I_D} = \sqrt{K} (V_{GS} - V_T)$$

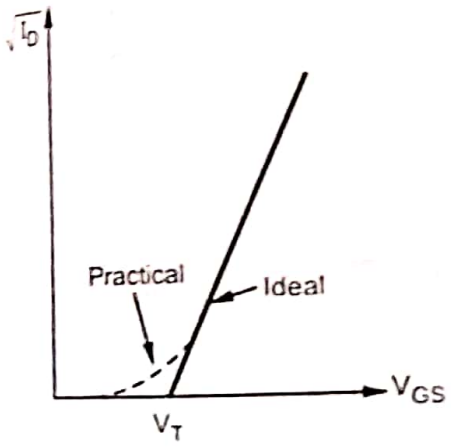

Fig. 4.43 Plot of $\sqrt{I_D}$ versus V_{GS}

The above relation is represented in Fig. 4.43. The ideal curve in the figure, says that $\sqrt{I_D}$ is a linear function of V_{GS}. However, in practice, when V_{GS} is slightly less than V_T, the drain current, I_D is not zero. This current is called the **subthreshold current.** This effect may not be significant for a single device, but if hundreds or thousands of devices on an integrated circuit are biased just slightly below the threshold voltage, the power supply current will not be zero but may contribute to significant power dissipation in the integrated circuit.

4.12.4 Breakdown Effects

There are three different breakdown effects which may occur in a MOSFET. These are

- Breakdown due to avalanche multiplication.
- Breakdown due to punch-through effect.
- Breakdown due to near-avalanche or snapback.

Breakdown due to avalanche multiplication

When applied drain voltage is too high, the drain-to-substrate pn junction may breakdown due to avalanche multiplication. This breakdown is same as reverse biased pn junction breakdown.

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Breakdown due to punch-through effect

Punch-through occurs when the drain voltage is large enough for the depletion region around the drain to extend completely through the channel to the source terminal. This effect also causes the drain current to increase rapidly with only a small increase in drain voltage. The punch through breakdown mechanism may become significant for smaller size devices.

Breakdown due to near-avalanche or snapback

The near-avalanche or snapback breakdown occurs due to second-order effects within the MOSFET, such as parasitic action or excess electric field in the oxide.

4.12.5 Temperature Effects

$K = \mu_n C_{ox}$

The values of threshold voltage; V_T and condition parameter K are dependent on temperature. The magnitude of the threshold voltage decreases with temperature, which means that the drain current increases with temperature at a given V_{GS}. On the other hand, the condition parameter K is a direct function of the inversion carrier mobility, which decreases as the temperature increases. This causes reduction in drain current. Since the temperature dependance of mobility is larger than that of the threshold voltage, the net effect of increasing temperature is a decrease in drain current at a given V_{GS}. This particular result provides temperature stability for MOSFETs and prevents them from thermal runaway.

4.13 Single Stage MOS Amplifier

Before studying single stage MOS amplifier, let us first define parameter, g_m, for MOS transistor.

The parameter relating i_d and v_{gs} under small-signal conditions, is

$$g_m = \left.\frac{\partial i_D}{\partial v_{gs}}\right|_{v_{gs}=V_{GS}} \quad V_{DS} \text{ constant}$$

It is known as transconductance or mutual conductance.

The voltage gain, A_v of the amplifier is then

$$|A_v| = g_m R_D$$

where

R_D is externally connected drain resistance, serving as the load resistance for the amplifier.

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Consider the basic single stage common-source MOSFET amplifier.

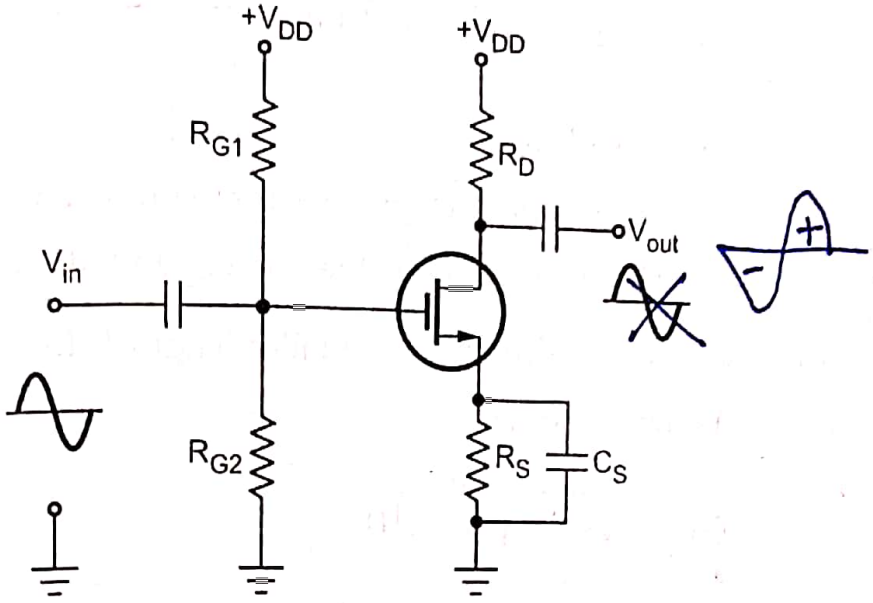

Fig. 4.44

Here, the input is applied between gate and ground and the output is taken from the drain. The input signal voltage v_{gs} between gate and source provides a current $g_m v_{gs}$ at the drain terminal as MOSFET is a voltage controlled current source for signal purposes. The input resistance is very large, ideally infinite since the gate current is practically zero. The output resistance looking into the drain r_o, is also very large. Then the small signal ac equivalent circuit for MOSFET is as shown in Fig. 4.45.

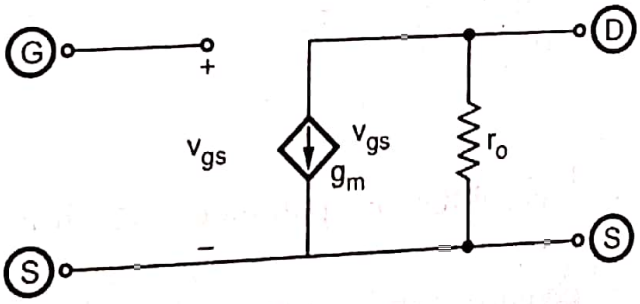

Fig. 4.45

While analyzing the amplifier circuit for signal purposes, the dc voltage sources are to be replaced by short circuits. The output resistance, r_o, is of the order of 10 kΩ to 1 MΩ.

Note that the small-signal parameters, g_m and r_o, depend upon the DC quiescent operating point of the MOSFET. If the output resistance is considered then the voltage gain of the circuit is

$$A_v = -g_m R_{eq} \text{ where } R_{eq} = R_D \parallel r_o$$

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The parameter g_m is given by

$$g_m = k'_n\left[\frac{W}{L}\right][V_{GS} - V_{Th}]$$

where $$k'_n = \mu_n C_{ox}$$

It is seen that g_m is proportional to process transconductance parameter, k'_n and to the ratio $\frac{W}{L}$. Hence to obtain a larger value for g_m and thereby larger voltage gain, the device must have larger width W and smaller length L for channel region.

The g_m can also be obtained as

$$g_m = \sqrt{2k'_n}\sqrt{\frac{W}{L}}\sqrt{I_D}$$

This equations indicates that, g_m is proportional to the square-root of the DC bias current. Increasing I_D 4 times will increase g_m two times.

One more equation for g_m is

$$g_m = \frac{2I_D}{V_{GS} - V_{Th}} = \frac{2I_D}{V_{ov}}$$

where V_{ov} is known as **overdrive voltage.**

The output resistance r_o is given by

$$r_o = \frac{|V_A|}{I_D}$$

where

$V_A = \frac{1}{\lambda}$ is a MOSFET parameter which is either given or can be measured

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4.13.1 Common - Source MOSFET Amplifier

Similar to Common Emitter (CE) configuration of BJT, Common Source (CS) configuration is the most commonly used configuration for MOSFET amplifier circuits.

A common - source amplifier, using constant-current biasing is shown in Fig. 4.49.

For ac analysis of the amplifier, we will assume that all capacitors in the circuit act as a short circuit at signal frequency. The constant-current source, I, is used for DC biasing and for ac purposes, it is shorted by ~~CS~~. Hence it need no be considered in ac

CS (capacitor By-pass)

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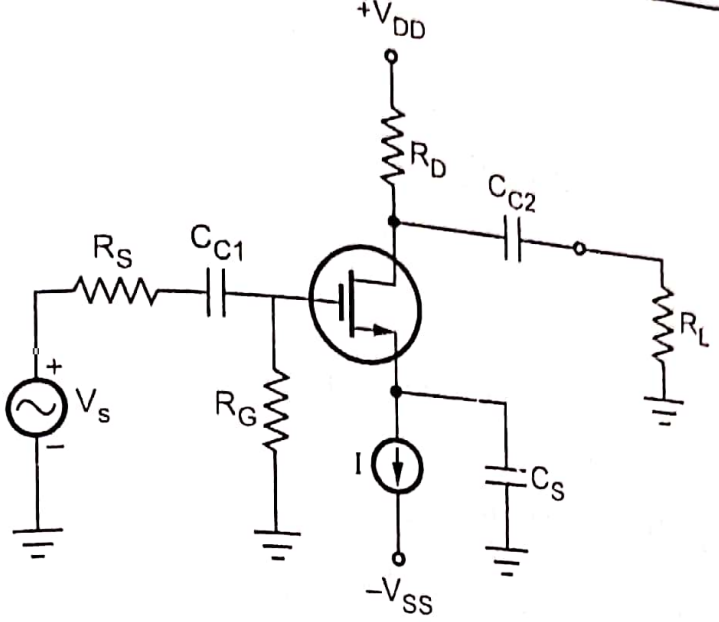

Fig. 4.48

analysis. Also, the DC supply voltage points, V_{DD} and $-V_{SS}$, will be assumed to be at ground potential for ac signal analysis. This ground is called as signal ground or ac ground. The signal source voltage V_S is connected to the gate through a coupling capacitor C_{C1}. The internal resistance of V_S is R_S. The signal output voltage at the drain is coupled to the load resistance R_L through a large coupling capacitor C_{C2} which blocks the dc drain voltage and applies only ac signal voltage to R_L.

To analyze the amplifier, we replace the MOSFET by its small-signal equivalent circuit. It is shown in the Fig. 4.49.

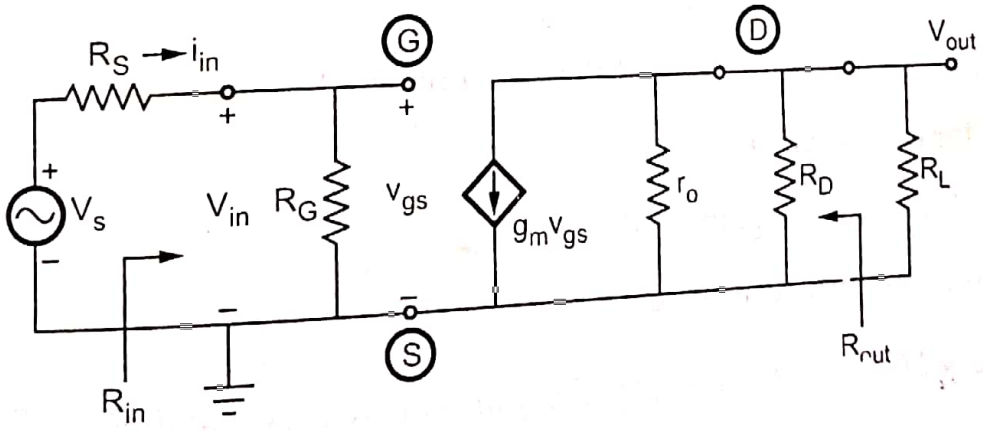

Fig. 4.49

Assume the gate current equal to zero.

Then $$V_{in} = i_{in} R_G$$

Hence $$R_{in} = \frac{V_{in}}{i_{in}} = R_G$$

$$V_{in} = \frac{R_G}{R_S + R_G} V_S$$

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Normally R_G selected is in MΩ range, then many times $R_G >> R_S$.

and $v_{in} \approx v_{sig}$

Let $R_{eq} = r_o \parallel R_D \parallel R_L$

$v_{out} = - g_m v_{gs} R_{eq}$

But $v_{gs} = v_{in}$

$\therefore$ Voltage gain $= A_v = \dfrac{v_{out}}{v_{in}} = - g_m R_{eq}$

Voltage gain including the source is

$$A_{vs} = \frac{v_{out}}{v_s} = \frac{v_{out}}{v_{in}} \times \frac{v_{in}}{v_s}$$

$$\therefore \quad A_{vs} = A_v \left[\frac{R_G}{R_G + R_S} \right]$$

To find R_{out}, we replace v_s by a short circuit. Then

$v_s = 0$; and hence $v_{gs} = 0$

and also $g_m v_{gs} = 0$

i.e. current source = 0 meaning that it acts as an open circuit (no current). Therefore, looking back into output terminals,

$$R_{out} = r_o \parallel R_D$$

From the above analysis of CS amplifier, we note that it has

1. very high input resistance,
2. reasonably high voltage gain, and
3. relatively high output resistance

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4.13.2 Common Source Amplifier with a Source Resistance

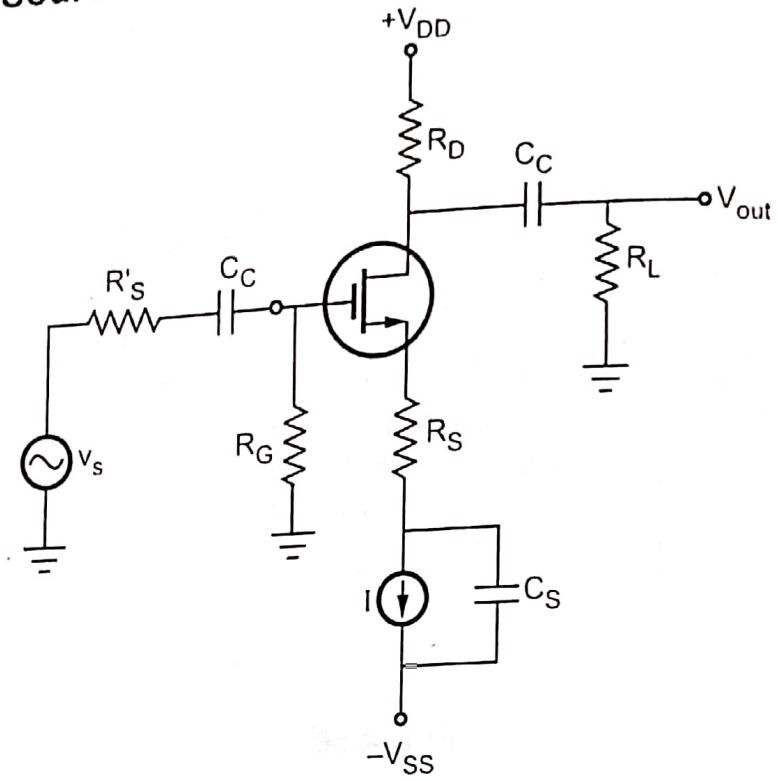

Fig. 4.51 Common source amplifier with a source resistance

The Fig. 4.51 shows a common source amplifier, using constant-current source biasing, with a resistance. – R_S in the source lead.

The effect of r_o on the operation of this discrete-circuit amplifier is not important. Hence we shall neglect it and analyze the circuit. The small-signal ac equivalent circuit is shown in the Fig. 4.52.

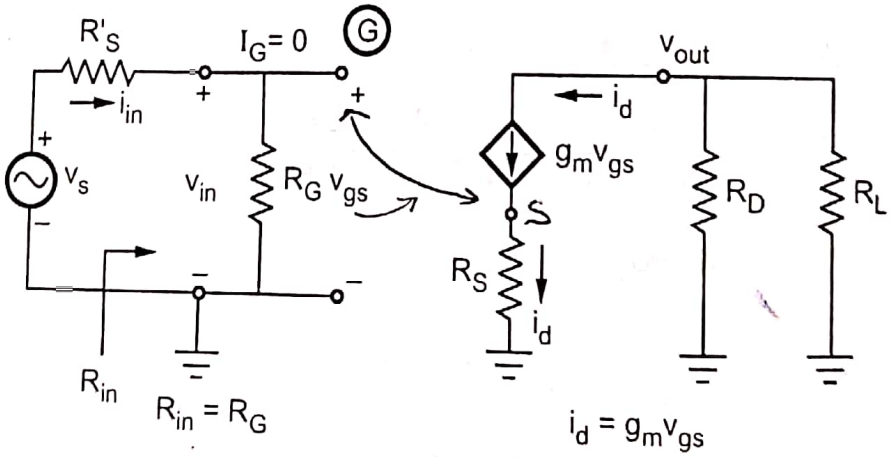

Fig. 4.52

$$v_{gs} = v_g - v_s = v_{in} - i_d R_s$$

$$v_{out} = - i_d [R_D \parallel R_C] = - (g_m v_{gs}) [R_D \parallel R_L]$$

$$\therefore \quad v_{out} = - g_m [v_{in} - i_d R_s] [R_D \parallel R_L]$$

$$\therefore \quad v_{out} = - g_m v_{in} (R_D \parallel R_L) + g_m i_d R_S (R_D \parallel R_L)$$

$$v_{out} = - g_m v_{in} [R_D \parallel R_L] + g_m R_S [- v_{out}]$$

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$$v_{out} + g_m R_S v_{out} = -g_m v_{in} [R_D \parallel R_L]$$

$$v_{out} [1 + g_m R_S] = -g_m v_{in} [R_D \parallel R_C]$$

$$A_v = \frac{v_{out}}{v_{in}} = \frac{-g_m (R_D \parallel R_L)}{1 + g_m R_S}$$

$$v_{in} = \frac{v_s}{R_S + R_G} \times R_G$$

$$\frac{v_s}{v_{in}} = \frac{R_G}{R_S + R_G}$$

$$A_{VS} = \frac{v_{out}}{v_S} = \frac{v_{out}}{v_{in}} \times \frac{v_{in}}{v_s}$$

$$A_{VS} = A_v \times \frac{R_G}{R_S + R_G}$$

Comparing the performance of this circuit with its counterpart, i.e. previous circuit without R_S in the source lead, we note that inclusion of R_S in the source lead reduces the voltage gain of the circuit. This is because R_S introduces negative feedback. As the gain is reduced, R_S is also known as source degeneration resistance.

4.13.3 Common - Gate (CG) Amplifier

In the common-gate or grounded-gate amplifier, the gate terminal of the MOSFET is grounded for ac or signal purposes. The input is applied to the source, while the output is taken from the drain. Thus gate remains common between the input and output.

A common-gate amplifier circuit is shown below.

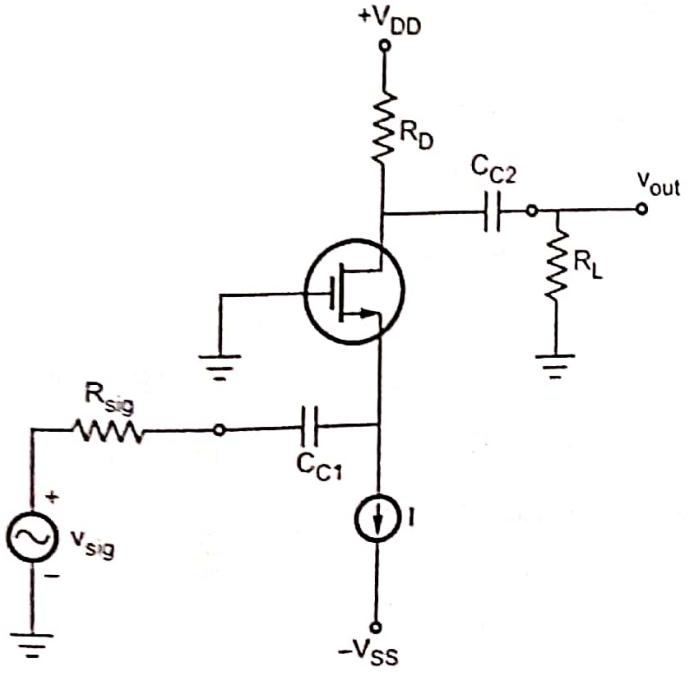

Fig. 4.53

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Assume all capacitors to act as short circuit at signal frequency. The small signal equivalent circuit is shown in Fig. 4.54.

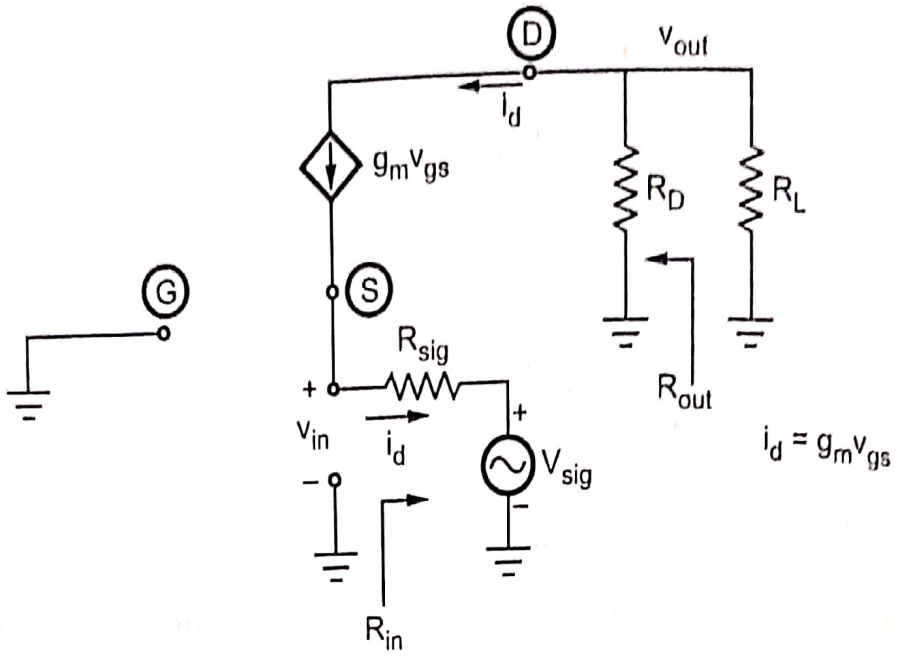

Fig. 4.54

$$R_{in} = \frac{v_{in}}{i_d} = \frac{v_{in}}{g_m v_{gs}}$$

Normally, R_{sig} is much less than $\frac{1}{g_m}$.

When R_{sig} is small, $v_{in} \approx v_{gs}$

and

$$R_{in} \cong \frac{v_{in}}{g_m v_{in}} = \frac{1}{g_m}$$

$$v_{gs} = v_g - v_s = [0] - [i_d R_{sig} + v_{sig}]$$

$$v_{out} = - i_d [R_D \parallel R_L]$$

$$= - (g_m v_{gs}) [R_D \parallel R_L]$$

$$= - (g_m) [- i_d R_{sig} + v_{sig}] [R_D \parallel R_L]$$

$$= g_m R_{sig} [R_D \parallel R_L] i_d + g_m [R_D \parallel R_L] v_{sig}$$

$$\therefore \quad v_{out} = g_m R_{sig} [- v_{out}] + g_m [R_D \parallel R_L] v_{sig}$$

$$\therefore \quad v_{out} [1 + g_n R_{sig}] = g_m (R_D \parallel R_L) v_{sig}$$

$$A_{vs} = \frac{v_{out}}{v_{sig}} = \frac{+g_m (R_D \parallel R_L)}{1 + g_m R_{sig}}$$

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To find R_{out}, we replace the voltage source v_{sig} by short circuit. Then $v_{gs} = 0$; and current source, $g_m v_{gs} = 0$, i.e. open circuit. Therefore

$$R_{out} = R_D$$

Let us compare CS amplifier with CG amplifier.

1. In the CS amplifier, output is inverted w.r.t input, i.e. there is phase shift of 180° between input and output signals. In CG amplifier, the input and output signals are in phase.
2. The input resistance of the CS amplifier is very high, while that of CG amplifier, is low.
3. While the voltage gain $A_V = \frac{V_{out}}{V_{in}}$ for CS amplifier is nearly equal to that of CG amplifier; the overall voltage gain, $A_{vs} = \frac{V_{out}}{V_s}$, for the CG amplifier is less than that for the CS amplifier. This is due to the low input resistance of the CG configuration.

Let us consider the CG amplifier supplied from the signal current source i_{sig} having an internal resistance R_{sig}. The circuit is shown below.

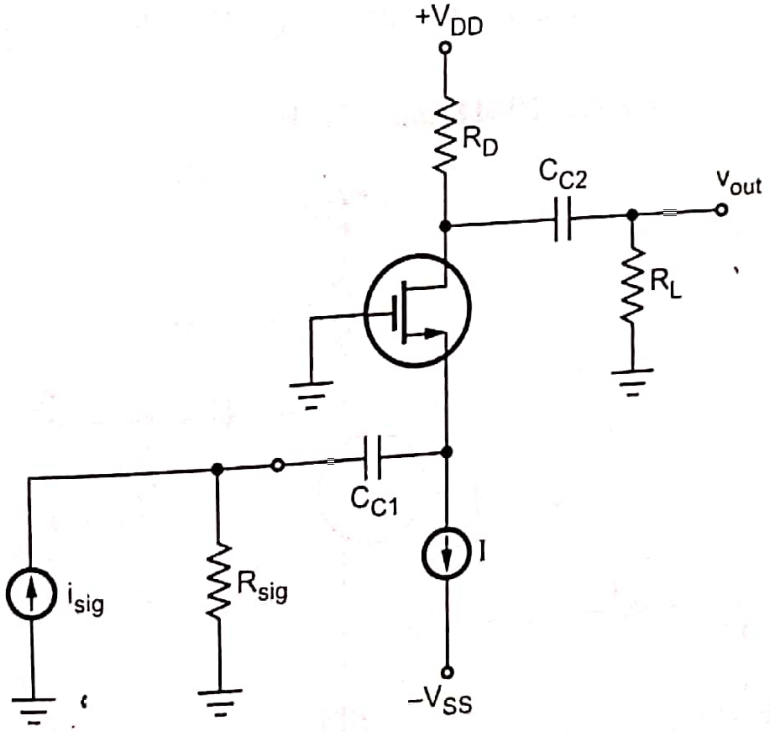

Fig. 4.55

We have shown previously that for CG circuit,

$$R_{in} = \frac{1}{g_m}$$

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Then the equivalent circuit on the input side is as shown below :

By current division : $i_{in} = i_{sig}\left(\frac{R_{sig}}{R_{sig} + R_{in}}\right)$

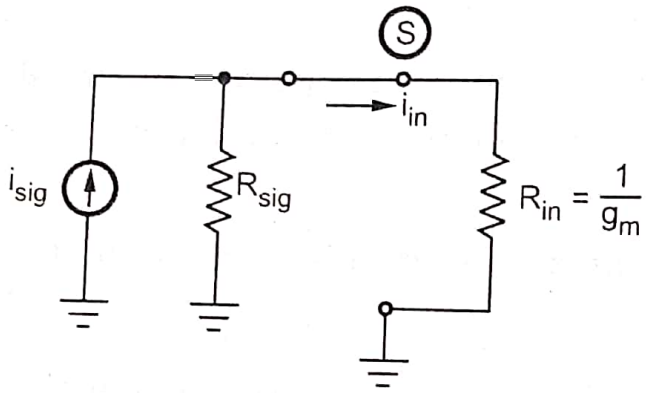

Fig. 4.56

$$i_{in} = i_{sig}\left(\frac{R_{sig}}{R_{sig} + 1/g_m}\right)$$

Normally

$$R_{sig} >> \frac{1}{g_m},$$

and then

$$i_{in} \approx i_{sig}$$

This equation shows that there is very little signal-current attenuation at the input. As shown previously, $i_{in} = i_d = g_m v_{gs}$. Thus, this circuit acts as a unity gain current amplifier or current follower. For input current, input resistance is small, while the same current is reproduced at the output at a much higher output resistance. This property of CG configuration is used in its most widely used application, known as the cascode circuit.

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4.13.4 Common-Drain or Source-Follower Amplifier

In common-drain configuration of MOSFET amplifier, the drain terminal is kept at ac ground (it need not be at ground potential for DC) so that the drain becomes common between input, applied to gate, and output, taken from the source. This configuration is more commonly known as source follower, rather than common-drain.

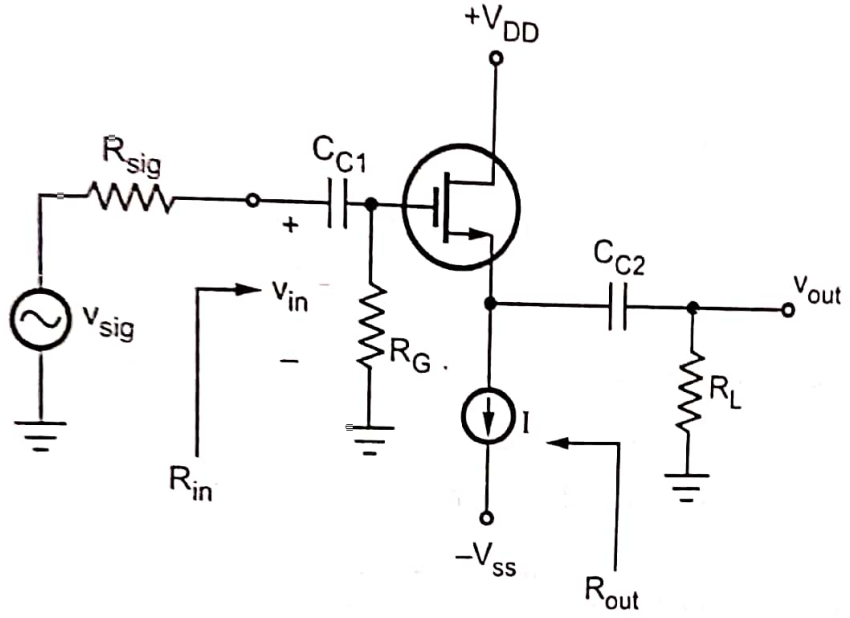

Fig. 4.58

As the drain terminal is to be at ac ground to make drain as common terminal, the externally connected resistor R_D required in other configurations, is not necessary in this configuration. The signal input is applied to the gate via coupling capacitor C_{C1} and the output signal voltage is connected to the load resistor R_L via coupling capacitor C_{C2}.

Both the capacitors C_{C1} and C_{C2} will be assumed to act as short circuit at input signal frequency.

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The small-signal ac equivalent circuit is shown below.

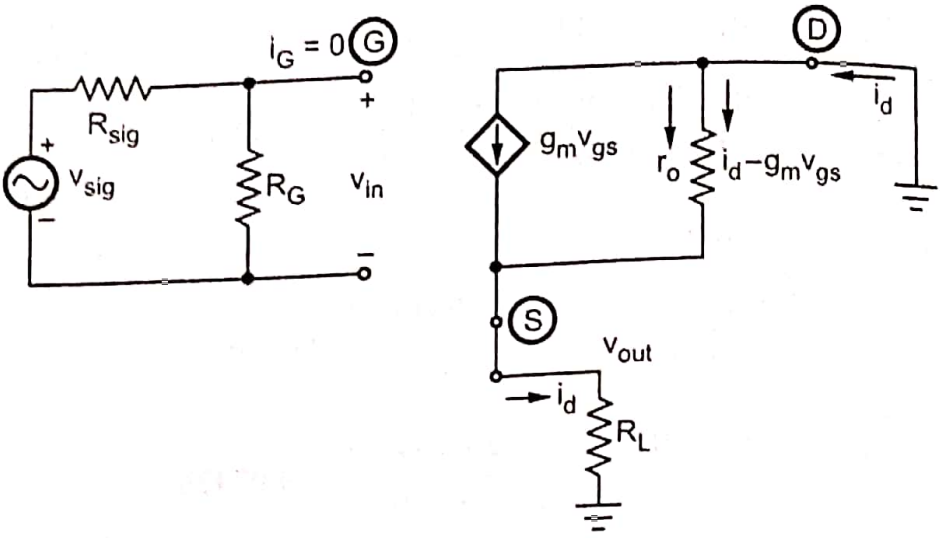

Fig. 4.59

$$v_{in} = \frac{v_{sig}}{R_G + R_{sig}} \times R_G$$

$$\therefore \quad \frac{v_{in}}{v_{sig}} = \frac{R_G}{R_G + R_{sig}}$$

By KVL to drain circuit

$$r_o [i_d - g_m v_{gs}] + i_d R_L = 0$$

$$v_{gs} = v_g - v_s = v_{in} - i_d R_L$$

$$\therefore \; r_o i_d - g_m r_o [v_{in} - i_d R_L] + i_d R_L = 0$$

$$\therefore i_d [r_o + g_m r_o R_L + R_L] = g_m r_o v_{in}$$

$$\therefore \quad i_d = \frac{g_m r_o v_{in}}{r_o + R_L(1 + g_m r_o)}$$

$$v_{out} = i_d R_L = \frac{g_m r_o R_L v_{in}}{r_o + (1 + g_m r_o) R_L}$$

$$\therefore \quad A_v = \frac{v_{out}}{v_{in}} = \frac{g_m r_o R_L}{r_o + (1 + g_m r_o) R_L}$$

$$\therefore \quad A_v = \frac{r_o R_L}{\frac{r_o}{g_m} + \frac{R_L}{g_m} + r_o R_L} = \frac{r_o R_L}{r_o R_L + \frac{r_o + R_L}{g_m}}$$

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$$A_v = \frac{\frac{r_o R_L}{r_o + R_L}}{\frac{1}{g_m} + \frac{r_o R_L}{r_o + R_L}}$$

$$\therefore \quad A_v = \frac{(r_o || R_L)}{(r_o || R_L) + \frac{1}{g_m}}$$

As normally, $\frac{1}{g_m} < (r_o \parallel R_L)$,

the voltage gain will be nearly equal to "one", but slightly less than "1".

When $A_v \approx 1$, then $v_{out} \approx v_{in}$. This means as v_{in} increases, v_{out} will increase and as v_{in} decreases v_{out} will also decrease. Thus output follows input. As the output is taken from the source, the circuit is known as source follower.

$$A_{vs} = \frac{v_{out}}{v_{sig}} = \frac{v_{out}}{v_{in}} \times \frac{v_{in}}{v_{sig}}$$

$$\therefore \quad A_{vs} = \frac{R_G}{R_G + R_{sig}} \times A_v$$

To find R_{out} of the circuit, we disconnect the load R_L and replace the input signal source by short circuit. At the output terminal, we apply externally the voltage V. The circuit becomes as shown below.

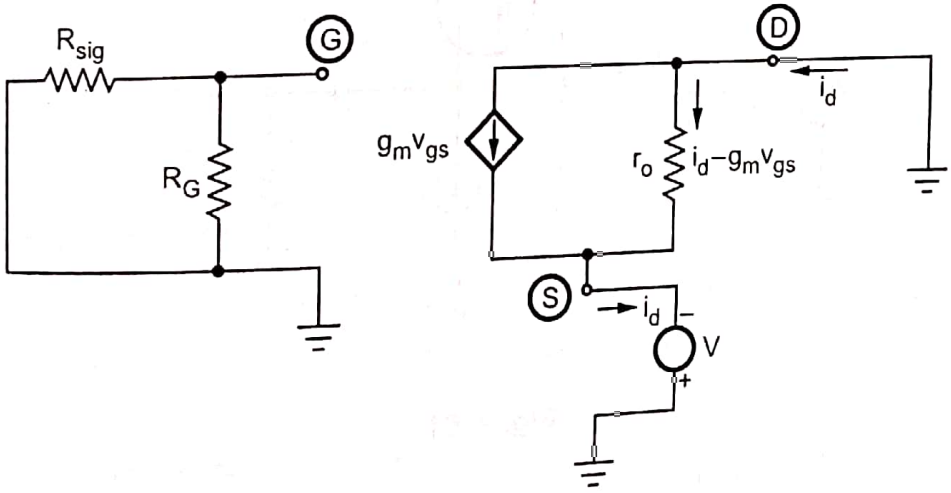

Fig. 4.60

$$v_{gs} = v_g - v_s = 0 - (v) = v$$

By KVL to drain side

$$r_o [i_d - g_m v_{gs}] - v = 0$$

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$\therefore \quad r_o\, i_d - g_m\, r_o\, [v] - v = 0 \qquad \therefore \quad r_o\, i_d = v\,[1 + g_m\, r_o]$

$$\therefore \quad R_{out} = \frac{v}{i_d} = \frac{r_o}{1 + g_m r_o}$$

$$\therefore \quad R_{out} = \frac{r_o \times \dfrac{1}{g_m}}{\dfrac{1}{g_m} + r_o} = r_o \parallel \frac{1}{g_m}$$

Usually, $r_o >> \dfrac{1}{g_m}$; then $R_{out} \approx \dfrac{1}{g_m}$

This shows that R_{out} is reasonably small. Thus, the source follower has a very high input resistance, a relatively low output resistance, and a voltage gain which is less than but nearly equal to unity.

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14 Internal Capacitances of MOSFET

When the MOSFET is to be used at high frequency or when it is to be operated at gh speed in digital logic circuits; the internal capacitances of MOSFET play an portant role.

There are basically two types of internal capacitances in the MOSFET.

1. **The gate capacitive effect capacitance :** The gate terminal forms a parallel-plate capacitor with the channel, the two being separated from each other by oxide insulating layer serving as the dielectric. Its value per unit area is denoted by C_{ox} (F/m^2)

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2. **Depletion-layer Capacitances :** There are two depletion-layer capacitances associated with MOSFET.

   For n-channel MOSFET, drain and source regions are of n-type, while the substrate in between is of p-type. Thus, there are two p-n junctions : one between source and substrate, the other between drain and substrate. These are reverse biased p-n junctions. Associated with each of them, there is depletion region capacitance. Thus, there is one depletion region capacitance between source and substrate and the other between drain and substrate.

For MOSFET with four terminals, viz. Gate, Drain, Source, and Body (substrate) there are five capacitances :

C_{gs} : capacitance between gate and source,

C_{gd} : capacitance between gate and drain,

C_{gb} : capacitance between gate and body,

C_{sb} : capacitance between source and body,

C_{db} : capacitance between drain and body.

Gate Capacitive Effect

The gate capacitive effect can be taken into account by the three capacitances : C_{gs}, C_{gd} and C_{gb}

1. When the MOSFET is operating in the triode region of its characteristics where the drain current increases with increasing drain voltage, the channel is having uniform depth.

   C_{ox} is gate capacitance per unit area. Hence, if W and L are width and length of the channel, respectively; then the gate capacitance = WL C_{ox}. (F). With uniform channel depth, this is equally divided between the source and drain ends; thus

$$C_{gs} = C_{gd} = \frac{1}{2} WL\, C_{ox} \text{ (triode region)}$$

Of course, this is an approximation, but sufficiently justifiable for the triode region.

2. In saturation region, the channel is tapering and it pinches off at or near the drain. Due to this, C_{gd} can be assumed to be zero. It can be shown that the gate-to-channel capacitance is approximately $\frac{2}{3}$ WL C_{ox}.

Thus

$$\left.\begin{aligned} & C_{gs} = \frac{2}{3} WLC_{ox} \\ \text{and} \quad & \\ & C_{gd} = 0 \end{aligned}\right\} \text{ saturation region}$$

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: The channel disappears when the MOSFET is cutoff. This makes C_{gs} and C_{gd} equal to zero. But we can consider the gate capacitive effect by assigning a capacitance WL C_{ox} to the gate body capacitance.

Thus

$$\left.\begin{aligned} C_{gs} &= C_{gd} = 0 \\ \text{and} \\ C_{gb} &= WL\,C_{ox} \end{aligned}\right\} \text{ cut off}$$

: To the above formulae for different capacitances, an additional small capacitive component is to be added to C_{gs} and C_{gd}. The small capacitance results due to source and drain diffusions extending slightly under the gate oxide. If this overlap length is denoted by L_{ov}, then the overlap capacitance component is

$$C_{ov} = WL_{ov}\,C_{ox}$$

Typically, L_{ov} = 0.05 to 0.1 times L (channel length).

The Junction Capacitances

The two pn junctions, one between the source and body and the other between drain and body are reverse-biased p-n junction. With each of these two p-n junctions, a depletion-layer capacitance is associated.

The depletion-layer capacitance between the source and body, C_{sb}, is given by

$$C_{sb} = \frac{C_{sbo}}{\sqrt{1 + \frac{V_{sb}}{V_0}}}$$

where,

C_{sbo} = value of C_{sb} when no bias is applied

V_{sb} = magnitude of the reverse bias voltage applied,

V_0 = internally developed junction potential,

typically between 0.6 V to 0.8 V

Similarly,

the depletion-layer capacitance between the drain and the body is given by

$$C_{db} = \frac{C_{dbo}}{\sqrt{1 + \frac{V_{DB}}{V_0}}}$$

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where

C_{db0} = capacitance value when no reverse-bias voltage is applied

V_{DB} = magnitude of reverse bias voltage

While calculating the depletion layer capacitance using above mentioned equation, it is to be noted that the grading coefficient, m is assumed to be equal to 0.5 for both junctions. Also the above formulae for depletion-layer capacitances assume small-signal operation. These formulae can be suitably modified to obtain approximately the average values for these capacitances when the MOSFET is operated under large-signal conditions e.g. use of MOSFET in logic circuits.

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4.15 The High-Frequency MOSFET Model

The small-signal model of a MOSFET including four capacitances C_{gs}, C_{gd}, C_{sb}, and C_{db} is shown in the Fig. 4.62. This circuit is useful for determining the high-frequency response of MOSFET amplifiers.

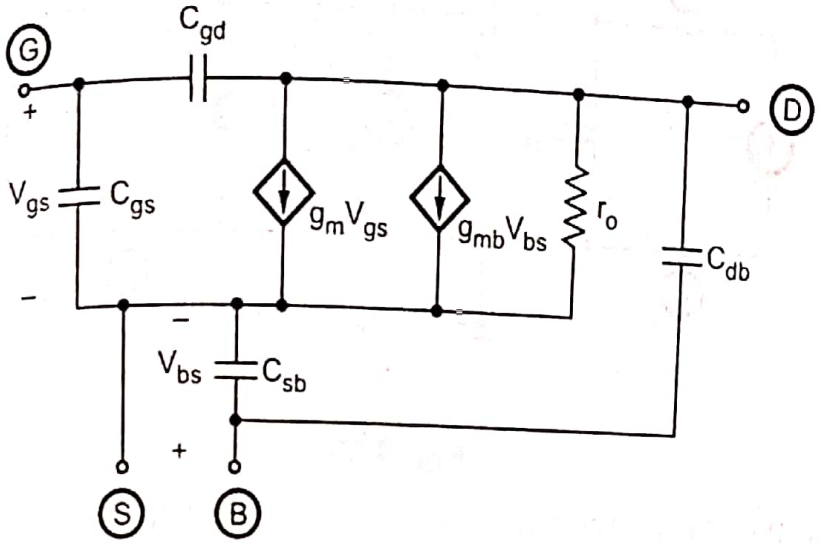

Fig. 4.62

When the body and source are shorted together, the above equivalent circuit reduces to the following :

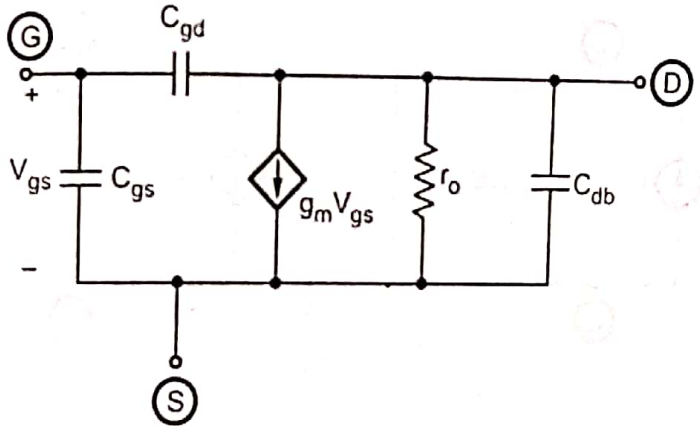

Fig. 4.63

The capacitance C_{db} is usually neglected while C_{gd} plays main role in the high frequency response determination for MOSFET amplifier. Neglected C_{bd}, circuit reduces to the following :

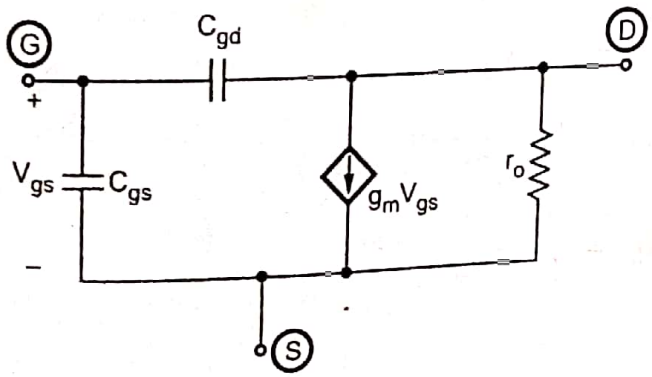

Fig. 4.64

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Using the above model shown in Fig. 4.64, we can determine the short-circuit current gain of common source MOSFET amplifier, as shown inFig. 4.65.

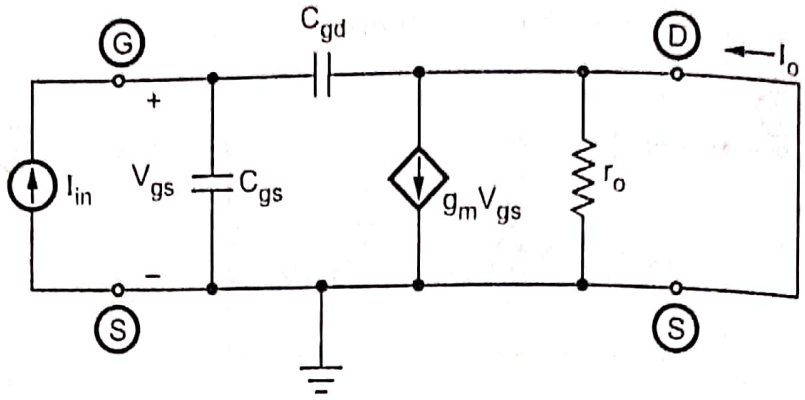

Fig. 4.65

To determine the short-circuit gain, the amplifier is supplied from a current-source I_{in} and the output terminals are directly short-circuited with I_o as short-circuit output current. With the output terminals shorted, the circuit reduces as shown in Fig. 4.66.

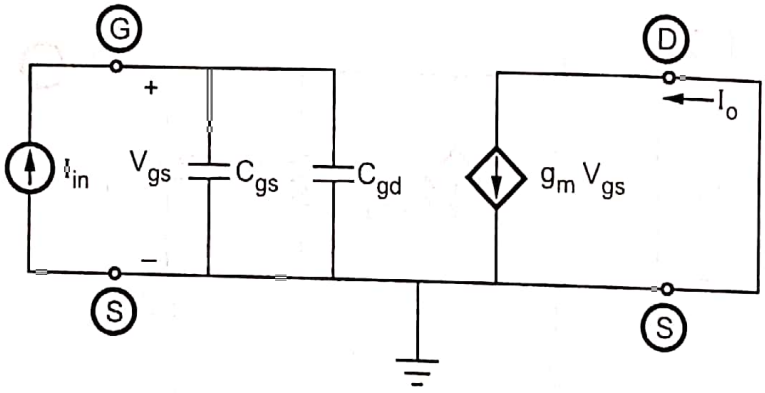

Fig. 4.66

Short-circuit current gain A_{Is} is

$$A_{Is} = \frac{I_o}{I_{in}}$$

$$I_o = g_m V_{gs}$$

$$V_{gs} = I_{in} \times \frac{1}{j\omega[C_{gs} + C_{gd}]}$$

$$\therefore \quad A_{Is} = \frac{I_o}{I_{in}} = \frac{g_m}{j\omega (C_{gs} + C_{gd})}$$

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$$|A_{Is}| = \frac{g_m}{\omega (C_{gs} + C_{gd})}$$

At a frequency f_T; known as unity-gain frequency; the magnitude of the current gain is unity.

Thus
$$|A_{Is}| = 1 = \frac{g_m}{2\pi f_T (C_{gs} + C_{gd})}$$

$$\therefore \quad f_T = \frac{g_m}{2\pi (C_{gs} + C_{gd})}$$

For older technologies f_T was ranging from about 100 MHz to many GHz for new high-speed technologies.

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3

Feedback Amplifiers

3.1 Introduction

Feedback plays an important role in almost all electronic circuits. It is almost invariably used in the amplifier to improve its performance and to make it more ideal. In the process of feedback, a part of output is sampled and fed back to the input of the amplifier. Therefore, at input we have two signals : Input signal and part of the output which is fed back to the input. Both these signals may be in phase or out of phase. When input signal and part of output signal are in phase, the feedback is called **positive feedback**. On the other hand, when they are in out of phase, the feedback is called **negative feedback**. Use of positive feedback results in oscillations and hence not used in amplifiers.

In this chapter, we introduce the concept of feedback and show how to modify the characteristics of an amplifier by combining a portion or part of the output signal with the input signal.

3.2 Classification of Amplifiers

Before proceeding with the concepts of feedback, it is useful to understand the classification of amplifiers based on the magnitudes of the input and output impedances of an amplifier relative to the source and load impedances, respectively. The amplifiers can be classified into four broad categories : voltage, current, transconductance and transresistance amplifiers.

3.2.1 Voltage Amplifier

Fig. 3.1 shows a Thevenin's equivalent circuit of an amplifier.

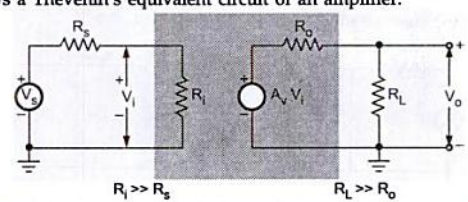

Fig. 3.1 Thevenin's equivalent circuits of a voltage amplifier

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If the amplifier input resistance R_i is large compared with the source resistance R_s then $V_i \approx V_s$. If the external load resistance R_L is large compared with the output resistance R_o of the amplifier, then $V_o \approx A_v V_i \approx A_v V_s$. Such amplifier circuit provides a voltage output proportional to the voltage input and the proportionality factor does not depend on the magnitudes of the source and load resistances. Hence, this amplifier is called **voltage amplifier**. An ideal voltage amplifier must have infinite input resistance R_i and zero output resistance R_o. For practical voltage amplifier we must have $R_i >> R_s$ and $R_L >> R_o$.

3.2.2 Current Amplifier

Fig. 3.2 shows Norton's equivalent circuit of a current amplifier. If amplifier input resistance $R_i \to 0$, then $I_i \approx I_s$. If amplifier output resistance $R_o \to \infty$, then $I_L = A_i I_i$. Such amplifier provides a current output proportional to the signal current and the proportionality factor is independent of source and load resistances. This amplifier is called **current amplifier**. An ideal current amplifier must have zero input resistance R_i and infinite output resistance R_o. For practical current amplifier we must have $R_i << R_s$ and $R_o >> R_L$.

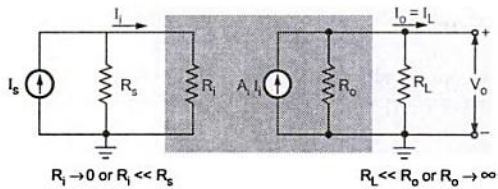

Fig. 3.2 Norton's equivalent circuits of a current amplifier

3.2.3 Transconductance Amplifier

Fig. 3.3 shows a transconductance amplifier with a Thevenin's equivalent in its input circuit and Norton's equivalent in its output circuit. In this amplifier, an output current is proportional to the input signal voltage and the proportionality factor is independent of the magnitudes of the source and load resistances. Ideally, this amplifier must have an infinite input resistance R_i and infinite output resistance R_o. For practical transconductance amplifier we must have $R_i >> R_s$ and $R_o >> R_L$.

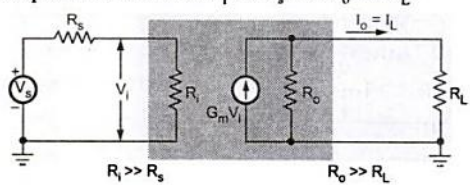

Fig. 3.3 Transconductance amplifier

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3.2.4 Transresistance Amplifier

Fig. 3.4 shows a transresistance amplifier with a Norton's equivalent in its input circuit and a Thevenin's equivalent in its output circuit. In this amplifier an output voltage is proportional to the input signal current and the proportionality factor is independent on the source and load resistances. Ideally, this amplifier must have zero input resistance R_i and zero output resistance R_o. For practical transresistance amplifier we must have $R_i << R_s$ and $R_o << R_L$.

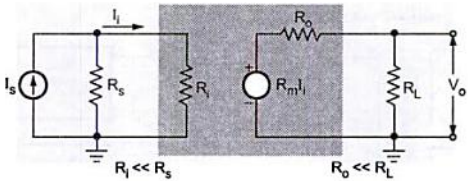

Fig. 3.4

3.3 Feedback Concept

In the previous section we have seen four basic amplifier types and their ideal characteristics. In each one of these circuits we can sample the output voltage or current by means of a suitable sampling network and apply this signal to the input through a feedback two port network, as shown in the Fig. 3.5. At the input the feedback signal is combined with the input signal through a mixer network and is fed into the amplifier.

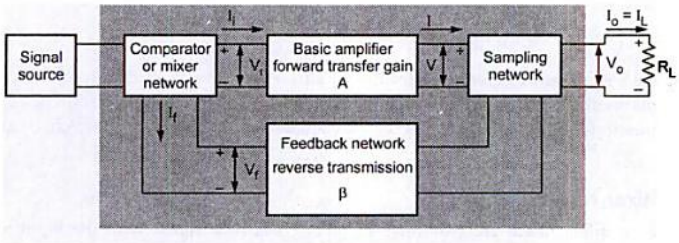

Fig. 3.5 Typical feedback connection around a basic amplifier

As shown in the Fig. 3.5 feedback connection has three networks :

- Sampling Network
- Feedback Network
- Mixer Network

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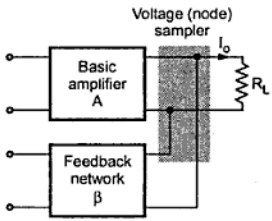
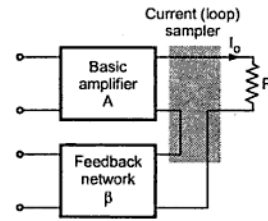
3.3.1 Sampling Network

There are two ways to sample the output, according to the sampling parameter, either voltage or current. The output voltage is sampled by connecting the feedback network in shunt across the output, as shown in the Fig. 3.6 (a). This type of connection is referred to as **voltage or node sampling**. The output current is sampled by connecting the feedback network in series with the output as shown in the Fig. 3.6 (b). This type of connection is referred to as **current or loop sampling**.



(a) Voltage or node sampling



(b) Current or loop sampling

Fig. 3.6

3.3.2 Feedback Network

It may consists of resistors, capacitors and inductors. Most often it is simply a resistive configuration. It provides reduced portion of the output as feedback signal to the input mixer network. It is given as,

$$V_f = \beta V_o$$

where β is a **feedback factor** or **feedback ratio**. The symbol β used in feedback circuits represents feedback factor which always lies between 0 and 1. It is totally different from β symbol used to represent current gain in common emitter amplifier, which is greater than 1.

3.3.3 Mixer Network

Like sampling, there are two ways of mixing feedback signal with the input signal. These are : series input connection and shunt input connection. The Fig. 3.7 (a) and (b) show the simple and very common **series (loop)** input and **shunt (node)** input connections, respectively.

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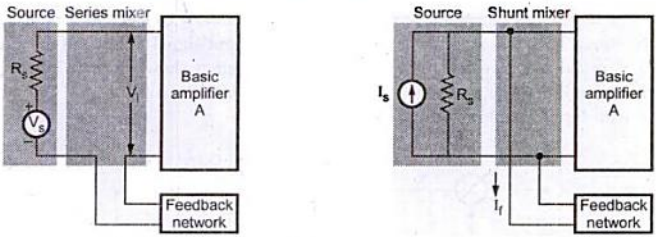

(a) Series mixing (b) Shunt mixing

Fig. 3.7

3.3.4 Transfer Ratio or Gain

In Fig. 3.5, the ratio of the output signal to the input signal of the basic amplifier is represented by the symbol A. The suffix of A given next, represents the different transfer ratios.

$$\frac{V}{V_i} = A_V = \text{Voltage gain} \quad \ldots (1)$$

$$\frac{I}{I_I} = A_I = \text{Current gain} \quad \ldots (2)$$

$$\frac{I}{V_I} = G_M = \text{Transconductance} \quad \ldots (3)$$

$$\frac{V}{I_i} = R_M = \text{Transresistance} \quad \ldots (4)$$

The four quantities A_V, A_I, G_M and R_M are referred to as a transfer gain of the basic amplifier without feedback and use of only symbol A represent any one of these quantities.

The transfer gain with feedback is represented by the symbol A_f. It is defined as the ratio of the output signal to the input signal of the amplifier configuration shown in Fig. 3.5. Hence A_f is used to represent any one of the following four ratios :

$$\frac{V_o}{V_s} = A_{Vf} = \text{Voltage gain with feedback} \quad \ldots (5)$$

$$\frac{I_o}{I_s} = A_{If} = \text{Current gain with feedback} \quad \ldots (6)$$

$$\frac{I_o}{V_s} = G_{Mf} = \text{Transconductance with feedback} \quad \ldots (7)$$

$$\frac{V_o}{I_s} = R_{Mf} = \text{Transresistance with feedback} \quad \ldots (8)$$

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Fig. 3.8 shows the schematic representation of a feedback connection around a basic amplifier. Recall that, when part of output signal and input signal are in out of phase the feedback is called **negative feedback**. The schematic diagram shown in Fig. 3.8 represents negative feedback because the feedback signal is fed back to the input of the amplifier out of phase with input signal of the amplifier.

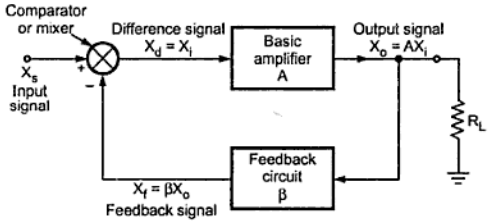

Fig. 3.8 Schematic representation of negative feedback amplifier

3.4 Ways of Introducing Negative Feedback in Amplifiers

The basic amplifier shown in Fig. 3.8 may be a voltage, current, transconductance, or transresistance amplifier. These can be connected in a feedback configuration as shown in the Fig. 3.9.

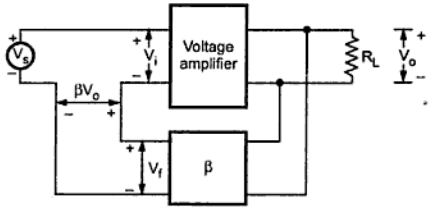

Fig. 3.9 (a) Voltage amplifier with voltage series feedback

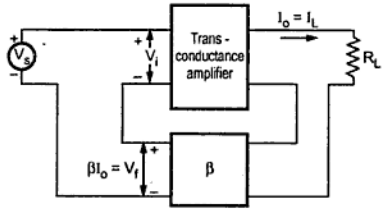

Fig. 3.9 (b) Transconductance amplifier with current series feedback

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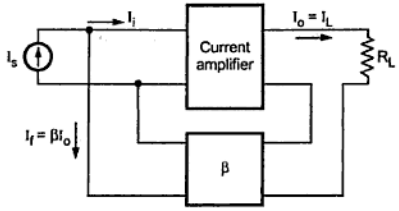

Fig. 3.9 (c) Current amplifier with current shunt feedback

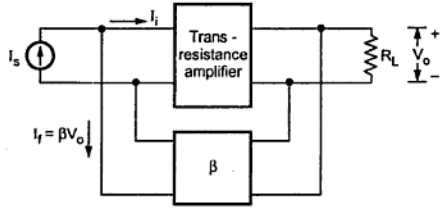

Fig. 3.9 (d) Transresistance amplifier with voltage shunt feedback

3.5 Effect of Negative Feedback

3.5.1 Transfer Gain

We have seen, the symbol A is used to represent transfer gain of the basic amplifier without feedback and symbol A_f is used to represent transfer gain of the basic amplifier with feedback. These are given as,

$$A = \frac{X_o}{X_i} \text{ and } A_f = \frac{X_o}{X_s}$$

where X_o = Output voltage or output current

X_i = Input voltage or input current

X_s = Source voltage or source current

As it is a negative feedback the relation between X_i and X_s is given as,

$$X_i = X_s + (- X_f)$$

where X_f = Feedback voltage or feedback current

$$\therefore \quad A_f = \frac{X_o}{X_s} = \frac{X_o}{X_i + X_f}$$

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Dividing by X_i to numerator and denominator we get,

$$A_f = \frac{X_o / X_i}{(X_i + X_f)/X_i}$$

$$= \frac{A}{1 + X_f / X_i} \quad \because A = \frac{X_o}{X_i}$$

$$= \frac{A}{1 + (X_f / X_o)(X_o / X_i)}$$

$$\therefore \quad A_f = \frac{A}{1 + \beta A} \quad \because \quad \beta = \frac{X_f}{X_o} \quad \ldots (1)$$

where β is a feedback factor.

Looking at equation we can say that gain without feedback (A) is always greater than gain with feedback ($A/(1 + \beta A)$) and it decreases with increase in β i.e. increase in feedback factor.

For voltage amplifier, gain with negative feedback is given as,

$$A_{Vf} = \frac{A_V}{1 + A_V \beta} \quad \ldots (2)$$

where A_V = Open loop gain i.e. gain without feedback

β = Feedback factor

3.5.2 Stability of Gain

The transfer gain of the amplifier is not constant as it depends on the factors such as operating point, temperature etc. This lack of stability in amplifiers can be reduced by introducing negative feedback.

We know that,

$$A_f = \frac{A}{1 + \beta A}$$

Differentiating both sides with respect to A we get,

$$\frac{dA_f}{dA} = \frac{(1 + \beta A)1 - \beta A}{(1 + \beta A)^2}$$

$$= \frac{1}{(1 + \beta A)^2}$$

$$\therefore \quad dA_f = \frac{dA}{(1 + \beta A)^2}$$

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Dividing both sides by A_f we get,

$$\frac{dA_f}{A_f} = \frac{dA}{(1+\beta A)^2} \times \frac{1}{A_f}$$

$$= \frac{dA}{(1+\beta A)^2} \times \frac{(1+\beta A)}{A_f} \quad \text{since } A_f = \frac{A}{1+\beta A}$$

$$\frac{dA_f}{A_f} = \frac{dA}{A} \frac{1}{(1+\beta A)} \quad \ldots (3)$$

where

$\frac{dA_f}{A_f}$ = Fractional change in amplification with feedback

$\frac{dA}{A}$ = Fractional change in amplification without feedback

Looking at equation (3) we can say that change in the gain with feedback is less than the change in gain without feedback by factor $(1+\beta A)$. The fractional change in amplification with feedback divided by the fractional change without feedback is called the **sensitivity of the transfer gain** $(1/(1+\beta A)$. The reciprocal of the sensitivity is called the **desensitivity D** $(1+\beta A)$.

Therefore, stability of the amplifier increases with increase in desensitivity.

If $\beta A >> 1$, then

$$A_f = \frac{A}{1+\beta A} = \frac{A}{\beta A}$$

$$= \frac{1}{\beta} \quad \ldots (4)$$

and the gain is dependant only on the feedback network.

Since A represents either A_V, G_M, A_I or R_M and A_f represents the corresponding transfer gains with feedback either A_{Vf}, G_{Mf}, A_{If} or R_{Mf} the equation signifies that :

- For voltage series feedback

$$A_{Vf} = \frac{1}{\beta} \quad \text{Voltage gain is stabilized.} \quad \ldots (5)$$

- For current series feedback

$$G_{Mf} = \frac{1}{\beta} \quad \text{Transconductance gain is stabilized.} \quad \ldots (6)$$

- For voltage shunt feedback

$$R_{Mf} = \frac{1}{\beta} \quad \text{Transresistance gain is stabilized.} \quad \ldots (7)$$

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- For current shunt feedback

$$A_{If} = \frac{1}{\beta} \quad \text{Current gain is stabilized.} \qquad \ldots (8)$$

3.5.3 Frequency Response and Bandwidth

We know that,

$$A_f = \frac{A}{1+\beta A}$$

Using this equation we can write,

$$A_{f\,mid} = \frac{A_{mid}}{1+\beta A_{mid}} \qquad \ldots (9)$$

$$A_{f\,low} = \frac{A_{low}}{1+\beta A_{low}} \qquad \ldots (10)$$

and $$A_{f\,high} = \frac{A_{high}}{1+\beta A_{high}} \qquad \ldots (11)$$

Now we analyze the effect of negative feedback on lower cut-off and upper cut-off frequency of the amplifier.

Lower cut-off frequency

We know that, the relation between gain at low frequency and gain at mid frequency, is given as,

$$\frac{A_{low}}{A_{mid}} = \frac{1}{1-j\left(\frac{f_L}{f}\right)} \quad \therefore \; A_{low} = \frac{A_{mid}}{1-j\left(\frac{f_L}{f}\right)} \qquad \ldots (12)$$

Substituting value of A_{low} in equation (10) we get,

$$A_{f\,low} = \frac{\frac{A_{mid}}{1-j\left(\frac{f_L}{f}\right)}}{1+\beta\left(\frac{A_{mid}}{1-j\left(\frac{f_L}{f}\right)}\right)} = \frac{A_{mid}}{1-j\left(\frac{f_L}{f}\right)+A_{mid}\beta}$$

$$= \frac{A_{mid}}{(1+A_{mid}\beta)-j\left(\frac{f_L}{f}\right)}$$

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Dividing numerator and denominator by $(1 + A_{mid}\,\beta)$ we get,

$$A_{f\,low} = \frac{\dfrac{A_{mid}}{1+A_{mid}\beta}}{1-j\left[\dfrac{f_L}{\dfrac{1+A_{mid}\beta}{f}}\right]}$$

$$= \frac{A_{f\,mid}}{1-j\left[\left(\dfrac{f_L}{\dfrac{1+A_{mid}\,\beta}{f}}\right)\right]} \quad \because\ A_{f\,mid} = \frac{A_{mid}}{1+A_{mid}\,\beta}$$

$$\therefore \quad \frac{A_{f\,low}}{A_{f\,mid}} = \frac{1}{1-j\left(\dfrac{f_{Lf}}{f}\right)} \qquad \ldots(13)$$

where

Lower cut-off frequency with feedback = $f_{Lf} = \dfrac{f_L}{1+A_{mid}\,\beta}$. ... (14)

From equation (14), we can say that lower cut-off frequency with feedback is less than lower cut-off frequency without feedback by factor $(1 + A_{mid}\,\beta)$. Therefore, by introducing negative feedback low frequency response of the amplifier is improved.

Upper Cut-off Frequency

We know that, the relation between gain at high frequency and gain at mid frequency is given as,

$$\frac{A_{high}}{A_{mid}} = \frac{1}{1-j\left(\dfrac{f}{f_H}\right)}$$

$$\therefore \quad A_{high} = \frac{A_{mid}}{1-j\left(\dfrac{f}{f_H}\right)} \qquad \ldots (15)$$

Substituting value of A_{high} in equation (11) we get,

$$A_{f\,high} = \frac{\dfrac{A_{mid}}{1-j\left(\dfrac{f}{f_H}\right)}}{1+\beta\left(\dfrac{A_{mid}}{1-j\left(\dfrac{f}{f_H}\right)}\right)} = \frac{A_{mid}}{1-j\left(\dfrac{f}{f_H}\right)+A_{mid}\beta}$$

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Dividing numerator and denominator by $(1 + A_{mid}\,\beta)$ we get,

$$A_{f\,high} = \frac{\dfrac{A_{mid}}{1+A_{mid}\,\beta}}{1-j\left[\dfrac{f}{(1+A_{mid}\beta)\,f_H}\right]}$$

$$A_{f\,high} = \frac{A_{f\,mid}}{1-j\left[\dfrac{f}{(1+A_{mid}\beta)\,f_H}\right]} \quad \because A_{f\,mid} = \frac{A_{mid}}{1+A_{mid}\beta}$$

$$= \frac{A_{f\,mid}}{1-j\left(\dfrac{f}{f_{Hf}}\right)}$$

where upper cut-off frequency with feedback is given as,

$$f_{Hf} = (1+A_{mid}\,\beta)\,f_H \qquad \ldots (16)$$

From equation (16), we can say that upper cut-off frequency with feedback is greater than upper cut-off frequency without feedback by factor $(1+A_{mid}\,\beta)$. Therefore, by introducing negative feedback high frequency response of the amplifier is improved.

Bandwidth

The bandwidth of the amplifier is given as,

BW = Upper cut-off frequency – Lower cut-off frequency

∴ Bandwidth of the amplifier with feedback is given as,

$$BW_f = f_{Hf} - f_{Lf} = (1+A_{mid}\,\beta)\,f_H - \frac{f_L}{(1+A_{mid}\,\beta)} \qquad \ldots (17)$$

It is very clear that $(f_{Hf} - f_{Lf}) > (f_H - f_L)$ and hence bandwidth of amplifier with feedback is greater than bandwidth of amplifier without feedback, as shown in Fig. 3.10.

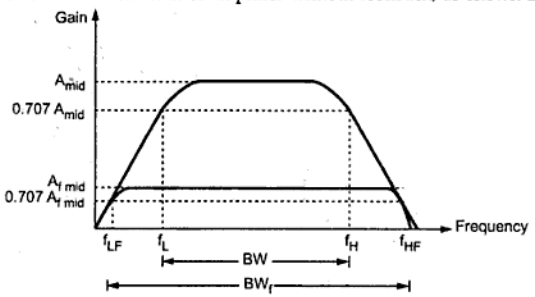

Fig. 3.10 Effect of negative feedback on gain and bandwidth

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3.5.4 Frequency Distortion

From equation (8) we can say that if the feedback network does not contain reactive elements, the overall gain is not a function of frequency. Under such conditions frequency and phase distortion is substantially reduced.

If β is made up of reactive components, the reactances of these components will change with frequency, changing the β. As a result, gain will also change with frequency. This fact is used in tuned amplifiers. In tuned amplifiers, feedback network is designed such that at tuned frequency $\beta \to 0$ and at other frequencies $\beta \to \infty$. As a result, amplifier provides high gain for signal at tuned frequency and relatively reject all other frequencies.

3.5.5 Noise and Nonlinear Distortion

Signal feedback reduces the amount of noise signal and nonlinear distortion. The factor $(1+\beta A)$ reduces both input noise and resulting nonlinear distortion for considerable improvement. Thus, noise and nonlinear distortion also reduced by same factor as the gain.

3.5.6 Input and Output Resistances

Input resistance

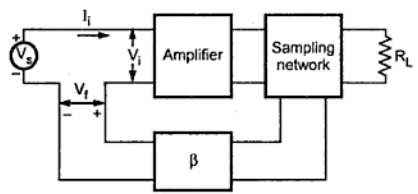

Fig. 3.11

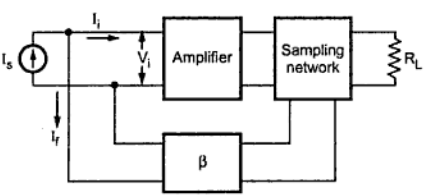

Fig. 3.12

If the feedback signal is added to the input in series with the applied voltage (regardless of whether the feedback is obtained by sampling the output current or voltage), it increases the input resistance. Since the feedback voltage V_f opposes V_s, the input current I_i is less than it would be if V_f were absent, as shown in the Fig. 3.11.

Hence, the input resistance with feedback $R_{if} = \frac{V_s}{I_i}$ is greater than the input resistance without feedback, for the circuit shown in Fig. 3.11.

On the other hand, if the feedback signal is added to the input in shunt with the applied voltage (regardless of whether the feedback is obtained by sampling the output voltage or current), it decreases the input resistance. Since $I_s = I_i + I_f$, the current I_s drawn from the signal source is increased over what it would be if there were no feedback current, as shown in the Fig. 3.12.

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Hence, the input resistance with feedback $R_{if} = \frac{V_i}{I_s}$ is decreased for the circuit shown in Fig. 3.12. Now we see the effect of negative feedback on input resistance in different topologies (ways) of introducing negative feedback and obtain R_{if} quantitatively.

Voltage series feedback

The voltage series feedback topology shown in Fig. 3.13 with amplifier is replaced by Thevenin's model. Here, A_v represents the open circuit voltage gain taking R_s into account. since throughout the discussion of feedback amplifiers we will consider R_s to be part of the amplifier and we will drop the subscript on the transfer gain and input resistance (A_v instead of A_{vs} and R_{if} instead of R_{ifs}).

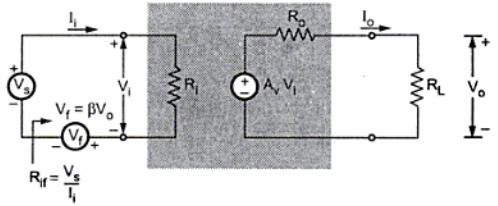

Fig. 3.13

Look at Fig. 3.13 the input resistance with feedback is given as,

$$R_{if} = \frac{V_s}{I_i} \quad \ldots (18)$$

Applying KVL to the input side we get,

$$V_s - I_i R_i - V_f = 0$$

$$\therefore \quad V_s = I_i R_i + V_f$$

$$= I_i R_i + \beta V_o \quad \ldots (19)$$

The output voltage V_o is given as,

$$V_o = \frac{A_v V_i R_L}{R_o + R_L}$$

$$= A_V I_i R_i = A_V V_i \quad \ldots (20)$$

where $$A_V = \frac{V_o}{V_i} = \frac{A_v R_L}{R_o + R_L}$$

Key Point: *A_v represents the open circuit voltage gain without feedback and A_V is the voltage gain without feedback taking the load R_L into account.*

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Substituting value of V_o from equation (20) in equation (19) we get,

$$V_s = I_i R_i + \beta A_V I_i R_i$$

$$\therefore \quad \frac{V_s}{I_i} = R_i + \beta A_V R_i$$

$$\therefore \quad R_{if} = R_i (1 + \beta A_V) \qquad \ldots (21)$$

Current series feedback

The current series feedback topology is shown in Fig. 3.14 with amplifier input circuit is represented by Thevenin's equivalent circuit and output circuit by Norton's equivalent circuit.

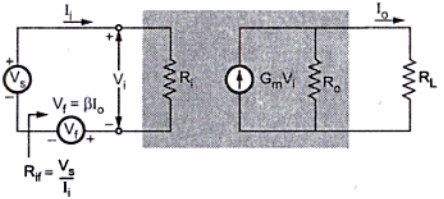

Fig. 3.14

Looking at Fig. 3.14 the input resistance with feedback is given as,

$$R_{if} = \frac{V_s}{I_i}$$

Applying KVL to the input side we get,

$$V_s - I_i R_i - V_f = 0$$

$$\therefore \quad V_s = I_i R_i + V_f = I_i R_i + \beta I_o \qquad \ldots (22)$$

The output current I_o is given as,

$$I_o = \frac{G_m V_i R_o}{R_o + R_L} = G_M V_i \qquad \ldots (23)$$

where $$G_M = \frac{I_o}{V_i}$$

$$G_M = \frac{G_m R_o}{R_o + R_L}$$

Key Point: *G_m represents the open circuit transconductance without feedback and G_M is the transconductance without feedback taking the load R_L into account.*

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Substituting value of I_o from equation (23) into equation (22) we get,

$$V_s = I_i R_i + \beta G_M V_i$$

$$= I_i R_i + \beta G_M I_i R_i \quad \because V_i = I_i R_i$$

$$\therefore \quad \frac{V_s}{I_i} = R_i (1 + \beta G_M)$$

$$\therefore \quad R_{if} = \frac{V_s}{I_i} = R_i (1 + \beta G_M) \qquad \ldots (24)$$

Current shunt feedback

The current shunt feedback topology is shown in Fig. 3.15 with amplifier input and output circuit replaced by Norton's equivalent circuit

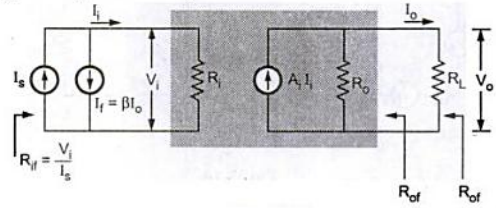

Fig. 3.15

Applying KCL to the input node we get,

$$I_s = I_i + I_f$$

$$= I_i + \beta I_o \qquad \ldots (25)$$

The output current I_o is given as,

$$I_o = \frac{A_i I_i R_o}{R_o + R_L}$$

$$= A_I I_i \qquad \ldots (26)$$

where $$A_I = \frac{A_i R_o}{R_o + R_L}$$

Key Point: A_i *represents the open circuit current gain without feedback and* A_I *is the current gain without feedback taking the load* R_L *into account.*

Substituting value of I_o from equation (26) into equation (25) we get,

$$I_s = I_i + \beta A_I I_i$$

$$= I_i (1 + \beta A_I)$$

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The input resistance with feedback is given as,

$$R_{if} = \frac{V_i}{I_s} = \frac{V_i}{I_i (1+\beta A_I)}$$

$$= \frac{R_i}{(1+\beta A_I)} \qquad \because R_i = \frac{V_i}{I_i} \qquad \ldots (27)$$

Voltage shunt feedback

The voltage shunt feedback topology is shown in Fig. 3.16 with amplifier input circuit is represented by Norton's equivalent circuit and output circuit represented by Thevenin's equivalent.

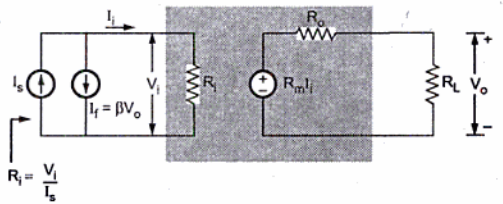

Fig. 3.16

Applying KCL at input node we get,

$$I_s = I_i + I_f$$

$$= I_i + \beta V_o \qquad \ldots (28)$$

The output voltage V_o is given as,

$$V_o = \frac{R_m I_i R_o}{R_o + R_L}$$

$$= R_M I_i \qquad \ldots (29)$$

where $$R_M = \frac{R_m R_o}{R_o + R_L}$$

Key Point: *R_m represents the open circuit transresistance without feedback and R_M is the transresistance without feedback taking the load R_L into account.*

Substituting value of V_o from equation (29) into equation (28) we get,

$$I_s = I_i + \beta R_M I_i$$

$$= I_i (1 + \beta R_M)$$

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The input resistance with feedback R_{if} is given as,

$$R_{if} = \frac{V_i}{I_s} = \frac{V_i}{I_i(1+\beta R_M)}$$

$$\therefore \quad R_{if} = \frac{R_i}{(1+\beta R_M)} \qquad \because R_i = \frac{V_i}{I_i} \qquad \ldots (30)$$

Output resistance

The negative feedback which samples the output voltage, regardless of how this output signal is returned to the input, tends to decrease the output resistance, as shown in the Fig. 3.17.

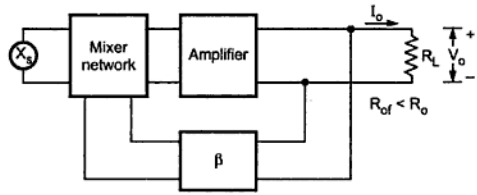

Fig. 3.17

On the other hand, the negative feedback which samples the output current, regardless of how this output signal is returned to the input, tends to increase the output resistance, as shown in the Fig. 3.18.

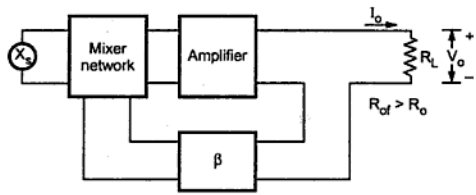

Fig. 3.18

Now, we see the effect of negative feedback on output resistance in different topologies (ways) of introducing negative feedback and obtain R_{of} quantitatively.

Voltage series feedback

In this topology, the output resistance can be measured by shorting the input source $V_s = 0$ and looking into the output terminals with R_L disconnected, as shown in the Fig. 3.19.

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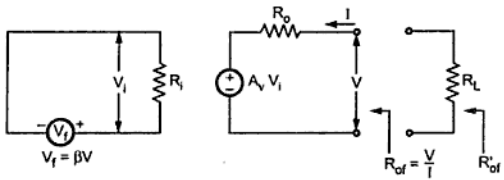

Fig. 3.19

Applying KVL to the output side we get,

$$A_v V_i + I R_o - V = 0$$

$$\therefore \quad I = \frac{V - A_v V_i}{R_o} \qquad \ldots (31)$$

The input voltage is given as,

$$V_i = -V_f = -\beta V \quad \because V_s = 0 \qquad \ldots (32)$$

Substituting the V_i from equation (32) in equation (31) we get,

$$I = \frac{V + A_v \beta V}{R_o}$$

$$= \frac{V(1 + \beta A_v)}{R_o}$$

$$\therefore \quad R_{of} = \frac{V}{I}$$

$$= \frac{R_o}{(1 + \beta A_v)} \qquad \ldots (33)$$

Key Point: *Here A_v is the open loop voltage gain without taking R_L in account.*

$$R'_{of} = R_{of} \parallel R_L$$

$$= \frac{R_{of} \times R_L}{R_{of} + R_L} = \frac{\left(\frac{R_o}{1+\beta A_v}\right) \times R_L}{\frac{R_o}{(1+\beta A_v)} + R_L}$$

$$= \frac{R_o R_L}{R_o + R_L(1+\beta A_v)} = \frac{R_o R_L}{R_o + R_L + \beta A_v R_L}$$

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Dividing numerator and denominator by $(R_o + R_L)$ we get

$$R'_{of} = \frac{\frac{R_o R_L}{R_o + R_L}}{1 + \frac{\beta A_v R_L}{R_o + R_L}}$$

$$= \frac{R'_o}{1 + \beta A_v} \qquad \because R'_o = \frac{R_o R_L}{R_o + R_L} \text{ and } A_v = \frac{A_v R_L}{R_o + R_L} \qquad \ldots (34)$$

Key Point : *Here A_v is the open loop voltage gain taking R_L into account.*

Voltage shunt feedback

In this topology, the output resistance can be measured by shorting the input source $V_s = 0$ and looking into the output terminals with R_L disconnected, as shown in the Fig. 3.20.

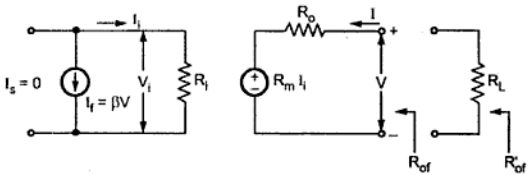

Fig. 3.20

Applying KVL to the output side we get,

$$R_m I_i + I R_o - V = 0$$

$$\therefore \quad I = \frac{V - R_m I_i}{R_o} \qquad \ldots (35)$$

The input current is given as,

$$I_i = -I_f = -\beta V \qquad \ldots (36)$$

Substituting I_i from equation (36) in equation (35) we get,

$$I = \frac{V + R_m \beta V}{R_o} = \frac{V(1 + R_m \beta)}{R_o}$$

$$\therefore \quad R_{of} = \frac{V}{I}$$

$$= \frac{R_o}{1 + R_m \beta} \qquad \ldots (37)$$

Key Point: *Here, R_m is the open loop transresistance without taking R_L in account.*

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$$R'_{of} = R_{of} \parallel R_L = \frac{R_{of} \times R_L}{R_{of} + R_L}$$

$$= \frac{\frac{R_o \times R_L}{1 + R_m \beta}}{\frac{R_o}{1 + R_m \beta} + R_L} = \frac{R_o R_L}{R_o + R_L (1 + R_m \beta)}$$

Dividing numerator and denominator by $R_o + R_L$ we get,

$$R'_{of} = \frac{\frac{R_o R_L}{R_o + R_L}}{1 + \frac{\beta R_m R_L}{R_o + R_L}}$$

$$= \frac{R'_o}{1 + \beta R_M} \quad \because R'_o = \frac{R_o R_L}{R_o + R_L} \text{ and } R_M = \frac{R_m R_L}{R_o + R_L} \quad \ldots (38)$$

Key Point: *Here, R_M is the open loop transresistance taking R_L in account.*

Current shunt feedback

In this topology, the output resistance can be measured by open circuiting the input source $I_s = 0$ and looking into the output terminals, with R_L disconnected, as shown in the Fig. 3.21.

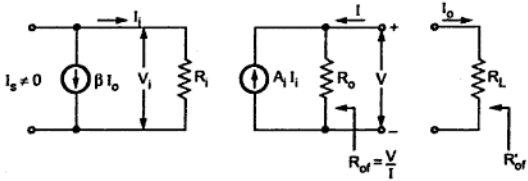

Fig. 3.21

Applying the KCL to the output node we get,

$$I = \frac{V}{R_o} - A_i I_i \quad \ldots (39)$$

The input current is given as,

$$I_i = -I_f = -\beta I_o \quad \because I_s = 0$$
$$= \beta I \quad \because I = -I_o \quad \ldots (40)$$

Substituting value of I_i from equation (40) in equation (39) we get,

$$I = \frac{V}{R_o} - A_i \beta I$$

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$$\therefore \quad I(1+A_i\beta) = \frac{V}{R_o}$$

$$\therefore \quad R_{of} = \frac{V}{I} = R_o(1+\beta A_i) \qquad \ldots (41)$$

Key Point: *Here, A_i is the open loop current gain without taking R_L in account.*

$$R'_{of} = R_{of} \,||\, R_L = \frac{R_{of} \times R_L}{R_{of} + R_L}$$

$$= \frac{R_o(1+\beta A_i)R_L}{R_o(1+\beta A_i)+R_L} = \frac{R_o R_L (1+\beta A_i)}{R_o + R_L + \beta A_i R_o}$$

Dividing numerator and denominator by $R_o + R_L$ we get,

$$R'_{of} = \frac{\dfrac{R_o R_L (1+\beta A_i)}{R_o + R_L}}{1+\dfrac{\beta A_i R_o}{R_o + R_L}} = \frac{R'_o(1+\beta A_i)}{(1+\beta A_I)}$$

$$\because \quad R'_o = \frac{R_o R_L}{R_o + R_L} \text{ and } A_I = \frac{A_i R_o}{R_o + R_L} \qquad \ldots (42)$$

Key Point: *Here, A_I is the open loop current gain taking R_L in account.*

Current series feedback

In this topology the output resistance can be measured by shorting the input source $V_s = 0$ and looking into the output terminals with R_L disconnected, as shown in the Fig. 3.22.

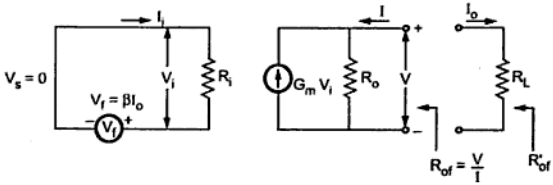

Fig. 3.22

Applying KCL to the output node we get,

$$I = \frac{V}{R_o} - G_m V_i \qquad \ldots (43)$$

The input voltage is given as, $V_i = -V_f = -\beta I_o$

$$= \beta I \qquad \because I_o = -I \qquad \ldots (44)$$

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Substituting value of V_i from equation (44) in equation (43) we get,

$$I = \frac{V}{R_o} - G_m \beta I$$

$$\therefore \quad I(1 + G_m \beta) = \frac{V}{R_o}$$

$$\therefore \quad R_{of} = \frac{V}{I} = R_o (1 + G_m \beta) \qquad \ldots (45)$$

Key Point: *Here, G_m is the open loop transconductance without taking R_L in account.*

$$R'_{of} = R_{of} \parallel R_L = \frac{R_{of} \times R_L}{R_{of} + R_L}$$

$$= \frac{R_o (1+\beta G_m) R_L}{R_o (1+\beta G_m) + R_L} = \frac{R_o R_L (1+\beta G_m)}{R_o + R_L + \beta G_m R_o}$$

Dividing numerator and denominator by $R_o + R_L$ we get,

$$R'_{of} = \frac{\frac{R_L R_o (1+\beta G_m)}{R_o + R_L}}{1 + \frac{\beta G_m R_o}{R_o + R_L}}$$

$$= \frac{R'_o (1+\beta G_m)}{1+\beta G_M} \quad \because R'_o = \frac{R_o R_L}{R_o + R_L} \text{ and } G_M = \frac{G_m R_o}{R_o + R_L} \qquad \ldots (46)$$

Key Point: *Note that here, G_M is the open loop current gain taking R_L in account.*

Table 3.1 summarizes the effect of negative feedback on amplifier.

Parameter	Voltage series	Current series	Current shunt	Voltage shunt
Gain with feedback	$A_{vf} = \frac{A_v}{1+\beta A_v}$ decreases	$G_{mf} = \frac{G_m}{1+\beta G_m}$ decreases	$A_{if} = \frac{A_i}{1+\beta A_i}$ decreases	$R_{mf} = \frac{R_m}{1+\beta R_{mf}}$ decreases
Stability	Improves	Improves	Improves	Improves
Frequency response	Improves	Improves	Improves	Improves
Frequency distortion	Reduces	Reduces	Reduces	Reduces
Noise and Nonlinear distortion	Reduces	Reduces	Reduces	Reduces
Input resistance	$R_{if} = R_i(1+\beta A_v)$ increases	$R_{if} = R_i(1+\beta G_M)$ increases	$R_{if} = \frac{R_i}{1+\beta A_I}$ decreases	$R_{if} = \frac{R_i}{1+\beta R_M}$ decreases
Output resistance	$R_{of} = \frac{R_o}{1+\beta A_v}$ decreases	$R_{of} = R_o(1+\beta G_m)$ increases	$R_{of} = R_o(1+\beta A_i)$ increases	$R_{of} = \frac{R_o}{1+\beta R_m}$ decreases

Table 3.1

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Characteristics	Topology			
	Voltage series	Current series	Current shunt	Voltage shunt
Feedback signal X_f	Voltage	Voltage	Current	Current
Sampled signal X_o	Voltage	Current	Current	Voltage
To find input loop, set	$V_o = 0$	$I_o = 0$	$I_o = 0$	$V_o = 0$
To find output loop, set	$I_i = 0$	$I_i = 0$	$V_i = 0$	$V_i = 0$
Single source	Thevenin	Thevenin	Norton	Norton
$\beta = X_f / X_o$	V_f / V_o	V_f / I_o	I_f / I_o	I_f / V_o
$A = X_o / X_i$	$A_V = V_o / V_i$	$G_M = I_o / V_i$	$A_I = I_o / I_i$	$R_M = V_o / I_i$
$D = 1 + \beta A$	$1 + \beta A_V$	$1 + \beta G_M$	$1 + \beta A_I$	$1 + \beta R_M$
A_f	A_V/D	G_M/D	A_I/D	R_M/D
R_{if}	R_iD	R_iD	R_i/D	R_i/D
R_{of}	$\frac{R_o}{1+\beta A_v}$	$R_o (1 + \beta G_m)$	$R_o (1 + \beta A_i)$	$\frac{R_o}{1+\beta R_m}$
$R'_{of} = R_{of} \parallel R_L$	$\frac{R'_o}{1+\beta A_V}$	$\frac{R'_o(1+\beta G_m)}{1+\beta G_M}$	$\frac{R'_o(1+\beta A_i)}{1+\beta A_I}$	$\frac{R'_o}{1+\beta R_M}$

Table 3.2

3.8 Voltage Series Feedback

In this section, we will see two examples of the voltage series amplifier. First we will analyze transistor emitter follower circuit and then source follower using FET.

3.8.1 Transistor Emitter Follower

Fig. 3.23 shows the transistor emitter follower circuit. Here feedback voltage is the voltage across R_o and sampled signal is V_o across R_e.

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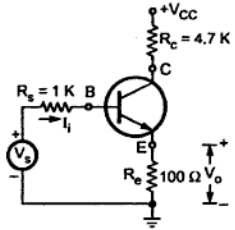

Fig. 3.23

Analysis

Step 1 : Identify topology.

By shorting output voltage ($V_o = 0$), feedback signal becomes zero and hence it is voltage sampling. Looking at Fig. 3.23 we can see that feedback signal V_f is subtracted from the externally applied signal V_s and hence it is a series mixing. Combining two conclusions we can say that it is a voltage series feedback amplifier.

Step 2 and Step 3 : Find input and output circuit.

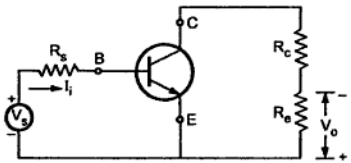

Fig. 3.24

To find the input circuit, set $V_o = 0$, and hence V_s in series with R_s appears between B and E. To find the output circuit, set $I_i = I_b = 0$, and hence R_c appears only in the output loop. With these connections we obtain the circuit as shown in the Fig. 3.24.

Step 4 : Replace transistor by its h-parameter equivalent circuit.

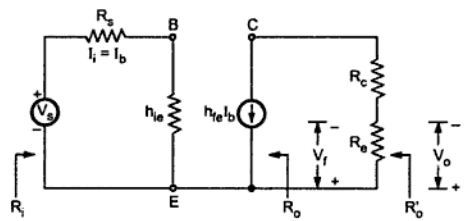

Fig. 3.25 Transistor replaced by its approximate h-parameter equivalent circuit

Step 5 : Find open loop voltage gain.

$$A_V = \frac{V_o}{V_s} = \frac{h_{fe} I_b R_c}{V_s}$$

Applying KVL to input loop we get,

$$V_s = I_b (R_s + h_{ic})$$

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Substituting value of V_s we get,

$$A_V = \frac{h_{fe} R_e}{R_s + h_{ie}} = \frac{50 \times 100}{1\,K + 1.1\,K} = 2.38$$

Step 6 : Indicate V_o and V_f and calculate β.

We have $\beta = \frac{V_f}{V_o} = 1$ $\because$ Both voltage present across R_e.

Step 7 : Calculate D, A_{Vf} , R_{if} , R_{of} and R'_{of}.

$$D = 1 + \beta A_V$$
$$= 1 + 1 \times 2.38$$
$$= 3.38$$
$$A_{Vf} = \frac{A_V}{1 + \beta A_V}$$
$$= \frac{A_V}{D} = \frac{2.38}{3.38}$$
$$= 0.7$$
$$R_i = R_s + h_{ie}$$
$$= 1\,K + 1.1\,K = 2.1\,K$$
$$R_{if} = R_i\, D$$
$$= 2.1\,K \times 3.38$$
$$= 7.098\,K$$
$$R_o = \infty$$
$$R_{of} = \infty$$
$$R'_{of} = \frac{R'_o}{D} \quad \text{where } R'_o = R_e$$

$\therefore$
$$R'_{of} = \frac{R_e}{D} = \frac{100}{3.38}$$
$$= 29.58\ \Omega$$

3.8.2 FET Source Follower

Fig. 3.26 shows the FET source follower circuit. Here feedback voltage is the voltage across R_s and sampled signal is V_o across R_e.

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Analysis :

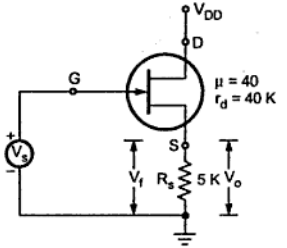

Fig. 3.26

Step 1 : Identify topology.

By shorting output voltage $V_o = 0$, feedback signal becomes zero and hence it is voltage sampling. Looking at Fig. 3.26 we can see that feedback signal V_f is subtracted from the externally applied signal V_s and hence it is a series mixing. Combining two conclusions we can say that it is a voltage series feedback amplifier.

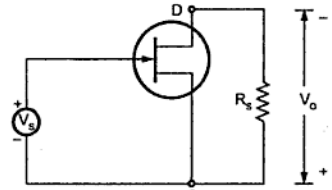

Fig. 3.27

Step 2 and Step 3 : Find input and output circuit.

To find the input circuit, set $V_s = 0$, and hence V_s appears between G and S. To find the output circuit, set $I_i = I_G = 0$, and hence R_s appears in the output loop. With these connections we obtain the circuit as shown in the Fig. 3.27.

Step 4 : Replace FET by its equivalent circuit.

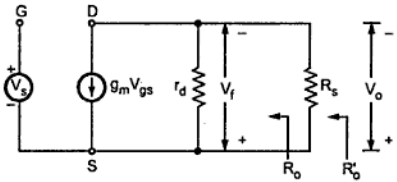

Fig. 3.28

Step 5 : Find open loop voltage gain.

$$A_V = \frac{V_o}{V_s} = \frac{g_m V_{gs} r_d R_s}{(r_d + R_s) V_s}$$

$$= \frac{g_m r_d R_s}{r_d + R_s} \quad \because V_{gs} = V_s \quad \ldots (1)$$

$$= \frac{\mu R_s}{r_d + R_s} \quad \because \mu = g_m r_d \quad \ldots (2)$$

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4 Oscillators

4.1 Introduction

Feedback plays an important role in almost all electronic circuits. It is almost invariably used in the amplifier to improve its performance and to make it more ideal. In the process of feedback, a part of output is sampled and fed back to the input of the amplifier. Therefore, at input we have two signals : Input signal, and part of the output which is fed back to the input. Both these signals may be in phase or out of phase. When input signal and part of output signal are in phase, the feedback is called **positive feedback**. On the other hand, when they are out of phase, the feedback is called **negative feedback.**

The positive feedback results into oscillations and hence used in electronic circuits to generate the oscillations of desired frequency. Such circuits are called oscillators.

4.2 Concept of Positive Feedback

The feedback is a property which allows to feedback the part of the output, to the same circuit as its input. Such a feedback is said to be positive whenever the part of the output that is fed back to the amplifier as its input, is in phase with the original input signal applied to the amplifier. Consider a non-inverting amplifier with the voltage gain A as shown in the Fig. 4.1.

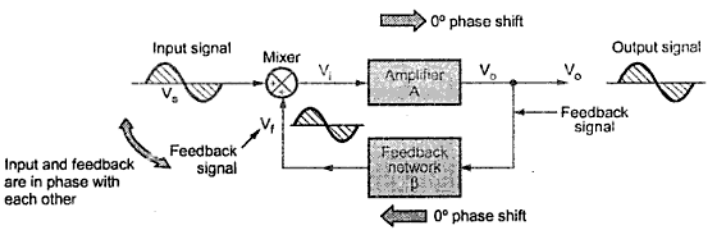

Fig. 4.1 Concept of positive feedback

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Assume that a sinusoidal input signal (voltage) V_s is applied to the circuit. As amplifier is non-inverting, the output voltage V_o is in phase with the input signal V_s. The part of the output is fed back to the input with the help of a feedback network. How much part of the output is to be fed back, gets decided by the feedback network gain β. No phase change is introduced by the feedback network. Hence the feedback voltage V_f is in phase with the input signal V_s.

Key Point: *As the phase of the feedback signal is same as that of the input applied, the feedback is called positive feedback.*

4.2.1 Expression for Gain with Feedback

The amplifier gain is A i.e. it amplifies its input V_i, A times to produce output V_o.

$$\therefore \quad \boxed{A = \frac{V_o}{V_i}}$$

This is called **open loop gain** of the amplifier.

For the overall circuit, the input is supply voltage V_s and net output is V_o. The ratio of output V_o to input V_s considering effect of feedback is called **closed loop gain** of the circuit or **gain with feedback** denoted as A_f.

$$\therefore \quad \boxed{A_f = \frac{V_o}{V_s}}$$

The feedback is positive and voltage V_f is added to V_s to generate input of amplifier V_i. So referring Fig. 4.1 we can write,

$$\boxed{V_i = V_s + V_f} \qquad \ldots(1)$$

The feedback voltage V_f depends on the feedback element gain β. So we can write,

$$\boxed{V_f = \beta V_o} \qquad \ldots(2)$$

Substituting (2) in (1),

$$V_i = V_s + \beta V_o$$

$$\therefore \quad V_s = V_i - \beta V_o \qquad \ldots (3)$$

Substituting in expression for A_f,

$$A_f = \frac{V_o}{V_i - \beta V_o}$$

Dividing both numerator and denominator by V_i,

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$$\therefore \quad A_f = \frac{(V_o / V_i)}{1 - \beta (V_o / V_i)}$$

$$\therefore \quad \boxed{A_f = \frac{A}{1 - A\beta}} \qquad \ldots \text{ as } A = \frac{V_o}{V_i}$$

Now consider the various values of β and the corresponding values of A_f for constant amplifier gain of A = 20.

A	β	A_f
20	0.005	22.22
20	0.04	100
20	0.045	200
20	0.05	∞

Table 4.1

Conclusions :

The above result shows that the gain with feedback increases as the amount of positive feedback increases. In the limiting case, the gain becomes infinite. This indicates that circuit can produce output without external input ($V_s = 0$), just by feeding the part of the output as its own input. Similarly, output cannot be infinite but gets driven into the oscillations. In other words, the circuit stops amplifying and starts oscillating.

Key Point: *Thus without an input, the output will continue to oscillate whose frequency depends upon the feedback network or the amplifier or both. Such a circuit is called as an oscillator.*

It must be noted that β the feedback network gain is always a fraction and hence $\beta < 1$. So the feedback network is an attenuation network. To start with the oscillations $A\beta > 1$ but the circuit adjusts itself to get $A\beta = 1$, when it produces sinusoidal oscillations while working as an oscillator.

An oscillator is an amplifier, which uses a positive feedback and without any external input signal, generates an output waveform, at a desired frequency.

An oscillator is a circuit which basically acts as a generator, generating the output signal which oscillates with constant amplitude and constant desired frequency. An oscillator does not require any input signal. An electrical device, alternator generates a sinusoidal voltage at a desired frequency of 50 Hz in our nation but electronic oscillator can generate a voltage of any desired waveform at any frequency. An oscillator can generate the output waveform of high frequency upto gigahertz.

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4.3 Barkhausen Criterion

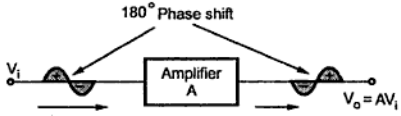

Fig. 4.2 Inverting amplifier

Consider a basic inverting amplifier with an open loop gain A. The feedback network attenuation factor β is less than unity. As basic amplifier is inverting, it produces a phase shift of 180° between input and output as shown in the Fig. 4.2.

Now the input V_i applied to the amplifier is to be derived from its output V_o using feedback network.

But the feedback must be positive i.e. the voltage derived from output using feedback network must be in phase with V_i. Thus the feedback network must introduce a phase shift of 180° while feeding back the voltage from output to input. This ensures positive feedback.

The arrangement is shown in the Fig. 4.3.

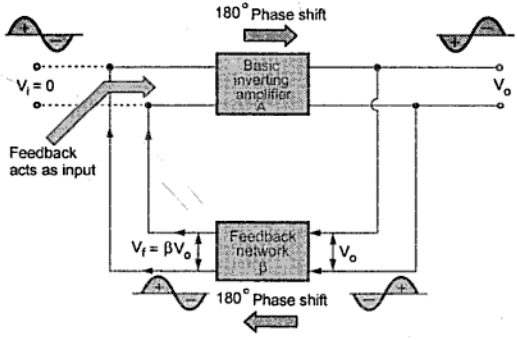

Fig. 4.3 Basic block diagram of oscillator circuit

Consider a fictitious voltage V_i applied at the input of the amplifier. Hence we get,

$$V_o = A\, V_i \qquad \ldots(1)$$

The feedback factor β decides the feedback to be given to input,

$$V_f = \beta\, V_o \qquad \ldots(2)$$

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Substituting (1) into (2) we get,

$$\boxed{V_f = A\,\beta\,V_i} \quad \ldots(3)$$

For the oscillator, we want that feedback should drive the amplifier and hence V_f must act as V_i. From equation (3) we can write that, V_f is sufficient to act as V_i when,

$$\boxed{|\,A\,\beta\,| = 1} \quad \ldots(4)$$

And the phase of V_f is same as V_i i.e. feedback network should introduce 180° phase shift in addition to 180° phase shift introduced by inverting amplifier. This ensures positive feedback. So total phase shift around a loop is 360°.

In this condition, V_f drives the circuit and without external input circuit works as an oscillator.

The two conditions discussed above, required to work the circuit as an oscillator are called **Barkhausen Criterion** for oscillation.

The **Barkhausen Criterion** states that :

1. The total phase shift around a loop, as the signal proceeds from input through amplifier, feedback network back to input again, completing a loop, is precisely 0° or 360°.
2. The magnitude of the product of the open loop gain of the amplifier (A) and the magnitude of the feedback factor β is unity i.e. $|\,A\,\beta\,| = 1$.

Satisfying these conditions, the circuit works as an oscillator producing sustained oscillations of constant frequency and amplitude.

In reality, no input signal is needed to start the oscillations. In practice, Aβ is made greater than 1 to start the oscillations and then circuit adjusts itself to get Aβ =1, finally resulting into self sustained oscillations. Let us see the effect of the magnitude of the product Aβ on the nature of the oscillations.

4.3.1 $|A\beta| > 1$

When the total phase shift around a loop is 0° or 360° and $|A\beta| > 1$, then the output oscillates but the oscillations are of growing type. The amplitude of oscillations goes on increasing as shown in the Fig. 4.4.

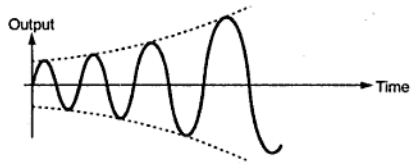

Fig. 4.4 Growing type oscillations

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4.3.2 | Aβ | = 1

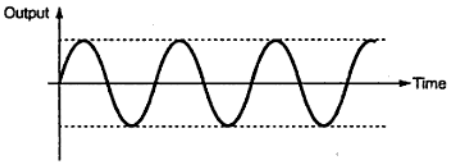

Fig. 4.5 Sustained oscillations

As stated by Barkhausen criterion, when total phase shift around a loop is 0° or 360° ensuring positive feedback and |A β| = 1 then the oscillations are with constant frequency and amplitude called sustained oscillations.

Such oscillations are shown in the Fig. 4.5.

4.3.3 | Aβ | < 1

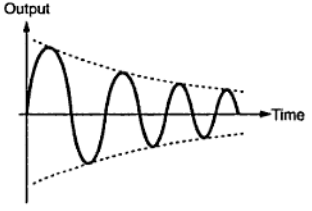

Fig. 4.6 Exponentially decaying oscillations

When total phase shift around a loop is 0° or 360° but |Aβ| < 1 then the oscillations are of decaying type i.e. such oscillation amplitude decreases exponentially and the oscillations finally cease. Thus circuit works as an amplifier without oscillations. The decaying oscillations are shown in the Fig. 4.6.

So to start the oscillations without input, |Aβ| is kept higher than unity and then circuit adjusts itself to get |Aβ| = 1 to result sustained oscillations.

4.3.4 Starting Voltage

It is mentioned that no external input is required in case of oscillators. In the earlier analysis also, the input V_i is assumed as fictitious input and practically no such input is required. The oscillator output supplies its own input under proper conditions. The obvious question is if no input is required, how oscillator starts ? And where does the starting voltage come from ?

Every resistance has some free electrons. Under the influence of normal room temperature, these free electrons move randomly in various directions. Such a movement of the free electrons generate a voltage called **noise voltage**, across the resistance. Such noise voltages present across the resistances are amplified. Hence to amplify such small noise voltages and to start the oscillations, |Aβ| is kept greater than unity at start. Such amplified voltage appears at the output terminals. The part of this output is sufficient to drive the input of amplifier circuit. Then circuit adjusts itself to get |Aβ| = 1 and with phase shift of 360° we get sustained oscillations.

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4.4 Classification of Oscillators

The oscillators are classified based on the nature of the output waveform, the parameters used, the range of frequency etc. The various ways in which oscillators are classified as :

4.4.1 Based on the Output Waveform

Under this, the oscillators are classified as sinusoidal and nonsinusoidal oscillators. The sinusoidal oscillators generate purely sinusoidal waveform at the output. While nonsinusoidal oscillators generate an output waveform as triangular, square, sawtooth etc. In this chapter, we are going to discuss only sinusoidal oscillators.

4.4.2 Based on the Circuit Components

The oscillators using the components resistance (R) and capacitor (C), are called RC oscillators. While the oscillators using the components inductance (L) and capacitor (C), are called LC oscillators. In some oscillators, crystal is used, which are called crystal oscillators.

4.4.3 Based on the Range of Operating Frequency

If the oscillators are used to generate the oscillations at audio frequency range which is 20 Hz to 100 - 200 kHz, then the oscillators are classified as low frequency (L.F.) or audio frequency (A.F.) oscillators. While the oscillators used at the frequency range more than 200 - 300 kHz upto gigahertz (GHz) are classified as high frequency (H.F.) or radio frequency (R.F.) oscillators. The RC oscillators are used at low frequency range while the LC oscillators are used at high frequency range.

4.4.4 Based on : Whether Feedback is Used or Not ?

The oscillators in which the feedback is used, which satisfies the required conditions, are classified as feedback type of oscillators. The oscillators in which the feedback is not used to generate the oscillations, are classified as nonfeedback oscillators. The nonfeedback oscillators use the negative resistance region of the characteristics of the device used. The example of the nonfeedback type of oscillator is the UJT relaxation oscillator.

4.5 R-C Phase Shift Oscillator

RC phase shift oscillator basically consists of an amplifier and a feedback network consisting of resistors and capacitors arranged in ladder fashion. Hence such an oscillator is also called ladder type RC phase shift oscillator.

To understand the operation of this oscillator let us study RC circuit first, which is used in the feedback network of this oscillator. The Fig. 4.7 shows the basic RC circuit.

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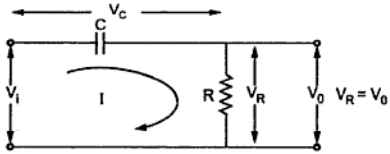

(a) Circuit **Fig. 4.7** **(b) Phasor diagram**

The capacitor C and resistance R are in series. Now X_C is the capacitive reactance in ohms given by,

$$X_C = \frac{1}{2\pi f C} \quad \Omega$$

The total impedance of the circuit is,

$$Z = R - j X_C = R - j\left(\frac{1}{2\pi f C}\right) \Omega = |Z| \angle -\phi^\circ \Omega$$

The r.m.s. value of the input voltage applied is say V_i volts. Hence the current is given by,

$$I = \frac{V_i \angle 0^\circ}{Z} = \frac{V_i \angle 0^\circ}{|Z| \angle -\phi}$$

$\therefore$

$$I = \frac{V_i}{Z} \angle +\phi \quad A$$

where

$$|Z| = \sqrt{R^2 + (X_C)^2}$$

and

$$\phi = \tan^{-1}\left(\frac{X_C}{R}\right)$$

From expression of current it can be seen that **current I leads input voltage V_i by angle ϕ.**

The output voltage V_o is the drop across resistance R given by,

$$V_o = V_R = IR$$

The voltage across the capacitor is,

$$V_C = I X_C$$

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The drop V_R is in phase with current I while the drop V_C lags current I by 90° i.e. I leads V_C by 90°. The phasor diagram is shown in the Fig. 4.7 (b).

> By using proper values of R and C, **the angle ϕ is adjusted in practice equal to 60°**, as required for RC phase shift oscillator.

4.5.1 RC Feedback Network

As stated earlier, RC network is used in feedback path. In oscillator, feedback network must introduce a phase shift of 180° to obtain total phase shift around a loop as 360°. Thus if one RC network produces phase shift of $\phi = 60°$ then to produce phase shift of 180° such three RC networks must be connected in cascade. Hence in RC phase shift oscillator, the feedback network consists of three RC sections each producing a phase shift of 60°, thus total phase shift due to feedback is 180° (3×60°). Such a feedback network is shown in the Fig. 4.8.

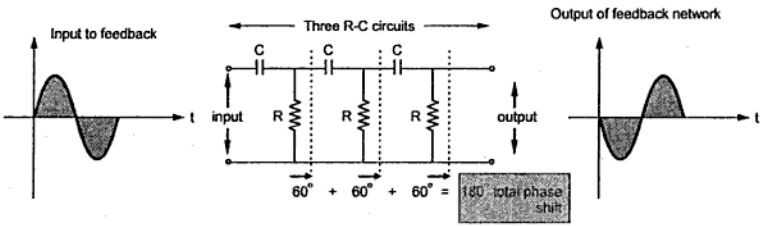

Fig. 4.8 Feedback network in RC phase shift oscillator

The network is also called the **ladder network**. All the resistance values and all the capacitance values are same, so that for a particular frequency, each section of R and C produces a phase shift of 60°.

4.5.2 Phase Shift Oscillator using Transistor

In a practical RC phase shift oscillator, a common emitter (CE) single stage amplifier is used as a basic amplifier. This produces 180° phase shift. The feedback network consists of 3 RC sections each producing 60° phase shift. Such a RC phase shift oscillator using BJT amplifier is shown in the Fig. 4.9.

The output of amplifier is given to feedback network. The output of feedback network drives the amplifier. The total phase shift around a loop is 180° of amplifier and 180° due to 3 RC section, thus 360°. This satisfies the required condition for positive feedback and circuit works as an oscillator.

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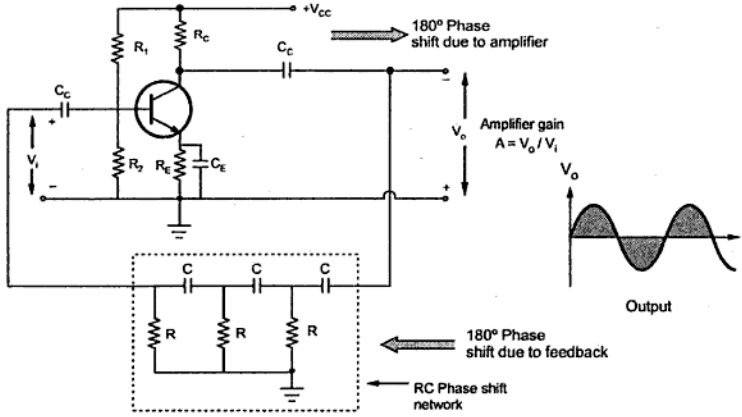

Fig. 4.9 Transistorised RC phase shift oscillator

The frequency of sustained oscillations generated depends on the values of R and C and is given by,

$$f = \frac{1}{2\pi\sqrt{6}\,R\,C}$$

The frequency is measured in Hz.

Actually to satisfy the Barkhausen condition, the expression for the frequency of oscillations is given by,

$$f = \frac{1}{2\pi\,R\,C} \cdot \frac{1}{\sqrt{6+4K}}$$

where $K = \frac{R_C}{R}$

As practically R_C/R is small, K is neglected,

The condition of h_{fe} for the transistor to obtain the oscillations is given by,

$$h_{fe} > 4K + 23 + \frac{29}{K}$$

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And value of K for minimum h_{fe} is 2.7 hence minimum h_{fe} = 44.5. So transistor with h_{fe} less than 44.5 cannot be used in phase shift oscillator.

But for most of practical circuits, the expression for the frequency is considered as,

$$f = \frac{1}{2\pi\sqrt{6}\,RC}$$

4.5.3 Derivation for the Frequency of Oscillations

Replacing the transistor by its approximate h-parameter model, we get the equivalent oscillator circuit as shown in the Fig. 4.10.

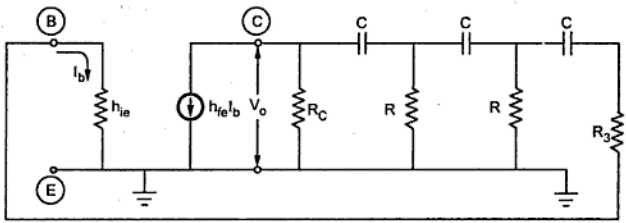

Fig. 4.10 Equivalent circuit using h-parameter model

Practically R_3 is used such that h_{ie} of transistor alongwith R_3 completers the need of R.

$$\therefore \quad R = h_{ie} + R_3$$

Note : If the resistances R_1 and R_2 are not neglected then the input impedance of the amplifier stage becomes as,

$$R_i' = R_1 \,||\, R_2 \,||\, h_{ie} \qquad \ldots (1)$$

In such a case, the value of R_3 must be so selected that

$$R_i' + R_3 = R \qquad \ldots (2)$$

Similarly we can replace, the current source $h_{fe}\,I_b$ by its equivalent voltage source. And assume the ratio of the resistance R_C to R be K.

$$\therefore \quad K = \frac{R_C}{R}$$

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The modified equivalent circuit is shown in the Fig. 4.11.

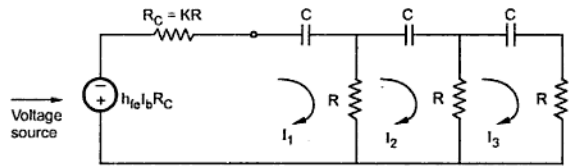

Fig. 4.11 Modified equivalent circuit

Applying KVL for the various loops in the modified equivalent circuit we get,

For Loop 1,

$$-I_1 R_C - \frac{1}{j\omega C} I_1 - I_1 R + I_2 R - h_{fe} I_b R_C = 0$$

Replacing R_C by KR and $j\omega$ by s we get,

$$\therefore \quad + I_1 \left[(K+1) R + \frac{1}{sC}\right] - I_2 R = - hfe\, I_b\, KR \qquad \ldots (3)$$

For Loop 2,

$$-\frac{1}{j\omega C} I_2 - I_2 R - I_2 R + I_1 R + I_3 R = 0$$

$$\therefore \quad - I_1 R + I_2 \left[2R + \frac{1}{sC}\right] - I_3 R = 0 \qquad \ldots (4)$$

For Loop 3,

$$-I_3 \frac{1}{j\omega C} - I_3 R - I_3 R + I_2 R = 0$$

$$\therefore \quad - I_2 R + I_3 \left[2R + \frac{1}{sC}\right] = 0 \qquad \ldots (5)$$

Using Cramer's Rule to solve for I_3,

$$D = \begin{vmatrix} (K+1) R + \frac{1}{sC} & -R & 0 \\ -R & 2R + \frac{1}{sC} & -R \\ 0 & -R & 2R + \frac{1}{sC} \end{vmatrix}$$

$$= \left[(K+1) R + \frac{1}{sC}\right]\left[2R + \frac{1}{sC}\right]^2 - R^2 \left[2R + \frac{1}{sC}\right] - R^2 \left[(K+1) R + \frac{1}{sC}\right]$$

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$$= \frac{[sRC(K+1)+1][2sCR+1]^2}{s^3 C^3} - \frac{R^2(2sCR+1)}{sC} - \frac{R^2[(K+1)sRC+1]}{sC}$$

First term can be written as,

$$[sKRC + sRC + 1][4s^2 C^2 R^2 + 4sRC + 1]/s^3 C^3$$

$$= \frac{4s^3 K R^3 C^3 + 4s^3 R^3 C^3 + 4s^2 C^2 R^2 + 4s^2 K R^2 C^2 + 4s^2 R^2 C^2 + 4sRC + sKRC + sRC + 1}{s^3 C^3}$$

Second and the Third term can be combined to get,

$$= \frac{-R^2[KsRC + sRC + 1] - R^2[1 + 2sRC]}{sC}$$

$$= \frac{-[2R^2 + 3sR^3 C + KsR^3 C]}{sC}$$

Combining the two terms and taking LCM as s^3C^3 we get,

$$D = \frac{s^3 C^3 R^3 [4K+4] + s^2 C^2 R^2 [4K+8] + sRC[5+K] + 1 - [2R^2 + 3sR^3 C + KsR^3 C] s^2 C^2}{s^3 C^3}$$

$$= \frac{s^3 C^3 R^3 [3K+1] + s^2 C^2 R^2 [4K+6] + sRC[5+K] + 1}{s^3 C^3} \quad \ldots (6)$$

Now

$$D_3 = \begin{vmatrix} (K+1)R + \frac{1}{sC} & -R & -h_{fe} I_b KR \\ -R & 2R + \frac{1}{sC} & 0 \\ 0 & -R & 0 \end{vmatrix}$$

$$= -R^2 (h_{fe} I_b KR)$$

$$= -K R^3 h_{fe} I_b \quad \ldots (7)$$

$$\therefore \quad I_3 = \frac{D_3}{D}$$

$$= \frac{-KR^3 h_{fe} I_b s^3 C^3}{s^3 C^3 R^3 [3K+1] + s^2 C^2 R^2 [4K+6] + sRC[5K+1] + 1} \quad \ldots (8)$$

Now I_3 = Output current of the feedback circuit

I_b = Input current of the amplifier

$I_c = h_{fe} I_b$ = Input current of the feedback circuit

$$\therefore \quad \beta = \frac{\text{Output of feedback circuit}}{\text{Input to feedback circuit}} = \frac{I_3}{h_{fe} I_b}$$

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And $$A = \frac{\text{Output of amplifier circuit}}{\text{Input to amplifier circuit}} = \frac{I_3}{I_b} = h_{fe}$$

$$\therefore \quad A\beta = \frac{I_3}{h_{fe}\, I_b} \times h_{fe} = \frac{I_3}{I_b} \qquad \ldots (9)$$

Using equation (9) we get,

$$A\beta = \frac{-KR^3\, h_{fe}\, s^3\, C^3}{s^3\, C^3\, R^3\, [3K+1] + s^2\, C^2\, R^2\, [4K+6] + sRC\,[5K+1] + 1} \qquad \ldots (10)$$

Substituting $s = j\omega$, $s^2 = j^2\omega^2 = -\omega^2$, $s^3 = j^3\omega^3 = -j\omega^3$ in the equation (10) we get,

$$A\beta = \frac{-j\omega^3\, KR^3\, C^3\, h_{fe}}{-j\omega^3\, C^3\, R^3\, [3K+1] - \omega^2\, C^2\, R^2\, [4K+6] + j\omega RC\,[5+K] + 1}$$

Separating the real and imaginary parts in the denominator we get,

$$A\beta = \frac{-j\omega^3\, KR^3\, C^3\, h_{fe}}{[1 - 4K\omega^2\, C^2\, R^2 - 6\omega^2\, C^2\, R^2] - j\omega[3K\omega^2\, R^3\, C^3 + \omega^2\, R^3\, C^3 - 5RC - KRC]}$$

Dividing numerator and denominator by $j\omega^3\, R^3\, C^3$,

$$A\beta = \frac{Kh_{fe}}{\left\{\frac{(1 - 4K\omega^2\, C^2\, R^2 - 6\omega^2\, C^2\, R^2)}{-j\omega^3\, R^3\, C^3}\right\} - \left\{\frac{j\omega[3K\omega^2\, R^3\, C^3 + \omega^2\, R^3\, C^3 - 5RC - KRC]}{-j\omega^3\, R^3\, C^3}\right\}}$$

Replacing $-1/j = j$,

$$= \frac{Kh_{fe}}{j\left\{\frac{1}{\omega^3\, R^3\, C^3} - \frac{4K}{\omega RC} - \frac{6}{\omega RC}\right\} + \left\{3K+1 - \frac{5}{\omega^2\, R^2\, C^2} - \frac{K}{\omega^2\, R^2\, C^2}\right\}}$$

Replacing $\frac{1}{\omega RC} = \alpha$ for simiplicity

$$\therefore \quad A\beta = \frac{Kh_{fe}}{[3K+1-5\alpha^2 - K\alpha^2] + j[\alpha^3 - 4K\alpha - 6\alpha]} \qquad \ldots (11)$$

As per the Barkhausen Criterion, $\angle A\beta = 0°$. Now the angle of numerator term Kh_{fe} of the equation (11) is 0° hence to have angle of the $A\beta$ term as 0°, the imaginary part of the denominator term must be 0.

$$\therefore \quad \alpha^3 - 4K\alpha - 6\alpha = 0$$

$$\alpha(\alpha^2 - 4K - 6) = 0$$

$$\therefore \quad \alpha^2 = 4K + 6 \text{ neglecting zero value}$$

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$$\therefore \quad \alpha = \sqrt{4K+6}$$

$$\therefore \quad \frac{1}{\omega RC} = \sqrt{4K+6}$$

$$\boxed{\omega = \frac{1}{RC\sqrt{4K+6}}}$$

$$\therefore \quad \boxed{f = \frac{1}{2\pi RC\sqrt{4K+6}}} \qquad \ldots(12)$$

This is the frequency at which $\angle A\beta = 0°$. At the same frequency, $|A\beta| = 1$.

Substituting $\alpha = \sqrt{4K+6}$ in the equation (11) we get,

$$A\beta = \frac{Kh_{fe}}{3K+1-(4K+6)[5+K]}$$

$$= \frac{Kh_{fe}}{3K+1-20K-30-4K^2-6K}$$

$$= \frac{Kh_{fe}}{-4K^2-23K-29}$$

Now $|A\beta| = 1$

$$\therefore \quad \left|\frac{Kh_{fe}}{-4K^2-23K-29}\right| = 1$$

$$\therefore \quad Kh_{fe} = 4K^2+23K+29$$

$$\boxed{h_{fe} = 4K + 23 + \frac{29}{K}} \qquad \ldots(13)$$

This must be the value of h_{fe} for the oscillations.

5.4 Minimum Value of h_{fe} for the Oscillations

To get minimum value of h_{fe},

$$\frac{d\,h_{fe}}{dK} = 0$$

$$\therefore \quad \frac{d}{dk}\left[4K+23+\frac{29}{K}\right] = 0$$

$$\therefore \quad \left[4-\frac{29}{K^2}\right] = 0$$

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$$\therefore \quad K^2 = \frac{29}{4}$$

$$\therefore \quad K = 2.6925 \text{ for minimum } h_{fe} \qquad \ldots (14)$$

Substituting in the equation (13),

$$(h_{fe})_{min} = 4\,(2.6925) + 23 + \frac{29}{(2.6925)}$$

$$\therefore \quad \boxed{(h_{fe})_{min} = 44.54} \qquad \ldots(15)$$

Key Point: *Thus for the circuit to oscillate, we must select the transistor whose (h_{fe}) min should be greater than 44.54.*

By changing the values of R and C, the frequency of the oscillator can be changed. But the values of R and C of all three sections must be changed simultaneously to satisfy the oscillating conditions. But this is practically impossible. Hence the phase shift oscillator is considered as a fixed frequency oscillator, for all practical purposes.

Example 4.1: *Find the capacitor C and h_{fe} for the transistor to provide a resonating frequncy of 10 kHz of a transistorised phase shift oscillator. Assume R_1 = 25 kΩ, R_2 = 57 kΩ, R_C = 20 kΩ, R = 7.1 kΩ and h_{ie} = 1.8 kΩ.*

Solution : Referring to equation (1),

$$R_i' = R_1 \parallel R_2 \parallel h_{ie} = 25\ k\Omega \parallel 57\ k\Omega \parallel 1.8\ k\Omega$$

$$\frac{1}{R_i'} = \frac{1}{25} + \frac{1}{57} + \frac{1}{1.8}$$

$$\therefore \quad R_i' = 1.631\ k\Omega$$

Now $R_i' + R_3 = R$

$$\therefore \quad R_3 = R - R_i' = 7.1 - 1.631$$

$$= 5.47\ K\Omega$$

$$K = \frac{R_C}{R} = \frac{20}{7.1} = 2.816$$

Now $$f = \frac{1}{2\pi RC\sqrt{6+4K}}$$

$$\therefore \quad 10\times10^3 = \frac{1}{2\pi\times7.1\times10^3\times C\times\sqrt{6+4\times2.816}}$$

$$\therefore \quad C = 539.45\ pF$$

$$h_{fe} \geq 4K + 23 + \frac{29}{K} \qquad \text{refer equation (13)}$$

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$$\therefore \quad h_{fe} \geq 4\times2.816+23+\frac{29}{2.816}$$

$$\therefore \quad h_{fe} \geq \mathbf{44.562}$$

4.5.5 Advantages

The advantages of R - C phase shift oscillator are,

1. The circuit is simple to design.
2. Can produce output over audio frequency range.
3. Produces sinusoidal output waveform.
4. It is a fixed frequency oscillator.

4.5.6 Disadvantages

By changing the values of R and C, the frequency of the oscillator can be changed. But the values of R and C of all three sections must be changed simultaneously to satisfy the oscillating conditions. But this is practically impossible. Hence the phase shift oscillator is considered as a fixed frequency oscillator, for all practical purposes.

And the frequency stability is poor due to the changes in the values of various components, due to effect of temperature, aging etc.

Example 4.2 : *In a RC phase shift oscillator, the phase shift network uses the resistances each of 4.7 kΩ and the capacitors each of 0.47 μF. Find the frequency of oscillations.*

Solution : The given values are, R = 4.7 kΩ and C = 0.47 μF

$$\therefore \quad f = \frac{1}{2\pi\sqrt{6}RC} = \frac{1}{2\pi\sqrt{6}\times4.7\times10^{3}\times0.47\times10^{-6}} = \mathbf{29.413\ Hz}$$

Example 4.3 : *Estimate the values of R and C for an output frequency of 1 kHz in a RC phase shift oscillator.*

Solution : f = 1 kHz

Now $f = \frac{1}{2\pi\sqrt{6}RC}$

Choose $C = \mathbf{0.1\ \mu F}$

$$\therefore \quad 1\times10^{3} = \frac{1}{2\pi\sqrt{6}R\times0.1\times10^{-6}}$$

$$\therefore \quad R = \mathbf{649.747\ \Omega}$$

Choose $R = \mathbf{680\ \Omega}$ standard value

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4.5.7 FET Phase Shift Oscillator

The practical circuit of FET phase shift oscillator is shown in the Fig. 4.12.

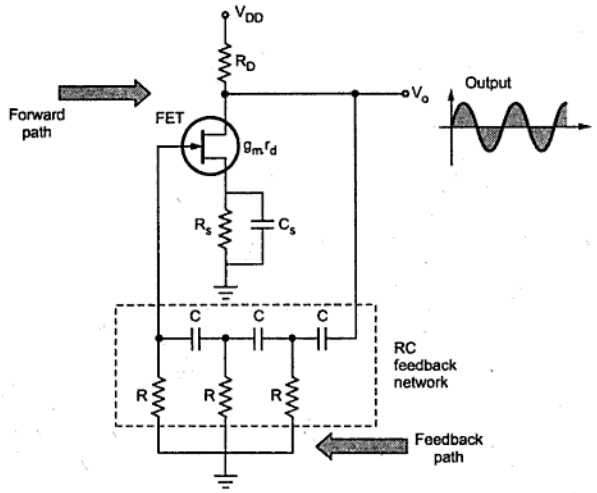

Fig. 4.12 FET phase shift oscillator

For the amplifier stage FET is used. It is self biased with a capacitor bypassed source resistance R_S and a drain bias resistance R_D. The important parameters of FET are g_m and r_d. From FET amplifier theory we can write,

$$|A| = g_m R_L \quad \text{... (27)}$$

Where R_L is the parallel equivalent of R_D and r_d.

$$R_L = \frac{R_D r_d}{R_D + r_d} \quad \text{... (28)}$$

Key Point : *The input impedance of the FET amplifier stage can be conveniently assumed as infinite, as long as the operating frequency is low enough to neglect the capacitive impedances.*

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The feedback network is again three stage R_C network having gain,

$$\boxed{|\beta| = \frac{1}{29}}$$

$$\therefore \quad |A| \geq 29 \qquad \ldots (29)$$

Hence the condition on gain of the amplifier is same as in case of op-amp, the frequency of the oscillator is given by,

$$\boxed{f = \frac{1}{2\pi RC\sqrt{6}}} \qquad \ldots (30)$$

Example 4.4 : *A phase shift oscillator is to be designed with FET having g_m= 5000 μS, r_d = 4 kΩ while the resistance in the feedback circuit is 9.7 kΩ. Select the proper value of C and R_D to have the frequency of oscillations as 5 kHz.*

Solution : Using the expression for the frequency

$$f = \frac{1}{2\pi RC\sqrt{6}}$$

$$\therefore \quad 5\times10^3 = \frac{1}{2\pi\times9.7\times10^3\times C\times\sqrt{6}}$$

$$\therefore \quad C = \mathbf{1.34\ nF}$$

Now using the equation (27),

$$|A| = g_m R_L$$

$$\therefore \quad |A| \geq 29$$

$$\therefore \quad g_m R_L \geq 29$$

$$\therefore \quad R_L \geq \frac{29}{g_m} \geq \frac{29}{5000\times10^{-6}} \geq 5.8\ k\Omega$$

With value of R_L = 6.8 kΩ,

$$R_L = \frac{R_D r_d}{R_D + r_d}$$

$$\therefore \quad 6.8\times10^3 = \frac{R_D\times40\times10^3}{R_D + 40\times10^3}$$

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$$\therefore \quad R_D + 40 \times 10^3 = 5.8823\, R_D$$

$$\therefore \quad 4.8823\, R_D = 40 \times 10^3$$

$$\therefore \quad R_D = \mathbf{8.12\ k\Omega}$$

While for minimum value of $R_L = 5.8\ k\Omega$

$$R_D = \mathbf{6.78\ k\Omega}$$

4.6 Wien Bridge Oscillator

Generally in an oscillator, amplifier stage introduces 180° phase shift and feedback network introduces additional 180° phase shift, to obtain a phase shift of 360° (2π radians) around a loop. This is required condition for any oscillator. But **Wien bridge oscillator uses a noninverting amplifier and hence does not provide any phase shift during amplifier stage.** As total phase shift required is 0° or 2nπ radians, in Wien bridge type no phase shift is necessary through feedback.

Key Point : *Thus the total phase shift around a loop is 0°.*

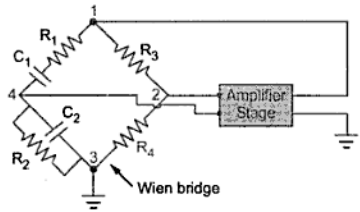

Fig. 4.13 Basic circuit of Wien bridge oscillator

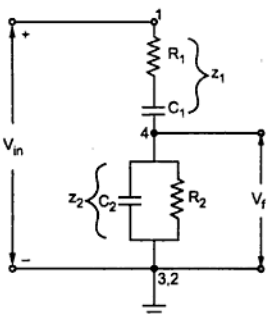

Fig. 4.14 Feedback network of Wien bridge oscillator

Let us study the basic version of the Wien bridge oscillator and its analysis.

A basic Wien bridge used in this oscillator and an amplifier stage is shown in the Fig. 4.13.

The output of the amplifier is applied between the terminals 1 and 3, which is the input to the feedback network. While the amplifier input is supplied from the diagonal terminals 2 and 4, which is the output from the feedback network. Thus amplifier supplied its own input through the Wien bridge as a feedback network.

The two arms of the bridge, namely R_1, C_1 in series and R_2, C_2 in parallel are called **frequency sensitive arms.** This is because the components of these two arms decide the frequency of the

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oscillator. Let us find out the gain of the feedback network. As seen earlier input V_{in} to the feedback network is between 1 and 3 while output V_f of the feedback network is between 2 and 4. This is shown in the Fig. 4.14. Such a feedback network is called **lead-lag network**. This is because at very low frequencies it acts like a lead while at very high frequencies it acts like lag network.

Now from the Fig. 4.14, as shown,

$$Z_1 = R_1 + \frac{1}{j\omega C_1} = \frac{1 + j\omega R_1 C_1}{j\omega C_1}$$

$$Z_2 = R_2 \parallel \frac{1}{j\omega C_2} = \frac{R_2 \times \frac{1}{j\omega C_2}}{R_2 + \frac{1}{j\omega C_2}}$$

$$\therefore \quad Z_2 = \frac{R_2}{1 + j\omega R_2 C_2} \quad \ldots (1)$$

Replacing $j\omega = s$,

$$Z_1 = \frac{1 + s R_1 C_1}{s C_1}$$

and

$$Z_2 = \frac{R_2}{1 + s R_2 C_2}$$

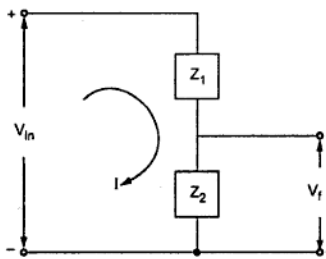

Fig. 4.15 Simplified circuit

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$$I = \frac{V_{in}}{Z_1 + Z_2}$$

and $$V_f = I Z_2$$

$\therefore$ $$V_f = \frac{V_{in} Z_2}{Z_1 + Z_2}$$

$\therefore$ $$\boxed{\beta = \frac{V_f}{V_{in}} = \frac{Z_2}{Z_1 + Z_2}} \quad \text{...(2)}$$

Substituting the values of Z_1 and Z_2,

$$\beta = \frac{\left[\frac{R_2}{1+sR_2C_2}\right]}{\left[\frac{1+sR_1C_1}{sC_1}\right] + \left[\frac{R_2}{1+sR_2C_2}\right]}$$

$$\beta = \frac{sC_1R_2}{(1+sR_1C_1)(1+sR_2C_2)+sC_1R_2}$$

$$= \frac{sC_1R_2}{1+s(R_1C_1+R_2C_2)+s^2R_1R_2C_1C_2+sC_1R_2}$$

$$= \frac{sC_1R_1}{1+s(R_1C_1+R_2C_2+C_1R_2)+s^2R_1R_2C_1C_2}$$

Replacing s by $j\omega$, $s^2 = -\omega^2$

$\therefore$ $$\beta = \frac{j\omega C_1R_2}{(1-\omega^2R_1R_2C_1C_2)+j\omega(R_1C_1+R_2C_2+C_1R_2)} \quad \text{... (3)}$$

Rationalising the expression,

$$\beta = \frac{j\omega C_1R_2\left[(1-\omega^2R_1R_2C_1C_2)-j\omega(R_1C_1+R_2C_2+C_1R_2)\right]}{\left(1-\omega^2R_1R_2C_1C_2\right)^2+\omega^2\left(R_1C_1+R_2C_2+C_1R_2\right)^2}$$

$$\boxed{\beta = \frac{\omega^2C_1R_2(R_1C_1+R_2C_2+C_1R_2)+j\omega C_1R_2(1-\omega^2R_1R_2C_1C_2)}{\left(1-\omega^2R_1R_2C_1C_2\right)^2+\omega^2\left(R_1C_1+R_2C_2+C_1R_2\right)^2}}$$

... (4)

To have zero phase shift of the feedback network, its imaginary part must be zero.

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$$\therefore \quad \omega (1 - \omega^2 R_1 R_2 C_1 C_2) = 0$$

$$\therefore \quad \omega^2 = \frac{1}{R_1 R_2 C_1 C_2} \text{ neglecting zero value.}$$

$$\boxed{\omega = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}}$$

$$\therefore \quad \boxed{f = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}} \quad \ldots(5)$$

Key Point : *This is the frequency of the oscillator and it shows that the components of the frequency sensitive arms are the deciding factors, for the frequency.*

In practice, $R_1 = R_2 = R$ and $C_1 = C_2 = C$ are selected.

$$\therefore \quad f = \frac{1}{2\pi\sqrt{R^2 C^2}}$$

$$\boxed{f = \frac{1}{2\pi RC}} \quad \ldots(6)$$

At $R_1 = R_2 = R$ and $C_1 = C_2 = C$, the gain of the feedback network becomes,

$$\beta = \frac{\omega^2 RC(3RC) + j\omega RC\left(1-\omega^2 R^2 C^2\right)}{\left(1-\omega^2 R^2 C^2\right) + \omega^2 (3RC)^2}$$

Substituting $f = \frac{1}{2\pi RC}$ i.e. $\omega = \frac{1}{RC}$,

we get the magnitude of the feedback network at the resonating frequency of the oscillator as,

$$\beta = \frac{3}{0 + \frac{1}{R^2 C^2} \times (3RC)^2} = \frac{3}{9}$$

$$\therefore \quad \boxed{\beta = \frac{1}{3}} \quad \ldots(7)$$

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The positive sign of β indicates that the phase shift by the feedback network is 0°. Now to satisfy the Barkhausen criterion for the sustained oscillations, we can write,

$$|A\beta| \geq 1$$

$$\therefore \quad |A| \geq \frac{1}{|\beta|} \geq \frac{1}{\left(\frac{1}{3}\right)}$$

$$\therefore \quad \boxed{|A| \geq 3}$$

This is the required gain of the amplifier stage, without any phase shift.

If $R_1 \neq R_2$ and $C_1 \neq C_2$ then

$$\boxed{f = \frac{1}{2\pi\sqrt{R_1R_2C_1C_2}}}$$

Substituting in the equation (4) we get,

$$\boxed{\beta = \frac{C_1R_2}{(R_1C_1 + R_2C_2 + C_1R_2)}}$$

$$|A\beta| \geq 1$$

$$\therefore \quad \boxed{A \geq \frac{R_1C_1 + R_2C_2 + C_1R_2}{C_1R_2}} \quad \ldots (8)$$

Another important advantage of the Wien bridge oscillator is that by varying the two capacitor values simultaneously, by mounting them on the common shaft, different frequency ranges can be provided.

Let us see the various versions of the Wien bridge oscillator by considering various circuits for the amplifier stage.

4.6.1 Transistorised Wien Bridge Oscillator

In this circuit, two stage common emitter transistor amplifier is used. Each stage contributes 180° phase shift hence the total phase shift due to the amplifier stage becomes 360° i.e. 0° which is necessary as per the oscillator conditions.

The practical, transistorised Wien bridge oscillator circuit is shown in the Fig. 4.16.

The bridge consists of R and C in series, R and C in parallel, R_3 and R_4. The feedback is applied from the collector of Q_2 through the coupling capacitor, to the bridge circuit.

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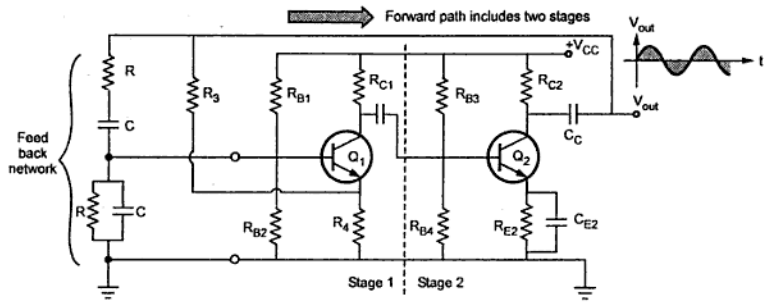

Fig. 4.16 Transistorised Wien bridge oscillator

The resistance R_4 serves the dual purpose of emitter resistance of the transistor Q_1 and also the element of the Wien bridge.

The two stage amplifier provides a gain much more than 3 and it is necessary to reduce it. To reduce the gain, the negative feedback is used without bypassing the resistance R_4. The negative feedback can accomplish the gain stability and can control the output magnitude. The negative feedback also reduces the distortion and therefore output obtained is a pure sinusoidal in nature. The amplitude stability can be improved using a nonlinear resistor for R_4. Due to this, the loop gain depends on the amplitude of the oscillations. Increase in the amplitude of the oscillations, increases the current through nonlinear resistance, which results into an increase in the value of nonlinear resistance R_4. When this value increases, a greater amount of negative feedback is applied. This reduces the loop gain. And hence signal amplitude gets reduced and controlled.

4.6.2 Wien Bridge Oscillator using FET

As a single stage FET amplifier gives a phase shift of 180° and it is required to have 360° phase shift from amplifier stage, the two stages of FET amplifier is the feature of the Wien bridge oscillator using FET.

The basic feedback network of Wien bridge remains same. Hence the condition of the oscillations, remains same.

The practical circuit of Wien bridge oscillator using two stage FET amplifier is shown in the Fig. 4.17.

The RC series and parallel combination forms the frequency sensitive arms of the Wien bridge. The resistances R_3 and R_4 form the part of the feedback path. The unbypassed source resistance R_4 provides the negative feedback required for gain stabilization. The

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amplifier gain is the product of the gains of the two stages. The operation of the circuit is similar to the Wien bridge oscillator circuit with op-amp.

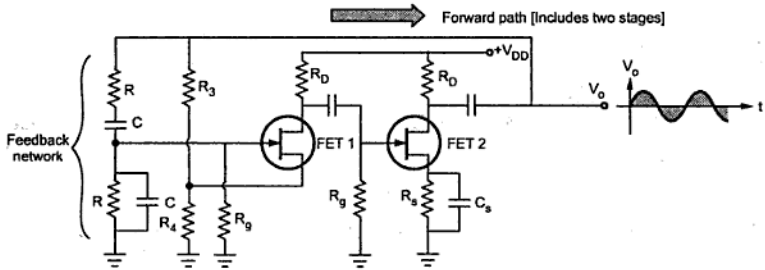

Fig. 4.17 FET Wien bridge oscillator

Key Point : *All the conditions derived earlier for the oscillating conditions are equally applicable to this circuit.*

Example 4.5 : *The frequency sensitive arms of the Wien bridge oscillator uses* $C_1 = C_2 = 0.001\,\mu F$ *and* $R_1 = 10\,k\Omega$ *while* R_2 *is kept variable. The frequency is to be varied from 10 kHz to 50 kHz, by varying* R_2*. Find the minimum and maximum values of* R_2*.*

Solution : The frequency of the oscillator is given by,

$$f = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$$

For $f = 10$ kHz,

$$10\times10^3 = \frac{1}{2\pi\sqrt{\left(10\times10^3\times R_2\times(0.001\times10^{-6}\right)^2}}$$

$$\therefore \quad R_2 = 25.33\ k\Omega$$

For $f = 50$ kHz

$$50\times10^3 = \frac{1}{2\pi\sqrt{\left(10\times10^3\times R_2\times(0.001\times10^{-6}\right)^2}}$$

$$\therefore \quad R_2 = 1.013\ k\Omega$$

So minimum value of R_2 is 1.013 kΩ while the maximum value of R_2 is 25.33 kΩ.

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4.7 Comparison of RC Phase Shift and Wien Bridge Oscillators

The similarities and the differences between the two oscillators are given in the Table 4.2.

Sr. No.	RC Phase Shift Oscillator	Wien Bridge Oscillator
1)	It is a phase shift oscillator used for low frequency range.	It is also a phase shift oscillator used for low frequency range.
2)	The feedback network is RC network with three RC sections.	The feedback network is lead-lag network which is called Wien bridge circuit.
3)	The feedback network introduces 180° phase shift.	The feedback network does not introduce any phase shift.
4)	Op-amp is used in an inverting mode.	Op-amp is used in non-inverting mode.
5)	Op-amp circuit introduces 180° phase shift.	Op-amp circuit does not introduce any phase shift.
6)	The frequency of oscillations is, $f = \frac{1}{2\pi RC\sqrt{6}}$	The frequency of oscillations is, $f = \frac{1}{2\pi RC}$
7)	The amplifier gain condition is, $\|A\| \geq 29$	The amplifier gain condition is, $\|A\| \geq 3$
8)	The frequency variation is difficult.	Mounting the two capacitors on common shaft and varying their values, frequency can be varied.

Table 4.2

4.8 Tuned Oscillator Circuits

The oscillators which use the elements L and C to produce the oscillations are called LC oscillator or tuned oscillators. The circuit using elements L and C is called **tank circuit** or **oscillatory circuit**, which is an important part of LC oscillators. This circuit is also referred as resonating circuit, or tuned circuit. These oscillators are used for high frequency range from 200 kHz upto few GHz. Due to high frequency range, these oscillators are often used for sources of RF (radio frequency) energy. Let us study the basic action of LC tank circuit first.

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4.8.1 Operation of LC Tank Circuit

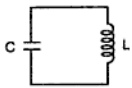

Fig. 4.18 LC tank circuit

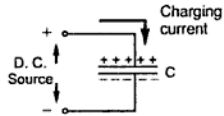

Fig. 4.19 Initial charging

The LC tank circuit consists of elements L and C connected in parallel as shown in the Fig. 4.18.

Let capacitor is initially charged from a d.c. source with the polarities as shown in the Fig. 4.19.

When the capacitor gets charged, the energy gets stored in a capacitor called electrostatic energy. When such a charged capacitor is connected across inductor L in a tank circuit, the capacitor starts discharging through L, as shown in the Fig. 4.20. The arrow indicates direction of flow of conventional current. Due to such current flow, the magnetic field gets set up around the inductor L. Thus inductor starts storing the energy. When capacitor is fully discharged, maximum current flows through the circuit. At this instant all the electrostatic energy get stored as a magnetic energy in the inductor L. This is shown in the Fig. 4.21.

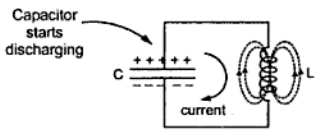

Fig. 4.20

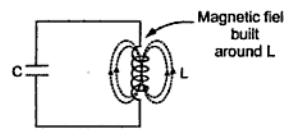

Fig. 4.21

Now the magnetic field around L starts collapsing. As per Lenz's law, this starts charging the capacitor with opposite polarity making lower plate positive and upper plate negative, as shown in the Fig. 4.22.

After some time, capacitor gets fully charged with opposite polarities, as compared to its initial polarities. This is shown in the Fig. 4.23. The entire magnetic energy gets converted back to electrostatic energy in capacitor.

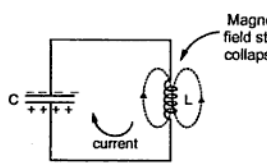

Fig. 4.22

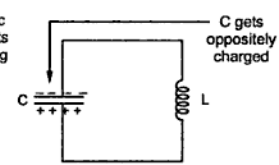

Fig. 4.23

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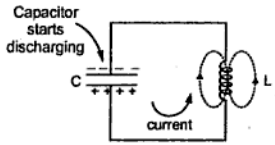

Fig. 4.24

Now capacitor again starts discharging through inductor L. But the direction of current through circuit is now opposite to the direction of current earlier in the circuit. This is shown in the Fig. 4.24. Again electrostatic energy is converted to magnetic energy. When capacitor is fully discharged, the magnetic field starts collapsing, charging the capacitor again in opposite direction.

Key Point: *Thus capacitor charges with alternate polarities and discharges producing alternating current in the tank circuit.*

This is nothing but oscillatory current. But every time when energy is transferred from C to L and L to C, the losses occur due to which amplitude of oscillating current keeps on decreasing everytime when energy transfer takes place. Hence actually we get exponentially decaying oscillations called damped oscillations. These are shown in the Fig. 4.25. Such oscillations stop after sometime.

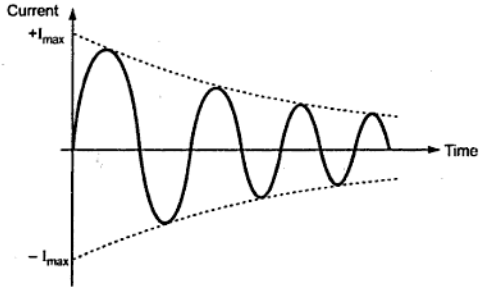

Fig. 4.25 Damped oscillations

Key Point : *In LC oscillator, the transistor amplifier supplies this loss of energy at the proper times.*

The care of proper polarity is taken by the feedback network. Thus LC tank circuit alongwith transistor amplifier can be used to obtain oscillators called LC oscillators. Due to supply of energy which is lost, the oscillations get maintained hence called **sustained oscillations** or **undamped oscillations.**

The frequency of oscillations generated by LC tank circuit depends on the values L and C and is given by,

$$f = \frac{1}{2\pi\sqrt{LC}}$$

where L is in henries and C is in farads.

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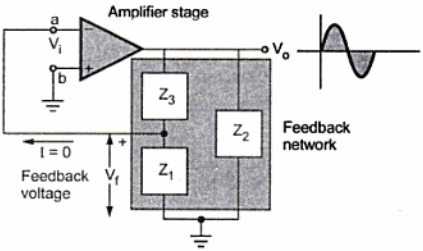
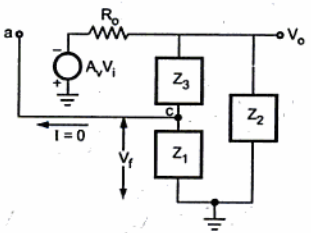
4.8.2 Basic Form of LC Oscillator Circuit

As stated earlier, LC tuned circuit forms the feedback network while an op-amp, FET or bipolar junction transistor can be active device in the amplifier stage. The Fig. 4.26 (a) shows the basic form of LC oscillator circuit with gain of the amplifier as A_v. The amplifier output feeds the network consisting of impedances Z_1, Z_2 and Z_3. Assume an active device with infinite input impedance such as FET or op-amp. Then the basic circuit can be replaced by its linear equivalent circuit as shown in the Fig. 4.26 (b).



(a) Basic form of LC oscillators



(b) Equivalent circuit
Fig. 4.26

Amplifier provides a phase shift of 180°, while the feedback network provides an additional phase shift of 180°, to satisfy the required condition.

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i) Analysis of the amplifier stage

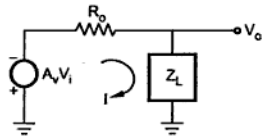

Fig. 4.27

As input impedance of the amplifier is infinite, there is no current flowing towards the input terminals. Let R_o be the output impedance of the amplifier stage.

As I = 0, Z_1, Z_3 appears in series and the combination in parallel with Z_2. The equivalent be Z_L i.e. load impedance. So circuit can be reduced, as shown in the Fig. 4.27.

$$\therefore \quad I = \frac{-A_V V_i}{R_o + Z_L} \qquad \ldots (1)$$

While $$V_o = I Z_L \qquad \ldots (2)$$

$$\therefore \quad V_o = \frac{-A_V V_i Z_L}{R_o + Z_L}$$

$$\therefore \quad \boxed{\frac{V_o}{V_i} = A = \frac{-A_V Z_L}{R_o + Z_L}} \qquad \ldots (3)$$

where A is the gain of the amplifier stage.

ii) Analysis of the feedback stage

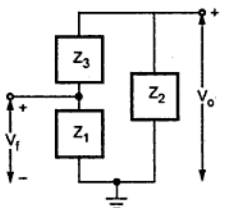

Fig. 4.28

For the feedback factor (β) calculation, consider only the feedback circuit as shown in the Fig. 4.28.

From the voltage division in parallel circuit, we can write,

$$V_f = V_o \left[\frac{Z_1}{Z_1 + Z_3}\right] \qquad \ldots (4)$$

$$\therefore \frac{V_f}{V_o} = \beta = \frac{Z_1}{Z_1 + Z_3} \qquad \ldots (5)$$

But as the phase shift of the feedback network is 180°,

$$\therefore \quad \boxed{\beta = -\frac{Z_1}{Z_1 + Z_3}} \qquad \ldots (6)$$

Obtain an expression for – Aβ as basic Barkhausen condition is – Aβ = 1. Refer Equation (4) of the section 4.3.

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$$\therefore \quad -A\beta = \frac{-A_V Z_1 Z_L}{(R_o + Z_L) \times (Z_1 + Z_3)} \qquad \ldots (7)$$

This is the required loop gain. Now Z_L can be written as $(Z_1 + Z_3) \| Z_2$ i.e.

$$Z_L = \frac{Z_2 (Z_1 + Z_3)}{Z_1 + Z_2 + Z_3} \qquad \ldots (8)$$

$$\therefore \quad -A\beta = \frac{-A_V Z_1 \left[\frac{Z_2 (Z_1 + Z_3)}{Z_1 + Z_2 + Z_3}\right]}{\left[R_o + \frac{Z_2 (Z_1 + Z_3)}{Z_1 + Z_2 + Z_3}\right](Z_1 + Z_3)}$$

Dividing numerator and denominator by $\frac{(Z_1 + Z_3)}{Z_1 + Z_2 + Z_3}$,

$$= \frac{-A_V Z_1 Z_2}{\left[\frac{R_o (Z_1 + Z_2 + Z_3)}{(Z_1 + Z_3)} + Z_2\right](Z_1 + Z_3)}$$

$$= \frac{-A_V Z_1 Z_2}{R_o (Z_1 + Z_2 + Z_3) + Z_2 (Z_1 + Z_3)} \qquad \ldots (9)$$

As Z_1 Z_2 and Z_3 are the pure reactive elements,

$$Z_1 = jX_1, \quad Z_2 = jX_2 \quad \text{and} \quad Z_3 = jX_3$$

where $X = \omega L$ for an inductive reactance

and $X = \frac{-1}{\omega C}$ for a capacitive reactance.

$$-A\beta = \frac{-A_V (jX_1)(jX_2)}{R_o (jX_1 + jX_2 + jX_3) + jX_2 (jX_1 + jX_3)}$$

$$\boxed{-A\beta = \frac{A_V X_1 X_2}{-X_2 (X_1 + X_3) + jR_o (X_1 + X_2 + X_3)}} \qquad \ldots (10)$$

To have 180° phase shift, the imaginary part of the denominator must be zero.

$$\therefore \quad \boxed{X_1 + X_2 + X_3 = 0} \qquad \ldots (11)$$

Substituting in the equation (10),

$$-A\beta = \frac{-A_V X_1 X_2}{X_2 (X_1 + X_3)}$$

But from the equation (11), $X_1 + X_3 = -X_2$

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$$\therefore \quad -A\beta = \frac{-A_V X_1}{-X_2} = +A_V\left(\frac{X_1}{X_2}\right) \qquad ...(12)$$

According to the Barkhausen criterion, $-A\beta$ must be positive and must be greater than or equal to unity. As A_V is positive, the $-A\beta$ will be positive only when X_1 and X_2 will have same sign. This indicates that X_1 and X_2 must be of same type of reactances either both inductive or capacitive.

While from the equation (11), we can say that $X_3 = -(X_1 + X_2)$ must be inductive if X_1, X_2 are capacitive while X_3 must be capacitive if X_1, X_2 are inductive.

Table 4.3 shows the various types of the LC oscillators depending on the design of the reactances X_1, X_2 and X_3.

Oscillator type	Reactance elements in the tank circuit		
	X_1	X_2	X_3
Hartley Oscillator	L	L	C
Colpitts Oscillator	C	C	L

Table 4.3

4.9 Hartley Oscillator

As seen earlier, a LC oscillator which uses two inductive reactances and one capacitive reactance in its feedback network is called Hartley Oscillator.

4.9.1 Transistorised Hartley Oscillator

The amplifier stage uses an active device as a transistor in common emitter configuration. The practical circuit is shown in the Fig. 4.29.

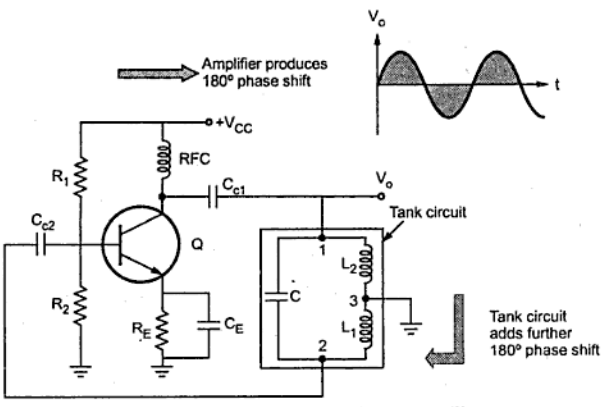

Fig. 4.29 Transistorised Hartley oscillator

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The resistances R_1 and R_2 are the biasing resistances. The RFC is the radio frequency choke. Its reactance value is very high for high frequencies, hence it can be treated as open circuit. While for d.c. conditions, the reactance is zero hence causes no problem for d.c. capacitors.

Hence due to RFC, the isolation between a.c. and d.c. operation is achieved. R_E is also a biasing circuit resistance and C_E is the emitter bypass capacitor. C_{C1} and C_{C2} are the coupling capacitor.

The common emitter amplifier provides a phase shift of 180°. As emitter is grounded, the base and the collector voltages are out of phase by 180°. As the centre of L_1 and L_2 is grounded, when upper end becomes positive, the lower becomes negative and viceversa. So the LC feedback network gives an additional phase shift of 180°, necessary to satisfy oscillation conditions.

4.9.2 Derivation of Frequency of Oscillations

The output current which is the collector current is $h_{fe}I_b$ where I_b is the base current. Assuming coupling condensers are short, the capacitor C is between base and collector. The inductance L_1 is between base and emitter while the inductance L_2 is between collector and emitter. The equivalent circuit of the feedback network is shown in the Fig. 4.30.

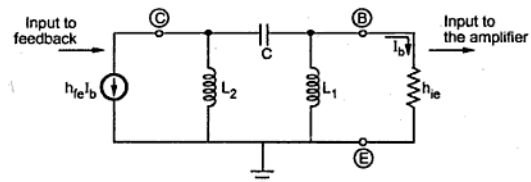

Fig. 4.30 Equivalent circuit

As h_{ie} is the input impedance of the transistor. The output of the feedback is the current I_b which is the input current of the transistor. While input to the feedback network is the output of the transistor which is $I_c = h_{fe}I_b$, converting current source into voltage source we get,

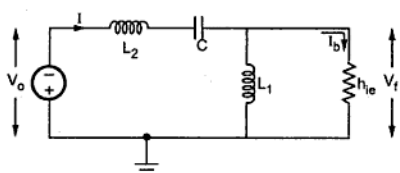

Fig. 4.31 Simplified equivalent circuit

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$$V_o = h_{fe} I_b X_{L_2} = h_{fe} I_b j\omega L_2 \quad \ldots (1)$$

Now L_1 and h_{ie} are in parallel, so the total current I drawn from the supply is,

$$I = \frac{-V_o}{[X_{L_2} + X_C] + [X_{L_1} \| h_{ie}]} \quad \ldots (2)$$

Negative sign, as current direction shown in opposite to the polarities of V_o.

Now $$X_{L_2} + X_C = j\omega L_2 + \frac{1}{j\omega C}$$

and $$X_{L_1} \| h_{ie} = \frac{j\omega L_1 h_{ie}}{(j\omega L_1 + h_{ie})}$$

Substituting in the equation (2) we get,

$$I = \frac{-h_{fe} I_b j\omega L_2}{\left[j\omega L_2 + \frac{1}{j\omega C}\right] + \frac{j\omega L_1 h_{ie}}{(j\omega L_1 + h_{ie})}} \quad \ldots (3)$$

Replacing $j\omega$ by s,

$$I = \frac{-s h_{fe} I_b L_2}{\left[s L_2 + \frac{1}{sC}\right] + \frac{s L_1 h_{ie}}{(s L_1 + h_{ie})}}$$

$$= \frac{-s h_{fe} I_b L_2}{\frac{[1+s^2 L_2 C]}{sC} + \frac{s L_1 h_{ie}}{(s L_1 + h_{ie})}}$$

$$= \frac{-s h_{fe} I_b L_2 (sC)(s L_1 + h_{ie})}{[1+s^2 L_2 C][s L_1 + h_{ie}] + (sC)(s L_1 h_{ie})}$$

$$= \frac{-s^2 h_{fe} I_b L_2 C(s L_1 + h_{ie})}{s^3 L_1 L_2 C + s L_1 + h_{ie} + s^2 L_2 C h_{ie} + s^2 L_1 C h_{ie}}$$

$$= \frac{-s^2 h_{fe} I_b L_2 C(s L_1 + h_{ie})}{s^3 L_1 L_2 C + s^2 C h_{ie}(L_1 + L_2) + s L_1 + h_{ie}}$$

According to current division in parallel circuit,

$$I_b = I \times \frac{X_{L_1}}{XL_1 + h_{ie}}$$

$$= I \times \frac{j\omega L_1}{(j\omega L_1 + h_{ie})}$$

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$$I_b = I \times \left[\frac{sL_1}{(sL_1 + h_{ie})}\right] \quad \ldots (4)$$

Substituting value of I from equation (3) in (4),

$$I_b = \frac{-s^2 h_{fe} I_b L_2 C(sL_1 + h_{ie})}{[s^3(L_1L_2C) + s^2 C h_{ie}(L_1 + L_2) + sL_1 + h_{ie}]} \times \frac{sL_1}{(sL_1 + h_{ie})}$$

$$= \frac{-s^3 h_{fe} I_b C L_1 L_2}{s^3(L_1L_2C) + s^2 C h_{ie}(L_1 + L_2) + sL_1 h_{ie}}$$

$$\therefore \quad 1 = \frac{-s^3 h_{fe} C L_1 L_2}{s^3(L_1L_2C) + s^2 C h_{ie}(L_1 + L_2) + sL_1 + h_{ie}} \quad \ldots (5)$$

Substituting $s = j\omega$, $s^2 = -\omega^2$, $s^3 = -j\omega^3$ we get

$$\therefore \quad 1 = \frac{j\omega^3 h_{fe} C L_1 L_2}{-j\omega^3 L_1 L_2 C - \omega^2 C h_{ie}(L_1 + L_2) + j\omega L_1 + h_{ie}}$$

$$= \frac{j\omega^3 h_{ie} C L_1 L_2}{[h_{ie} - \omega^2 C h_{ie}(L_1 + L_2)] + j\omega L_1(1 - \omega^2 L_2 C)} \quad \ldots (6)$$

Rationalising the R.H.S of the above equation,

$$\therefore \quad 1 = \frac{j\omega^3 h_{fe} C L_1 L_2 [h_{ie} - \omega^2 C h_{ie}(L_1 + L_2) - j\omega L_1(1 - \omega^2 L_2 C)]}{[h_{ie} - \omega^2 C h_{ie}(L_1 + L_2)]^2 + \omega^2 L_1^2 (1 - \omega^2 L_2 C)^2}$$

$$= \frac{\omega^4 h_{fe} L_1^2 L_2 C(1 - \omega^2 L_2 C) + j\omega^3 h_{fe} L_1 L_2 C [h_{ie} - \omega^2 C h_{ie}(L_1 + L_2)}{[h_{ie} - \omega^2 C h_{ie}(L_1 + L_2)]^2 + \omega^2 L_1^2 (1 - \omega^2 L_1^2 L_2 C)^2} \quad \ldots (7)$$

To satisfy this equation, imaginary part of R. H. S. must be zero.

$$\therefore \quad \omega^3 h_{fe} L_1 L_2 C [h_{ie} - \omega^2 h_{ie} C (L_1 + L_2)] = 0$$

$$\therefore \quad \omega^3 h_{fe} h_{ie} L_1 L_2 C [1 - \omega^2 C (L_1 + L_2)] = 0$$

$$\therefore \quad 1 - \omega^2 C (L_1 + L_2) = 0$$

$$\therefore \quad \omega^2 = \frac{1}{C(L_1 + L_2)}$$

$$\therefore \quad \boxed{\omega = \frac{1}{\sqrt{C(L_1 + L_2)}}}$$

$$\therefore \quad \boxed{f = \frac{1}{2\pi\sqrt{C(L_1 + L_2)}}} \quad \ldots (8)$$

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This is the frequency of the oscillations. At this frequency, the restriction of the value of h_{fe} can be obtained, by equating the magnitudes of the both sides of the equation (7).

$$\therefore \quad 1 = \frac{\omega^4 h_{fe} L_1^2 L_2 C(1-\omega^2 L_2 C)}{0+\omega^2 L_1^2 (1-\omega^2 L_2 C)^2} \text{ at } \omega = \frac{1}{\sqrt{C(L_1+L_2)}}$$

$$\therefore \quad 1 = \frac{h_{fe} L_2}{(1-\omega^2 L_2 C)} \text{ at } \omega = \frac{1}{\sqrt{C(L_1+L_2)}}$$

$$\therefore \quad 1 = \frac{h_{fe} L_2}{\left[1-\frac{L_2 C}{C(L_1+L_2)}\right]} = \frac{h_{fe} L_2}{L_1}$$

$$\therefore \quad \boxed{h_{fe} = \frac{L_1}{L_2}} \qquad \ldots (9)$$

This is the value of h_{fe}, required to satisfy the oscillating conditions.

For a mutual inductance of M,

$$\boxed{h_{fe} = \frac{L_1 + M}{L_2 + M}} \qquad \ldots (10)$$

Now $L_1 + L_2$ is the equivalent inductance of the two inductances L_1 and L_2, connected in series denoted as

$$\boxed{L_{eq} = L_1 + L_2} \qquad \ldots (11)$$

Hence the frequency of oscillations is given by,

$$\boxed{f = \frac{1}{2\pi\sqrt{C L_{eq}}}} \qquad \ldots (12)$$

Key Point: *So if the capacitor C is kept variable, frequency can be varied over a large range as per the requirement.*

In practice, L_1 and L_2 may be wound on a single core so that there exists a mutual inductance between them denoted as M.

In such a case, the mutual inductance is considered while determining the equivalent inductance L_{eq}. Hence,

$$\boxed{L_{eq} = L_1 + L_2 + 2M} \qquad \ldots (13)$$

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If L_1 and L_2 are assisting each other then sign of 2M is positive while if L_1 and L_2 are in series opposition then sign of 2M is negative.

The expression for the frequency of the oscillations remain same as given by (12).

A practical circuit where the mutual inductance exists between L_1 and L_2, of transistorised Hartley oscillator is shown in the Fig. 4.30.

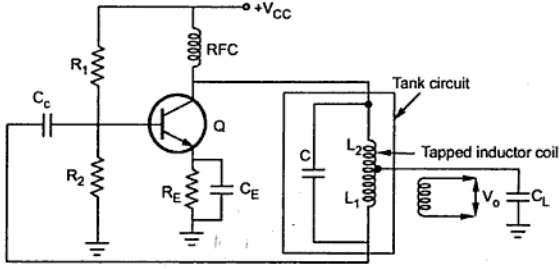

Fig. 4.32 Another form of transistorised Hartley oscillator

Key Point : *The Hartley oscillators are widely used in the radio receivers as local oscillators.*

Example 4.6 : *In a transistorised Hartley oscillator the two inductances are 2 mH and 20 μH while the frequency is to be changed from 950 kHz to 2050 kHz. Calculate the range over which the capacitor is to be varied.*

Solution : The frequency is given by,

$$f = \frac{1}{2\pi\sqrt{C(L_{eq})}}$$

where $L_{eq} = L_1 + L_2 = 2\times10^{-3} + 20\times10^{-6} = 0.00202$

For $f = f_{max} = \mathbf{2050\ kHz}$

$$2050\times10^3 = \frac{1}{2\pi\sqrt{C\times0.00202}}$$

$\therefore$ $C = \mathbf{2.98\ pF}$

For $f = f_{min} = \mathbf{950\ kHz}$

$$950\times10^3 = \frac{1}{2\pi\sqrt{C\times0.00202}}$$

$\therefore$ $C = \mathbf{13.89\ pF}$

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Hence C must be varied from 2.98 pF to 13.89 pF, to get the required frequency variation.

4.9.3 FET Hartley Oscillator

If FET is used as an active device in an amplifier stage, then the circuit is called FET Hartley oscillator. The practical circuit is shown in the Fig. 4.33.

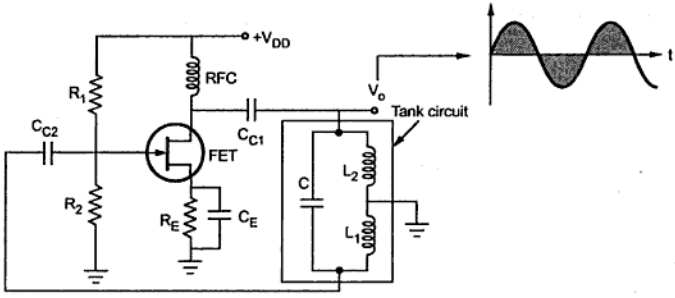

Fig. 4.33 FET Hartley oscillator

The resistances R_1, R_2 bias the FET along with R_s. The C_s in the source bypass capacitor. To maintain Q point stable, coupling capacitors C_{C1}, C_{C2} are used. These have very large values compared to capacitor C. The tank circuit is shown in a box.

We know,

$$X_1 + X_2 + X_3 = 0$$

And $$X_1 = j\omega L_1,\ X_2 = j\omega L_2 \text{ and } X_3 = \frac{1}{j\omega C}$$

Solving for ω, we get the same expression for the frequency as derived earlier.

$$f = \frac{1}{2\pi\sqrt{C L_{eq}}}$$

where $$L_{eq} = L_1 + L_2 \text{ or } L_1 + L_2 + 2M$$

This is dependent on whether L_1, L_2 are wound on the same core or not.

If $L_1 = L_2 = L$, then the frequency of oscillations is given by,

$$f = \frac{1}{2\pi\sqrt{2}\sqrt{LC}} \quad \text{... (14)}$$

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Example 4.7 : *Calculate the frequency of oscillations of a Hartley oscillator having $L_1 = 0.5$ mH, $L_2 = 1$ mH and $C = 0.2$ μF.*

Solution : The given values are,

$$L_1 = 0.5 \text{ mH}, \quad L_2 = 1 \text{ mH}, \quad C = 0.2 \text{ μF}$$

Now $$f = \frac{1}{2\pi\sqrt{L_{eq}C}}$$

and $$L_{eq} = L_1 + L_2 = 0.5 + 1 = 1.5 \text{ mH}$$

$\therefore$ $$f = \frac{1}{2\pi\sqrt{1.5\times10^{-3}\times0.2\times10^{-6}}} = \mathbf{9.19 \text{ kHz}}$$

4.10 Colpitts Oscillator

An LC oscillator which uses two capacitive reactances and one inductive reactance in the feedback network i.e. tank circuit, is called **Colpitts oscillator.**

4.10.1 Transistorised Colpitts Oscillator

The amplifier stage uses an active device as a transistor in common emitter configuration. The practical circuit is shown in the Fig. 4.34.

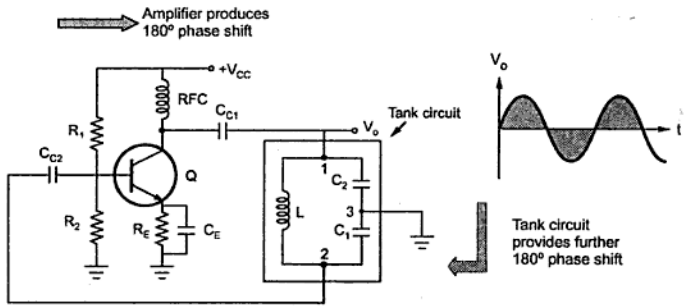

Fig. 4.34 Transistorised Colpitts oscillator

The basic circuit is same as transistorised Hartley oscillator, except the tank circuit. The common emitter amplifier causes a phase shift of 180°, while the tank circuit adds further 180° phase shift, to satisfy the oscillating conditions.

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4.10.2 Derivation of Frequency of Oscillations

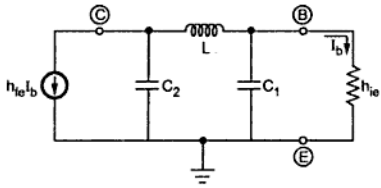

Fig. 4.35 Equivalent circuit

As seen earlier, the output current I_c which is h_{fe} I_b acts as input to the feedback network. While the base current I_b acts as the output current of the tank circuit, flowing through the input impedance of the amplifier h_{ie}. The equivalent circuit of the tank circuit is shown in the Fig. 4.35.

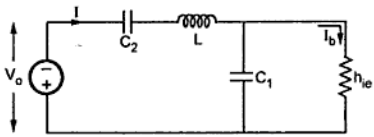

Fig. 4.36 Simplified equivalent circuit

Converting the current source into the voltage source. We get the equivalent circuit as shown in the Fig. 4.36.

$$V_o = h_{fe} I_b X_{C_2} = h_{fe} I_b \frac{1}{j\omega C_2} \quad ...(1)$$

The total current I, drawn from the supply is,

$$I = \frac{-V_o}{[X_{C_2} + X_L] + [X_{C_1} \| h_{ie}]} \quad ... (2)$$

The negative sign is because the current direction is assumed in the opposite direction to that, would be due to the polarities of V_o.

Now $$X_{C2} + X_L = \frac{1}{j\omega C_2} + j\omega L$$

and $$X_{C1} \| h_{ie} = \frac{\frac{1}{j\omega C_1} \times h_{ie}}{\left[\frac{1}{j\omega C_1} + h_{ie}\right]}$$

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Substituting in the equation (4.79),

$$\therefore \quad I = \frac{-h_{fe} I_b \left(\frac{1}{j\omega C_2}\right)}{\left[\frac{1}{j\omega C_2} + j\omega L\right] + \left[\frac{\frac{h_{ie}}{j\omega C_1}}{h_{ie} + \frac{1}{j\omega C_1}}\right]} \quad \ldots (3)$$

Replacing $j\omega$ by s,

$$\therefore \quad I = \frac{-h_{fe} I_b \left(\frac{1}{sC_2}\right)}{\left[\frac{1}{sC_2} + sL\right] + \left[\frac{\frac{h_{ie}}{sC_1}}{h_{ie} + \frac{1}{sC_1}}\right]}$$

$$= \frac{-h_{fe} I_b \left(\frac{1}{sC_2}\right)}{\frac{(1+s^2 LC_2)}{sC_2} + \left[\frac{h_{ie}}{1+sC_1 h_{ie}}\right]}$$

$$= \frac{-h_{fe} I_b \left(\frac{1}{sC_2}\right)(sC_2)(1+sC_1 h_{ie})}{(1+s^2 LC_2)(1+sC_1 h_{ie}) + sC_2 h_{ie}}$$

$$= \frac{-h_{fe} I_b (1+sC_1 h_{ie})}{s^3 LC_1 C_2 h_{ie} + s^2 LC_2 + sC_1 h_{ie} + 1 + sC_2 h_{ie}}$$

$$= \frac{-h_{fe} I_b (1+sC_1 h_{ie})}{s^3 LC_1 C_2 h_{ie} + s^2 LC_2 + sh_{ie}(C_1 + C_2) + 1} \quad \ldots (4)$$

According to the current division in the parallel circuit,

$$I_b = I \times \frac{X_{C_1}}{(X_{C1} + h_{ie})} = \frac{I \times \frac{1}{j\omega C_1}}{\left(h_{ie} + \frac{1}{j\omega C_1}\right)}$$

$$\therefore \quad I_b = \frac{I}{(1+sh_{ie} C_1)} \quad \ldots (5)$$

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Substituting value of I from the equation (4), in (5), we get

$$= \frac{-h_{fe} I_b (1 + s C_1 h_{ie})}{s^3 L C_1 C_2 h_{ie} + s^2 L C_2 + s h_{ie} (C_1 + C_2) + 1} \times \frac{1}{(1 + s C_1 h_{ie})}$$

$$= \frac{-h_{fe} I_b}{s^3 L C_1 C_2 h_{ie} + s^2 L C_2 + s h_{ie} (C_1 + C_2) + 1}$$

$$\therefore \quad 1 = \frac{-h_{fe}}{s^3 L C_1 C_2 h_{ie} + s^2 L C_2 + s h_{ie} (C_1 + C_2) + 1} \quad \ldots (6)$$

Replacing s by jω, and s^2 by $-\omega^2$ and s^3 by $-j\omega^3$

$$\therefore \quad 1 = \frac{-h_{fe}}{-j\omega^3 L C_1 C_2 h_{ie} - \omega^2 L C_2 + j\omega h_{ie} (C_1 + C_2) + 1}$$

$$= \frac{-h_{fe}}{(1 - \omega^2 L C_2) + j\omega h_{ie} [C_1 + C_2 - \omega^2 L C_1 C_2]} \quad \ldots (7)$$

There is no need to rationalize this as there are no j terms in the numerator, as in the equation (6 of 4.10.2).

It can be seen that, to satisfy the equation, the imaginary part of the denominator of the right hand side must be zero.

$$\therefore \quad \omega h_{ie} [C_1 + C_2 - \omega^2 L C_1 C_2] = 0$$

$$\therefore \quad C_1 + C_2 - \omega^2 L C_1 C_2 = 0$$

$$\therefore \quad \omega^2 = \frac{(C_1 + C_2)}{L C_1 C_2} = \frac{1}{L\left[\frac{C_1 C_2}{(C_1 + C_2)}\right]}$$

$$\therefore \quad \boxed{\omega = \frac{1}{\sqrt{L\left[\frac{C_1 C_2}{(C_1 + C_2)}\right]}}}$$

Now $\frac{C_1 C_2}{C_1 + C_2}$ is nothing but the equivalent of two capacitors C_1 and C_2 in series.

$$\therefore \quad \boxed{C_{eq} = \frac{C_1 C_2}{C_1 + C_2}}$$

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$$\therefore \quad \boxed{\omega = \frac{1}{\sqrt{L\,C_{eq}}}} \qquad \ldots(8)$$

$$\therefore \quad \boxed{f = \frac{1}{2\pi\sqrt{L\,C_{eq}}}} \qquad \ldots(9)$$

This is the frequency of the oscillations in the Colpitts oscillator.

Substituting this frequency in the equation (7) and equating the magnitudes of the both sides, the restriction on the value of h_{fe} can be obtained as,

$$\boxed{h_{fe} = \frac{C_2}{C_1}} \qquad \ldots(10)$$

Thus the behaviour of Colpitts oscillator is similar to the Hartley oscillator, as basic LC oscillator circuit is same, except the tank circuit.

Key Point: *The Colpitts oscillator is very commonly used as local oscillator in superheterodyne radio receiver.*

4.10.3 Colpitts Oscillator using FET

If in the basic circuit of Colpitts oscillator, the FET is used as an active device in the amplifier stage, the circuit is called as FET Colpitts oscillator. The tank circuit remains same as before. The working of the circuit and oscillating fequency also remains the same.

The practical circuit of FET Colpitts oscillator is shown in the Fig. 4.37.

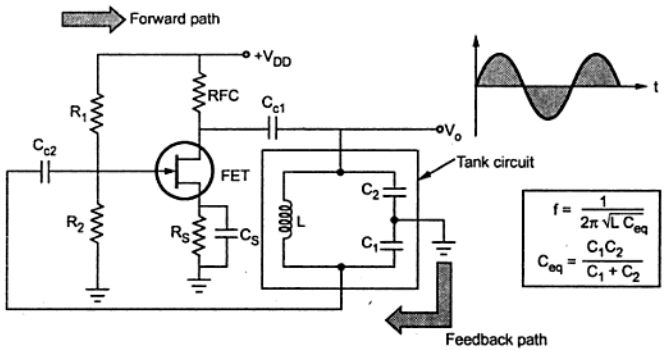

Fig. 4.37 FET Colpitts oscillator

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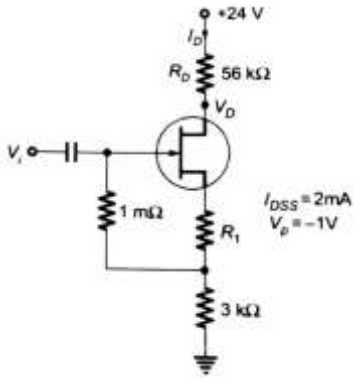
Unit 3

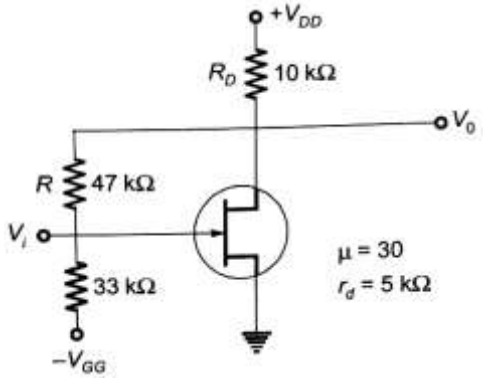
Tutorial sheet 3.1

Q1. Explain when the channel is said to be pinched-off and cut-off in MOS transistor?

Q2. Find the value of R_1 in the amplifier circuit shown below such that the quiescent drain to ground voltage becomes 10 V.

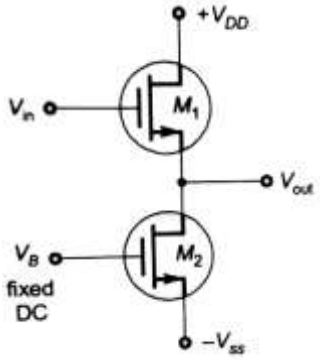


Q3. Determine the voltage gain $A_v=V_0/V_i$ for the amplifier circuit shown below, V_i is the input voltage between the gate terminal and ground. Neglect all capacitances

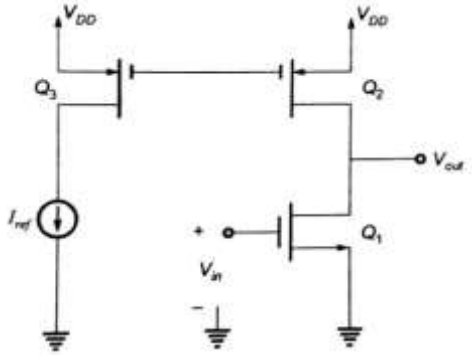


Q4. With neat sketch, explain drain characteristics of an n-channel enhancement MOSFET?

Q5. The figure below shows a source follower using n-channel MOSFETs. Assuming that M_1 and M_2 both are in saturation and have different transconductance parameters K_1 and K_2 where $K_i = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right) i; i = 1, 2$ and symbols have their usual meaning. Derive an expression for V_{out}, in terms of V_{in}, V_{DD}, V_s, V_B, V_{th} and, K_1 and K_2. Find out the small signal voltage gain and DC offset voltage appearing at output.

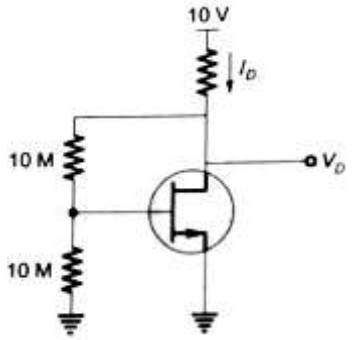


Q6. In the following circuit:



If V_{DD}=10V, V_{tn}=|V_{tp}|=1V, $\mu_n C_{ox}$=2 $\mu_p C_{ox}$ μA/V^2, W = 100 μm, L = 10 μm and |V_A|= Early voltage = 100 V both for n and p devices, I_{ref} = 100 μA, find the small voltage gain.

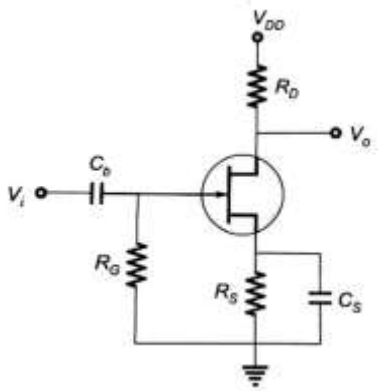
Q7. Analyze the circuit of figure to determine the drain current and drain voltage. Assume that the depletion type MOSFET has V_T= -1.0 V, k = 0.5 mA/V^2 and λ = 0.



Q8. For a particular IC fabrication, the quantity $\frac{1}{2}\mu_n C_{ox} = 10$ μA/V^2 and V_T = 1 V. In an application in which V_{GS} = V_{DS} = V_{supply} = 5 V a drain current of 0.8 mA is required of device of minimum length 2 μm. What value of channel width must the design use?

Q9. Discuss about nMOS transistor as a switch and pMOS transistor as a switch?

Q10. The amplifier shown in figure utilize an n-channel FET for which V_p = -2.0 V and I_{DSS} = 1.65 mA. It is required to bias the circuit at I_{DS} = 0.8 mA using V_{DD} = 24 V. Assume r_d >> R_d. Find (i) V_{GS}, (ii) g_m, (iii) R_s and (iv) R_d, such that the voltage gain is at least 20 dB with R_S bypassed with a very large capacitor C_S.

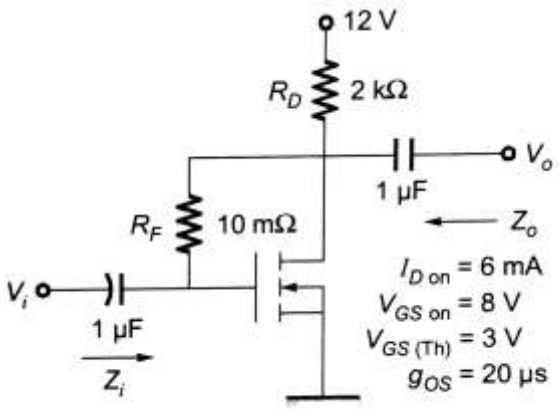


Unit 3

Tutorial sheet 3.2

Q1. Explain the MOS transistor operation with the help of neat sketches in the Depletion mode?

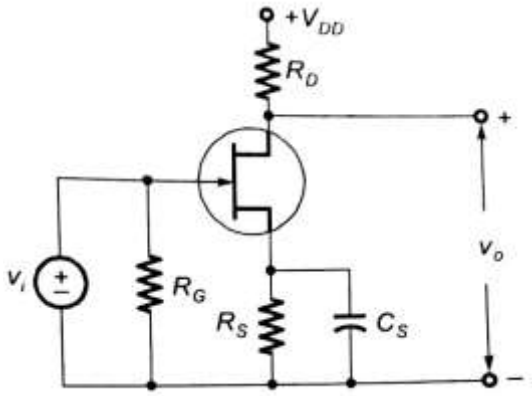
Q2. For the E-MOSFET of below figure. Determine;



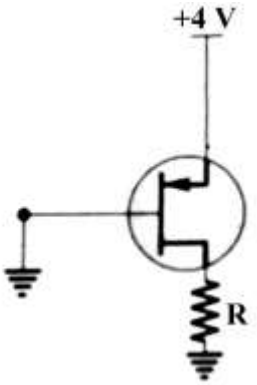
a. g_m
b. Find r_d
c. Calculate Z_i with and without r_d and compare result.
d. Calculate Z_0 with and without r_d and compare result.
e. Find A_V with and without r_d and compare result.
Given that k = 0.24 × 10^{-3} A/V^2, V_{GSQ} = 6.4; I_{DQ} = 2.75 mA.

Q3. Derive an equation for I_{DS} of an n-channel Enhancement MOSFET operating in Saturation region?

Q4. In the common source amplifier shown, evaluate voltage gain A_V given R_D = 2.7 kohm, μ = 50 and r_{ds} = 25 kohm. Derive the expression used.



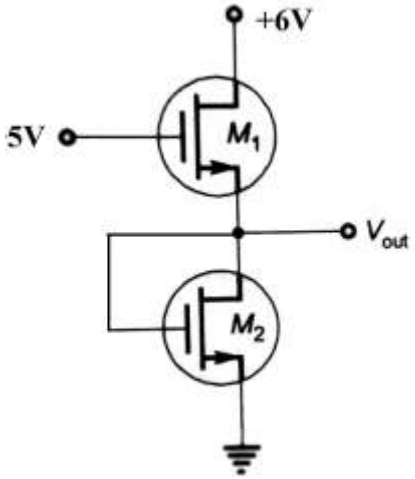
Q5. Find the value of R, where 1mA current for which PMOS transistor will be in the linear region.



Q6. (a) For a PMOS device, the threshold voltage is V_{TP} = -2 V and the applied source-to-gate voltage is V_{SG} = 3 V. Determine the region of operation when: (i) V_{SD} = 0.5 V; (ii) V_{SD} = 2 V; and (iii) V_{SD} = 5 V. (b) Repeat part (a) for a depletion- mode PMOS device with V_{TP} = 0.5 V.

Q7. Derive an equation for transconductance of an n-channel enhancement MOSFET operating in active region?

Q8. In the circuit shown below, For MOS transistor $\mu_n C_{cox}$ = 100 $\mu A/V^2$, V_T = 1 V. What is the value of V_{out}?



Q9. Give the high frequency small-signal circuit of a MOSFET with load resistance showing the effect of Miller capacitance. Also derive an expression for the Miller Capacitance and cut-off frequency (f_T).

Q10. In a self-bias n channel JFET, the operating point is to be set at I_D = 1.5 mA and V_{DS} = 10 V. The JFET parameters are I_{DSS} = 5 mA and V_P = -2V. Find the value of R_s and R_D for given V_{DD} = 20 V, draw the circuit diagram also.

Unit 4

Tutorial sheet4.1

Q1. What do you understand by feedback in amplifiers? Explain the terms feedback factor and open loop gain.

Q2. What are the different types of negative feedback? Explain how the input and output impedances of an amplifier are affected by different types of negative feedback?

Q3. What is the sensitivity of an amplifier?

Q4. An amplifier with open loop voltage gain $A_0 = 1000 \pm 100$ is available. It is required to have an amplifier whose voltage gain varies by no more than ± 0.1 percentage.

a. Find the value of the feedback factor required.
b. Find the gain with feedback

Q5. What are the effect of negative voltage series feedback on the characteristics of an amplifier? Derive an expression for input resistance of such an amplifier with feedback in terms of input resistance and feedback factor.

Q6. An amplifier with open loop voltage gain $A_V = 1000 \pm 100$ is available. It is required to have an amplifier whose gain varies by no more than ± 0.2 percentage.

a. Find the reverse transmission factor β of the feedback network.
b. Find the gain with feedback

Q7. Show that a feedback amplifier can be made to work as an amplifier.

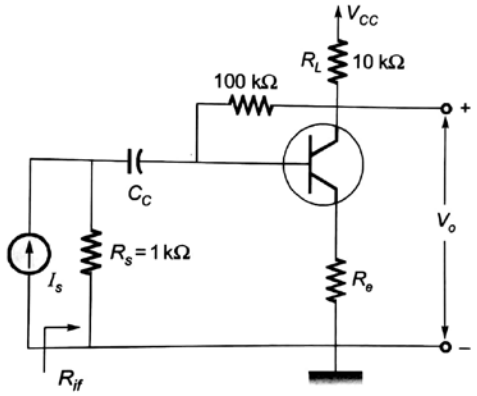
Q8. An amplifier with an open loop voltage gain of 500 delivers 10 W of output power at 5% second harmonic distortion when the input signal is 5 mV. If 20 dB negative feedback is applied and output power has to remain 10 W, determine

a. The required input signal strength.
b. The percentage second harmonic distortion

Q9. For the f_b amplifier shown below determine:

a. $R_{mf} = V_0/I_s$, where $I_s = V_s/R_s$
b. $A_{vf} = V_0/V_s$ and
c. R_{if}

Assume $R_e = 0$, $h_{fe} = 100$, $h_{ie} = 1k\Omega$, $h_{re} = h_{oe} = 0$.



Q10. State the condition of $(1 + A\beta)$ for which a feedback amplifier must satisfy in order to be stable.

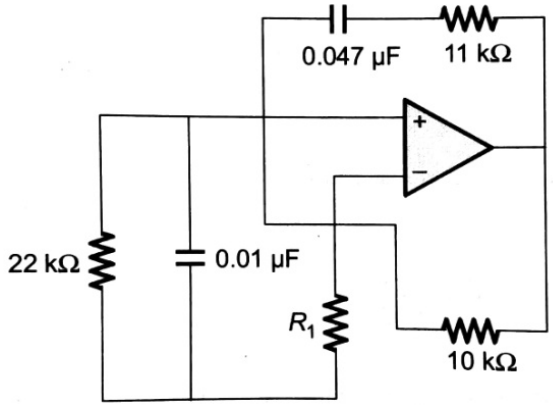
Unit 4

Tutorial sheet 4.2

Q1. Explain the main difference between an amplifier and an oscillator.

Q2. State and briefly explain the Barkhausen criterion for oscillation.

Q3. Determine the frequency of oscillation for the circuit shown below and the value of R_1 needed to maintain oscillations.

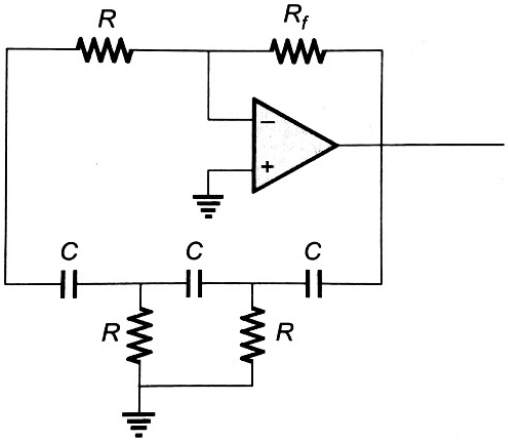


Q4. Derive the expression for the frequency of oscillations and condition for sustained oscillations in a Colpitt's oscillator.

Q5. Explain the principle of working of transistor Hartely oscillator. Draw circuit diagramand briefly function of each component.

Q6. In an Hartley oscillator, if L_1 = 0.2 mH, L_2 = 0.3 mH and C = 0.003 μF, calculate the frequency of its oscillations.

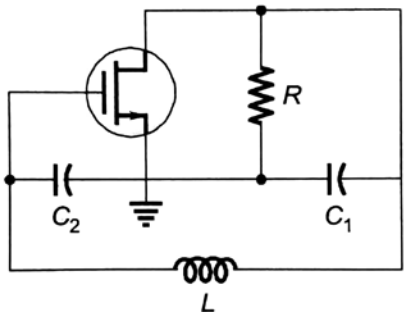
Q7. Minimum three identical *RC* high pass section connected in cascade are required in a phase shift oscillators. Justify, one such phase shift oscillator is shown below. Why is *R* of one section connected to virtual ground instead of actual ground?



Determine the value of R_f. What should be next higher number of high pass section connected in cascade? Draw the corresponding circuit of the oscillator.

Q8. Explain the principle of Clapp oscillator.

Q9. Consider the AC equivalent circuit of a MOSFET Colpitts oscillator.



Derive the expression for the oscillation frequency. Also find the condition on the gain to initiate the oscillations spontaneously.

Q10. As per the Barkhausen criterion, the positive feedback exists over a particular frequency range and the resulting feedback signal reinforces the error signal. Explain the phenomenon which limits the amplitude of oscillations under steady state. (Consider the figure given in Q9.)