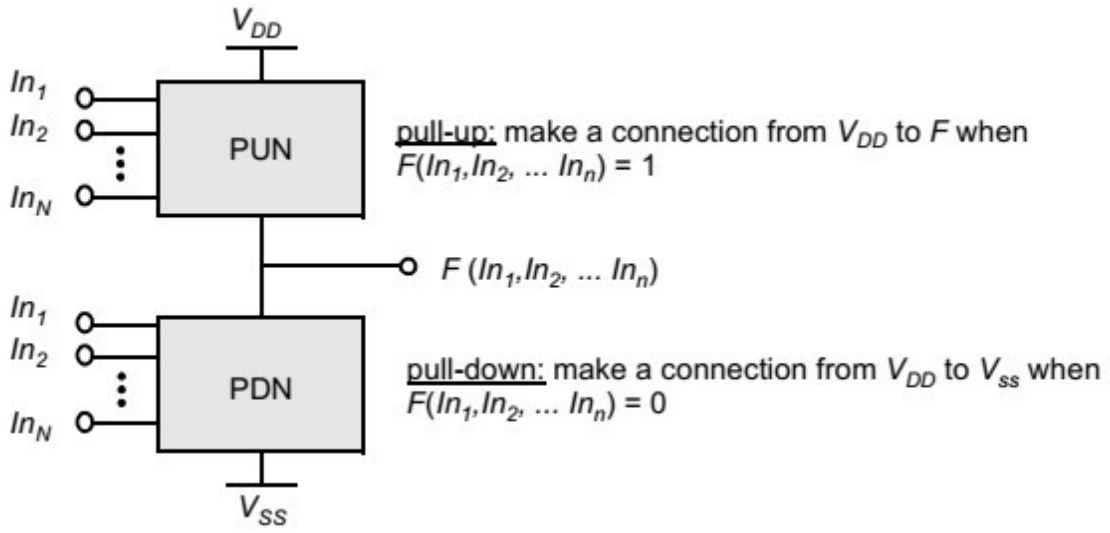
1. Static CMOS Design

The complementary CMOS circuit style falls under a broad class of logic circuits called *static* circuits in which at every point in time (except during the switching transients), each gate output is connected to either VDD or Vss via a low-resistance path. Also, the outputs of the gates assume at all times the value of the Boolean function implemented by the circuit (ignoring, once again, the transient effects during switching periods).

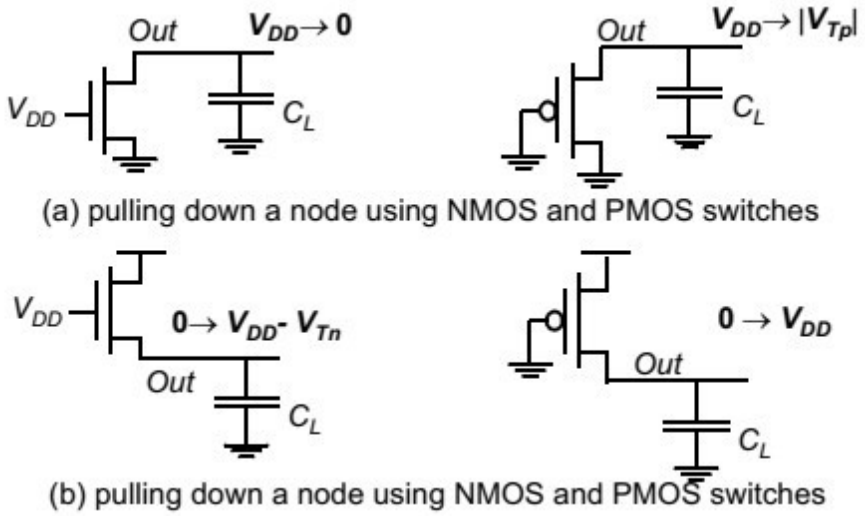
a. Complementary CMOS

Concept

A static CMOS gate is a combination of two networks, called the pull-up network (PUN) and the pull-down network(PDN). The figure shows a generic N input logic gate where all inputs are distributed to both the pull-up and pull-down networks.



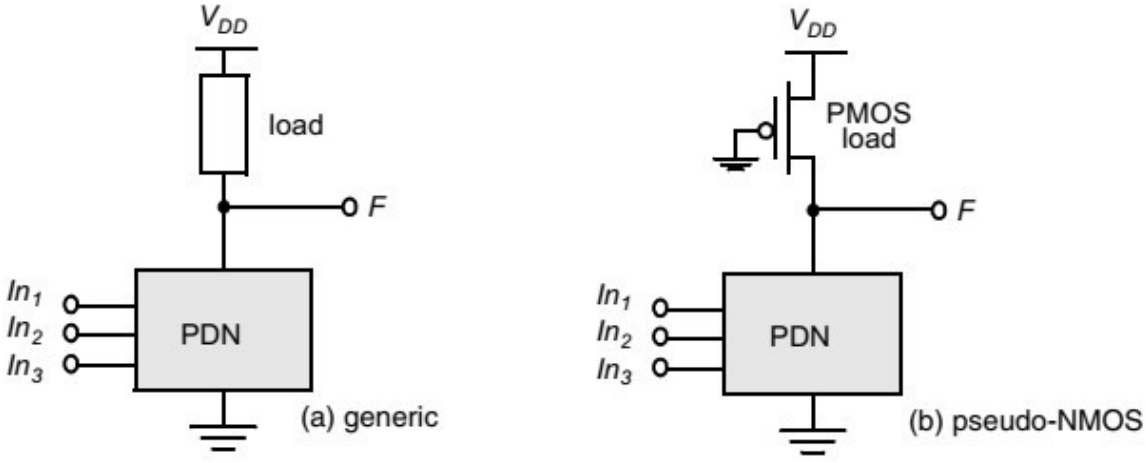
Complementary logic gate as a combination of a PUN (pull-up network) and a PDN (pull-down network)



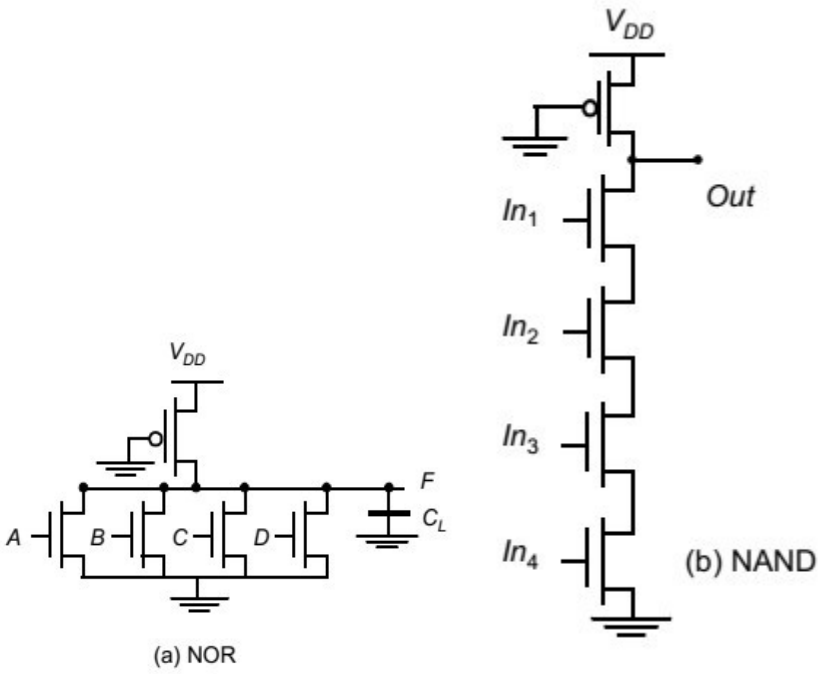
b. Ratioed Logic

Concept

Ratioed logic is an attempt to reduce the number of transistors required to implement a given logic function, at the cost of reduced robustness and extra power dissipation. The purpose of the PUN in complementary CMOS is to provide a conditional path between *VDD* and the output when the PDN is turned off. In ratioed logic, the entire PUN is replaced with a single unconditional load device that pulls up the output for a high output. Instead of a combination of active pull-down and pull-up networks, such a gate consists of an NMOS pull-down network that realizes the logic function, and a simple load device.



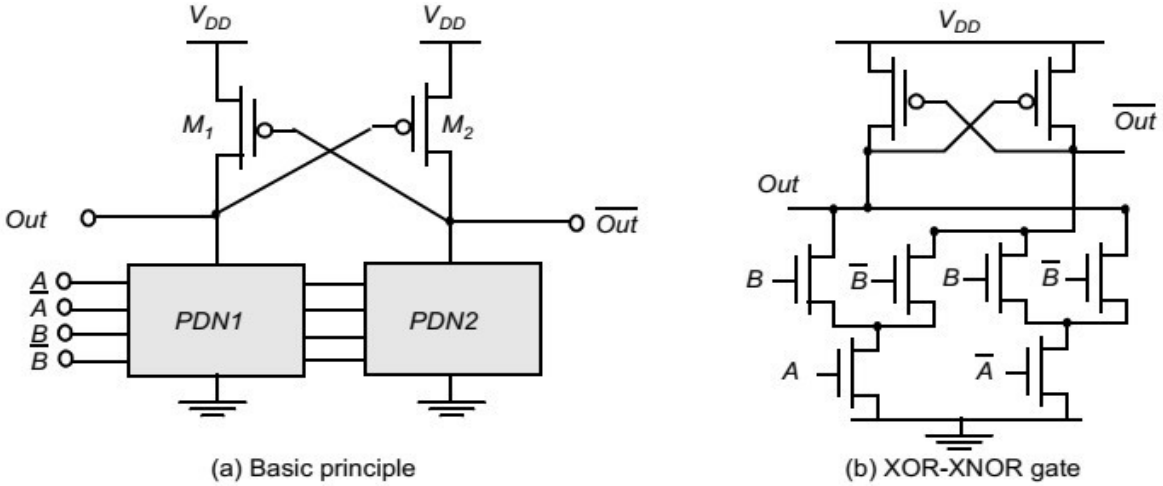
Ratioed logic gate.



Four-input pseudo-NMOS NOR and NAND gates

DCVSL logic gate:

To create a ratioed logic style that completely eliminates static currents and provides rail-to-rail swing. Such a gate combines two concepts: *differential logic* and *positive feedback*. A differential gate requires that each input is provided in complementary format, and produces complementary outputs in turn. The feedback mechanism ensures that the load device is turned off when not needed. Example of such a logic family, called Differential Cascode Voltage Switch Logic (or DCVSL).



DCVSL logic gate