VLSI Design (BEC-41)
(Unit-1, Lecture-3)

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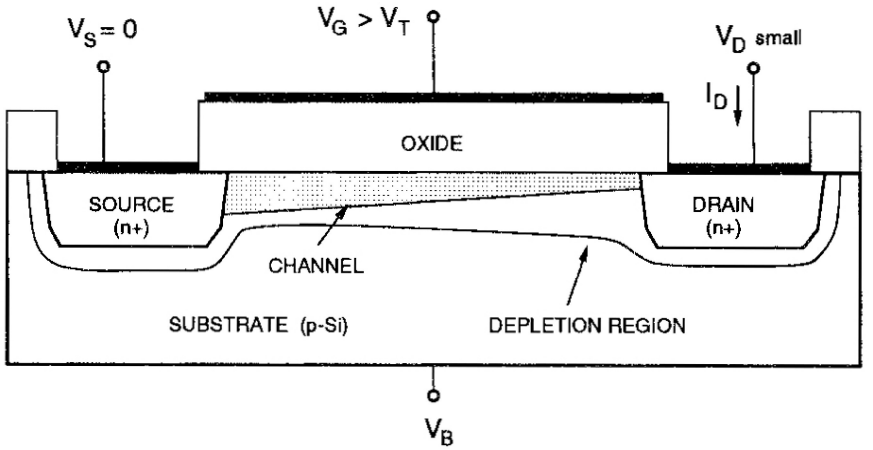
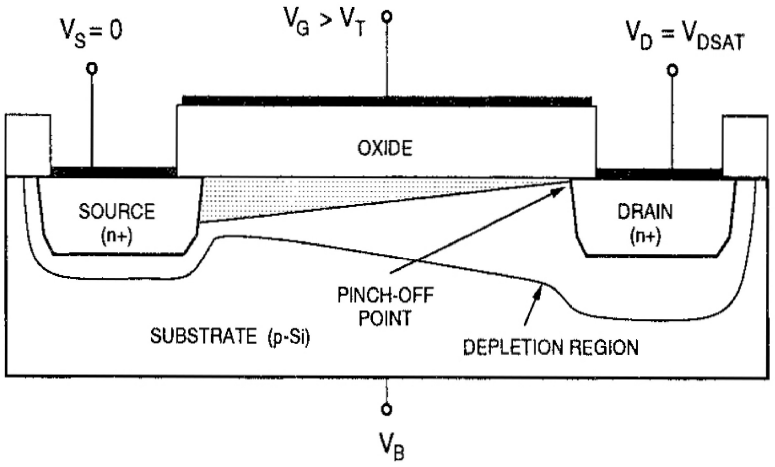
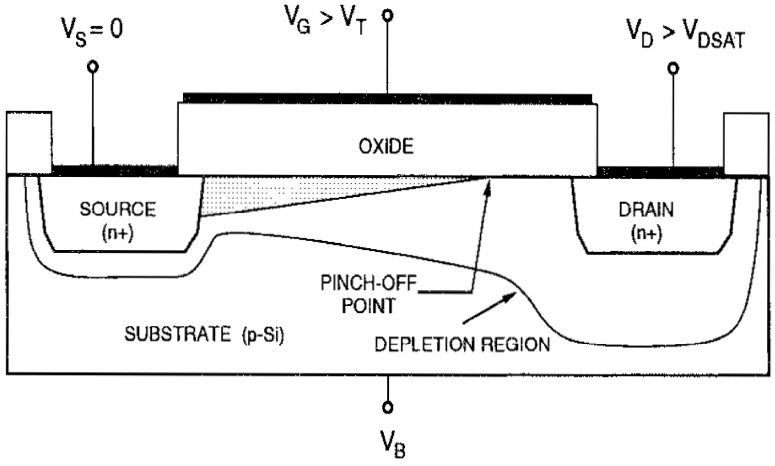
MOSFET operation: linear region

- The MOSFET consists
  - A MOS capacitor, two pn junction adjacent to the channel
  - The channel is controlled to the MOS gate
- The carrier (electron in nMOSFET)
  - Entering through source, controlling by gate, leaving through drain
- To ensure that both p-n junctions are reverse-biased initially
  - The substrate potential is kept lower than the other three terminal potentials
- When $0<V_{GS}<V_{T0}$
  - G-S region depleted, G-D region depleted
  - No current flow
- When $V_{GS}>V_{T0}$
  - Conduction channel formed
  - Capable of carrying the drain current
  - As $V_{DS}=0$
    - $I_D=0$
  - As $V_{DS}>0$ and small
    - I_D proportional to V_{DS}
    - Flowing from S to D through the conducting channel
    - The channel act as a voltage controlled resistor
    - The electron velocity much lower than the drift velocity limit
    - As $V_{DS}\uparrow\Rightarrow$the inversion layer charge and the channel depth at the drain end start to decrease



MOSFET operation: saturation region





- For $V_{DS}=V_{DSAT}$
  - The inversion charge at the drain is reduced to zero
  - *Pitch off* point
- For $V_{DS}>V_{DSAT}$
  - A depleted surface region forms adjacent to the drain
  - As further increases V_{DS} ⇨ this depletion region grows toward the source
  - The channel-end remains essentially constant and equal to V_{DSAT}
  - The pitch-off (depleted) section
    - Absorbing most of the excess voltage drop, V_{DS}-V_{DSAT}
    - A high-field forms between the channel-end of the drain boundary
      - Accelerating electrons, usually reaching the drift velocity limit

MOSFET current-voltage characteristics-gradual channel approximation (GCA)(1)

- Considering linear mode operation
  - $V_S=V_B=0$, the V_{GS} and V_{DS} are the external parameters controlling the drain current I_D
  - $V_{GS} > V_{T0}$ (assume constant through the channel) to create a conducting inversion layer
  - Defining
    - X-direction: perpendicular to the surface, pointing down into the substrate
    - Y-direction: parallel to the surface
      - The y=0 is at the source end of the channel
      - Channel voltage with respect to the source, $V_c(y)$
  - Assume the electric field E_y is *dominant* compared with E_x
    - This assumption reduced ⇨the current flow in the channel to the y-direction only
  - Let $Q_I(y)$ be the total mobile electron charge in the surface inversion layer
    - $Q_I(y)=-C_{ox}[V_{GS}-Vc(y)-V_{T0}]$

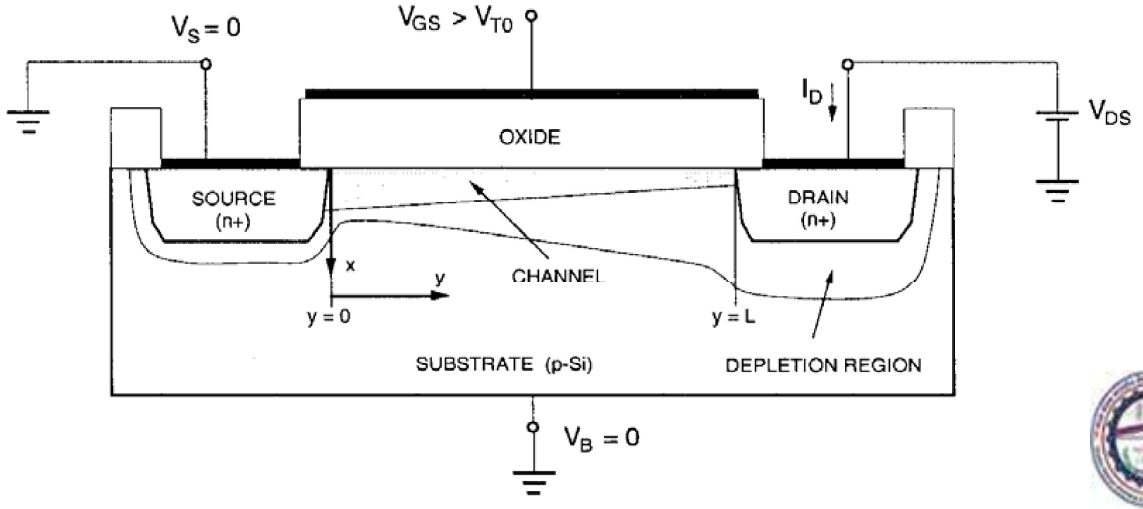


Figure 3.15 Cross-sectional view of an n-channel transistor, operating in linear region.

MOSFET current-voltage characteristics-gradual channel approximation (GCA)(2)

Assumeing that all mobile electrons in the inversion layer has a constant surfacr mobility μ_n

$dR = -\dfrac{dy}{W \cdot \mu_n \cdot Q_I(y)}$ (mimus sign is due to the negative polarity of the inversion layer charge Q_I)

The electron surface mobility μ_n dependents on the doping concentration of the channel region, and its magnitude is typically about one - half of that of the bulk electron mobility

$$dV_C = I_D \cdot dR = -\frac{I_D}{W \cdot \mu_n \cdot Q_I(y)} \cdot dy$$

$$\int_0^L I_D \cdot dy = -W \cdot \mu_n \int_0^{V_{DS}} Q_I(y) \cdot dV_C$$

$$I_D \cdot L = W \cdot \mu_n \cdot C_{ox} \int_0^{V_{DS}} \left(V_{GS} - V_C - V_{T0}\right) \cdot dV_C$$

$$I_D = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot \left[2 \cdot \left(V_{GS} - V_{T0}\right) V_{DS} - V_{DS}^2\right]$$

$$I_D = \frac{k'}{2} \cdot \frac{W}{L} \cdot \left[2 \cdot \left(V_{GS} - V_{T0}\right) V_{DS} - V_{DS}^2\right] \quad where\ k' = \mu_n C_{ox}$$

$$I_D = \frac{k}{2} \cdot \left[2 \cdot \left(V_{GS} - V_{T0}\right) V_{DS} - V_{DS}^2\right] \quad where\ k = k' \cdot \frac{W}{L}$$

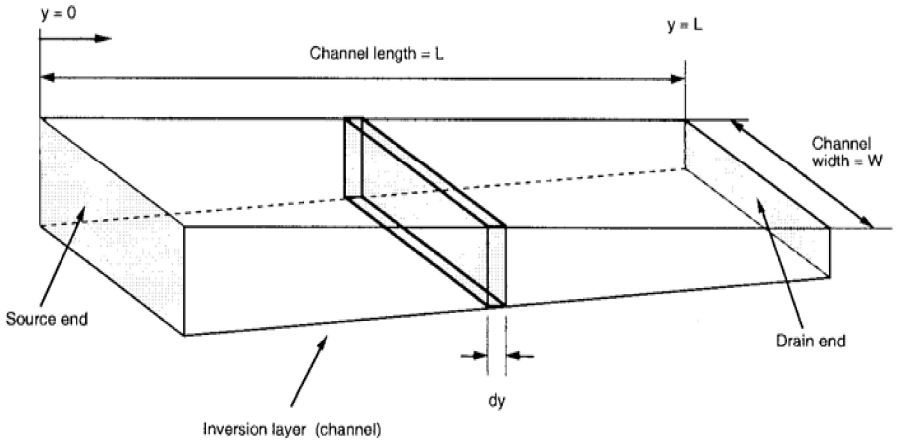


Figure 3.16 Simplified geometry of the surface inversion layer (channel region).

Example 4

For an n-channel MOS transistor with $\mu_n = 600\,\text{cm}^2/\text{V}\cdot\text{s}$, $C_{ox} = 7 \cdot 10^{-8}$ F/cm^2, $W = 20\ \mu\text{m}$, $L = 2\ \mu\text{m}$ and $V_{T0} = 1.0$ V, examine the relationship between the drain current and the terminal voltages.

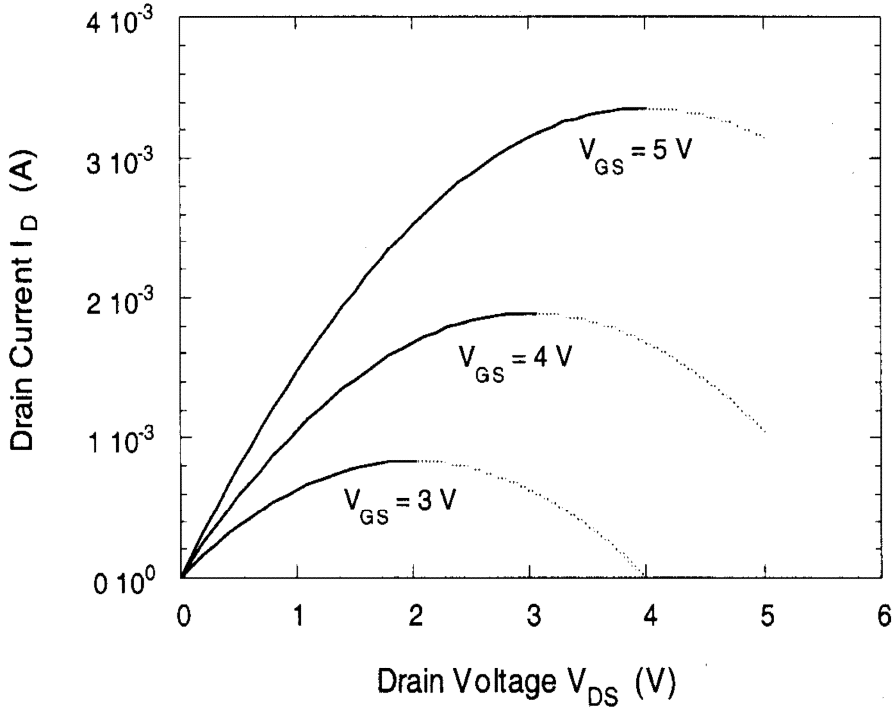
First, calculate the parameter k:

$$k = \mu_n \cdot C_{ox} \cdot \frac{W}{L} = 600\ \text{cm}^2/\text{V}\cdot\text{s} \times 7 \cdot 10^{-8}\ \text{F/cm}^2 \times \frac{20\ \mu\text{m}}{20\ \mu\text{m}} = 0.42\ \text{mA/V}^2$$

Now, the current-voltage equation (3.34) can be written as follows.

$$I_D = 0.21\ \text{mA/V}^2 \left[2 \cdot (V_{GS} - 1.0) \cdot V_{DS} - V_{DS}^2\right]$$

To examine the effect of the gate-to-source voltage and the drain-to-source voltage upon the drain current, we will plot I_D as a function of V_{DS}, for different (constant) values of V_{GS}. It can easily be seen that the second-order current-voltage equation given above produces a set of inverted parabolas for each constant V_{GS} value.



The drain current-drain voltage curves shown on page 104 reach their peak value for $V_{DS} = V_{GS} - V_{T0}$. Beyond this maximum, each curve exhibits a *negative* differential conductance, which is not observed in actual MOSFET current-voltage measurements (section shown by the dashed lines). We must remember now that the drain current equation (3.32) has been derived under the following voltage assumptions,

$$V_{GS} \geq V_{T0}$$

$$V_{GD} = V_{GS} - V_{DS} \geq V_{T0}$$

which guarantee that the entire channel region between the source and the drain is inverted. This condition corresponds to the *linear* operating mode for the MOSFET, which was examined qualitatively in Section 3.4. Hence, the current equation (3.32) is valid only for the linear mode operation. Beyond the linear region boundary, i.e., for V_{DS} values *larger* than $V_{GS} - V_{T0}$, the MOS transistor will be assumed to be in *saturation*. A different current-voltage expression will be necessary for the MOSFET operating in this region.

MOSFET current-voltage characteristics-gradual channel approximation (GCA)-saturation region

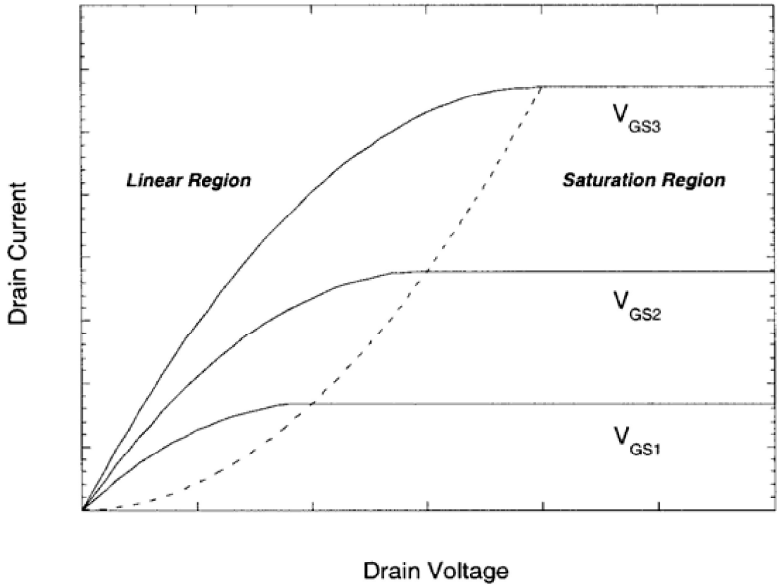


Figure 3.17 Basic current-voltage characteristics of an n-channel MOS transistor.

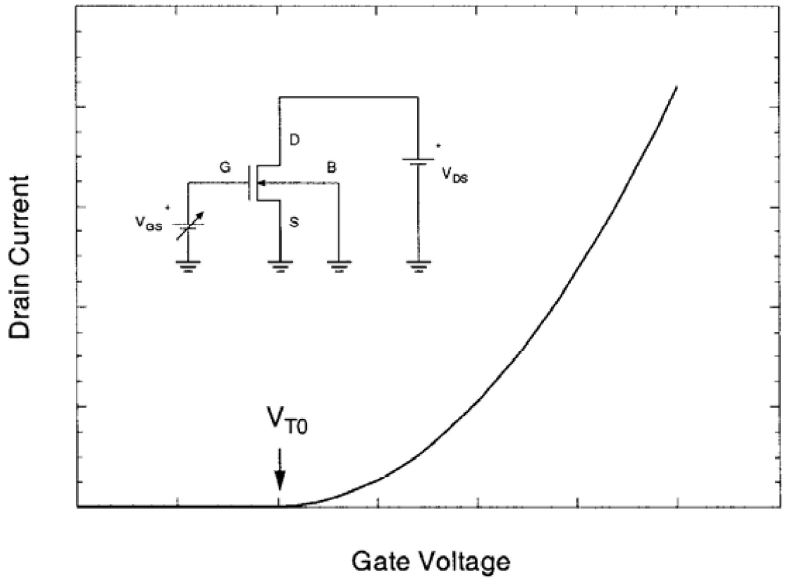


Figure 3.18 Drain current of the n-channel MOS transistor as a function of the gate-to-source voltage V_{GS}, with $V_{DS} > V_{DSAT}$ (transistor in saturation).

- For $V_{DS} \geq V_{DSAT} = V_{GS} - V_{T0}$
  - $$I_{D(sat)} = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot \left[2 \cdot (V_{GS} - V_{T0}) \cdot (V_{GS} - V_{T0}) - (V_{GS} - V_{T0})^2\right]$$
    $$= \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_{T0})^2$$
  - The drain current becomes a function only of V_{GS}, beyond the saturation boundary

Channel length modulation

The inversion layer charge at the source end of the channel is

$$Q_I(y=0) = -C_{ox} \cdot (V_{GS} - V_{T0})$$

and the inversion layer charge at the drain end of the channel is

$$Q_I(y=L) = -C_{ox} \cdot (V_{GS} - V_{T0} - V_{DS})$$

Note that at the edge of saturation, $V_{DS} = V_{DSAT} = V_{GS} - V_{T0}$

The inversion layer charge at the drain end become very small

$$Q_I(y=L) \approx 0$$

The effective channel length $L' = L - \Delta$-

where $\Delta\Delta$ is the length of the channel segment with $Q_I = 0$

$$I_{D(sat)} = \frac{\mu_n C_{ox}}{2} \cdot \frac{W}{L'} \cdot (V_{GS} - V_{T0})^2$$

$$I_{D(sat)} = \left(\frac{1}{1 - \frac{\Delta L}{L}} \right) \frac{\mu_n C_{ox}}{2} \cdot \frac{W}{L'} \cdot (V_{GS} - V_{T0})^2$$

$$\Delta L \propto \sqrt{V_{DS} - V_{DSAT}}$$

We use $1 - \frac{\Delta L}{L} \approx 1 - \lambda \cdot V_{DS}$, λ channel length modulation coeffic

Assuming that $\lambda\lambda_{DS} << 1$

$$I_{D(sat)} = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_{T0})^2 \cdot (1 + \lambda V_{DS})$$

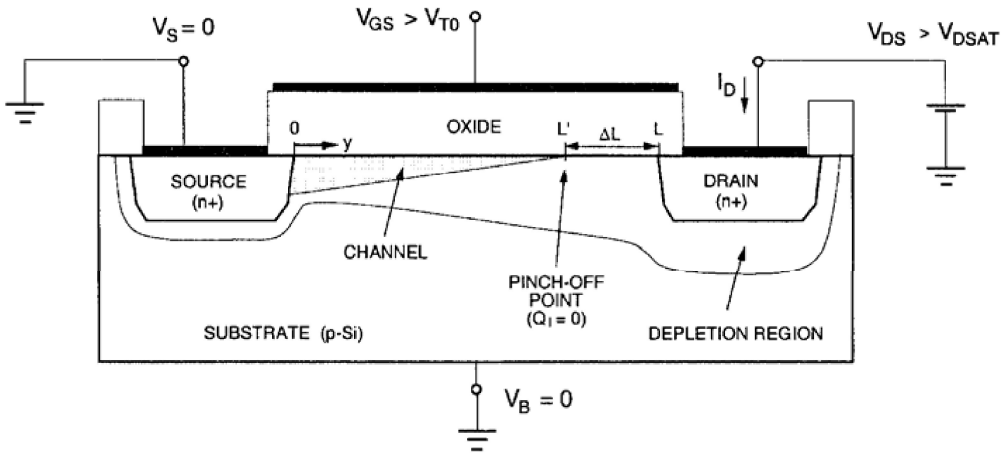


Figure 3.19 Channel length modulation in an n-channel MOSFET operation in saturation mode.

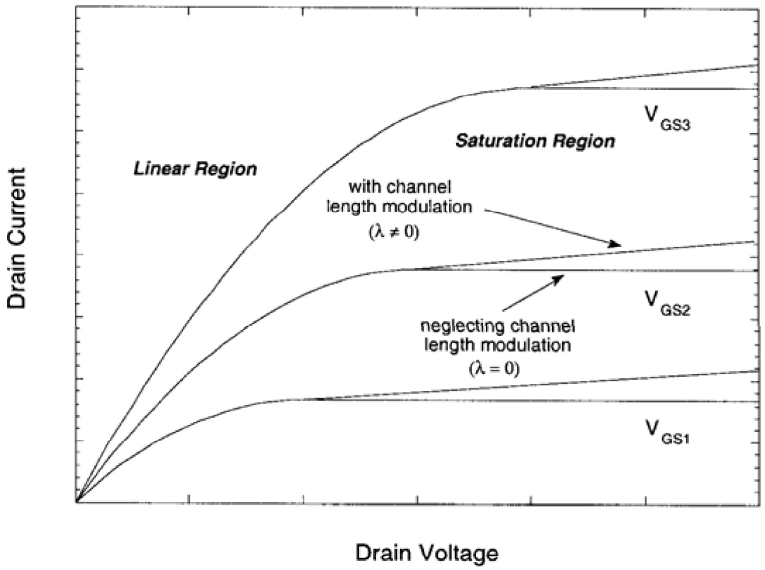


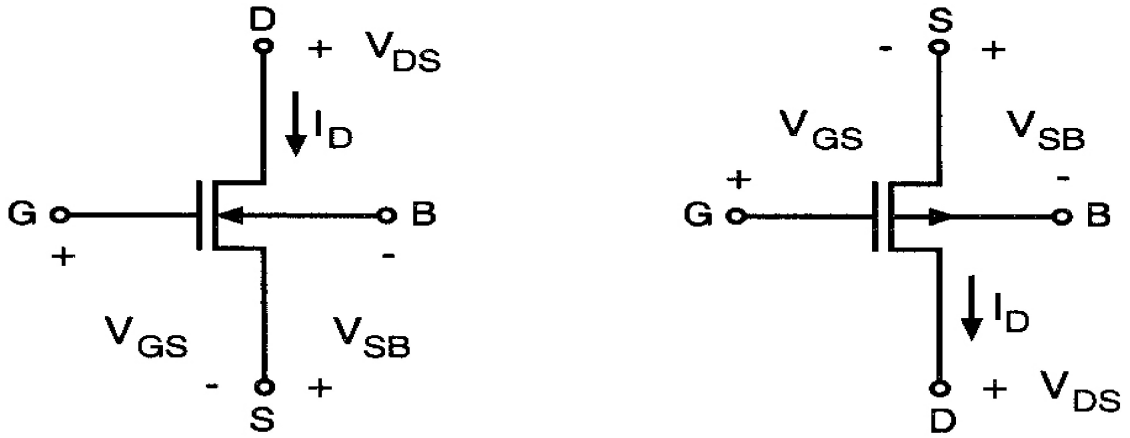
Figure 3.20 Current-voltage characteristics of an n-channel MOS transistor, including the channel length modulation effect.

Substrate bias effect

- The discussion in the previous has been done under the assumption
  - The substrate potential is equal to the source potential, i.e. $V_{SB}=0$
- On the other hand
  - the source potential of an nMOS transistor can be larger than the substrate potential, i.e. $V_{SB}>0$
  - $V_T(V_{SB}) = V_{T0} + \gamma \cdot \left(\sqrt{|2\phi_F| + V_{SB}} - \sqrt{|2\phi_F|} \right)$

$$I_{D(lin)} = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot \left[2 \cdot \left(V_{GS} - V_T(V_{SB}) \right) V_{DS} - V_{DS}^2 \right]$$

$$I_{D(sat)} = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot \left(V_{GS} - V_T(V_{SB}) \right)^2 \cdot \left(1 + \lambda \cdot V_{DS} \right)$$



n-channel MOSFET p-channel MOSFET

Figure 3.21 Terminal voltages and currents of the nMOS and the pMOS transistor.

Current-voltage equation of n-, p-channel MOSFET

For n - channel MOSFET

$$I_D = 0, \quad \text{for } V_{GS} < V_T$$

$$I_{D(lin)} = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot \left[2 \cdot (V_{GS} - V_T) V_{DS} - V_{DS}^2\right] \text{ for } V_{GS} \geq V_T$$

$$\text{and } V_{DS} < V_{GS} - V_T$$

$$I_{D(sat)} = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda \cdot V_{DS}) \text{ for } V_{GS} \geq V_T$$

$$\text{and } V_{DS} \geq V_{GS} - V_T$$

For p - channel MOSFET

$$I_D = 0, \quad \text{for } V_{GS} > V_T$$

$$I_{D(lin)} = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot \left[2 \cdot (V_{GS} - V_T) V_{DS} - V_{DS}^2\right] \text{ for } V_{GS} \leq V_T$$

$$\text{and } V_{DS} > V_{GS} - V_T$$

$$I_{D(sat)} = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda \cdot V_{DS}) \text{ for } V_{GS} \leq V_T$$

$$\text{and } V_{DS} \leq V_{GS} - V_T$$

Measurement of parameters- k_n, V_{T0}, and γ

- The V_{SB} is set at a constant value
  - The drain current is measured for different values of V_{GS}
  - V_{DG}=0
    - V_{DS}>V_{GS}-V_T is always satisfied ⇨ saturation mode
    - Neglecting the channel length modulation effect
      - $I_{D(sat)} = \frac{k_n}{2} \cdot (V_{GS} - V_{T0})^2, \sqrt{I_D} = \sqrt{\frac{k_n}{2}} \cdot (V_{GS} - V_{T0})$
      - Obtaining the parameters k_n, V_{T0}, and γ
      - $$\gamma = \frac{V_T(V_{SB}) - V_{T0}}{\sqrt{|2\phi_F| + V_{SB}} - \sqrt{|2\phi_F|}}$$

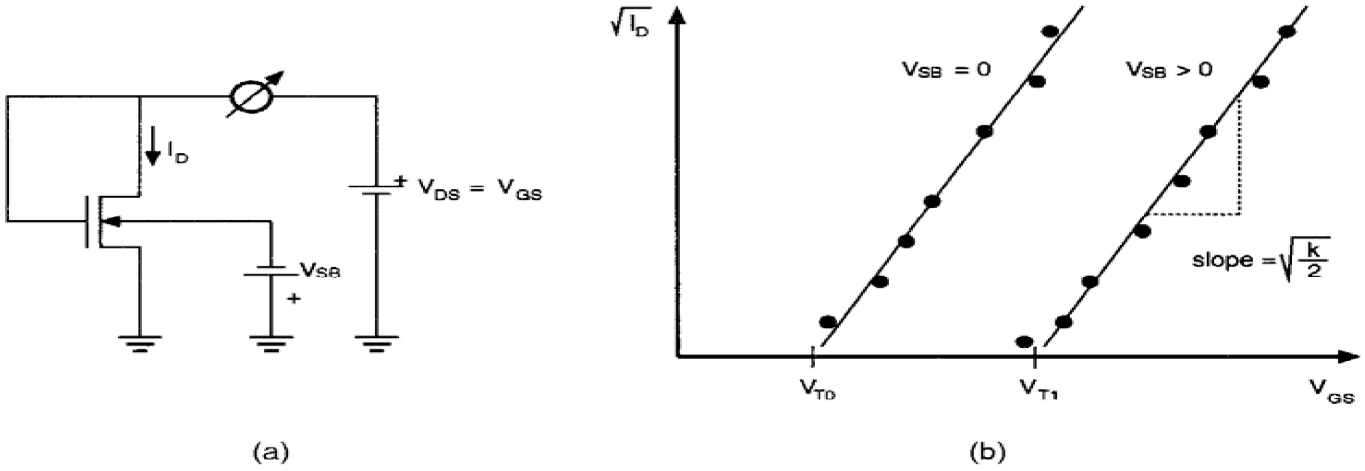


Figure 3.22 (a) Test circuit arrangement and (b) measured data for experimental determination of the parameters k_n, V_{T0}, and γ.

Measurement of parameters- λ

- The voltage V_{GS} is set to V_{T0}+1
- The voltage V_{DS} is chosen sufficiently large ($V_{DS}>V_{GS}-V_{T0}$) that the transistor operates in the saturation mode, V_{DS1}, V_{DS2}
  - $I_{D(sat)}=(k_n/2)(V_{GS}-V_{T0})^2(1+\lambda V_{DS})$
    - Since $V_{GS}=V_{T0}+1 \Rightarrow I_{D2}/I_{D1}=(1+\lambda V_{DS2})/(1+\lambda V_{DS1})$
    - Which can be used to calculate the channel length modulation coefficient λ
    - This is in fact equivalent to calculating the slope of the drain current versus drain voltage curve in the saturation region
      - The slope is $\lambda k_n/2$

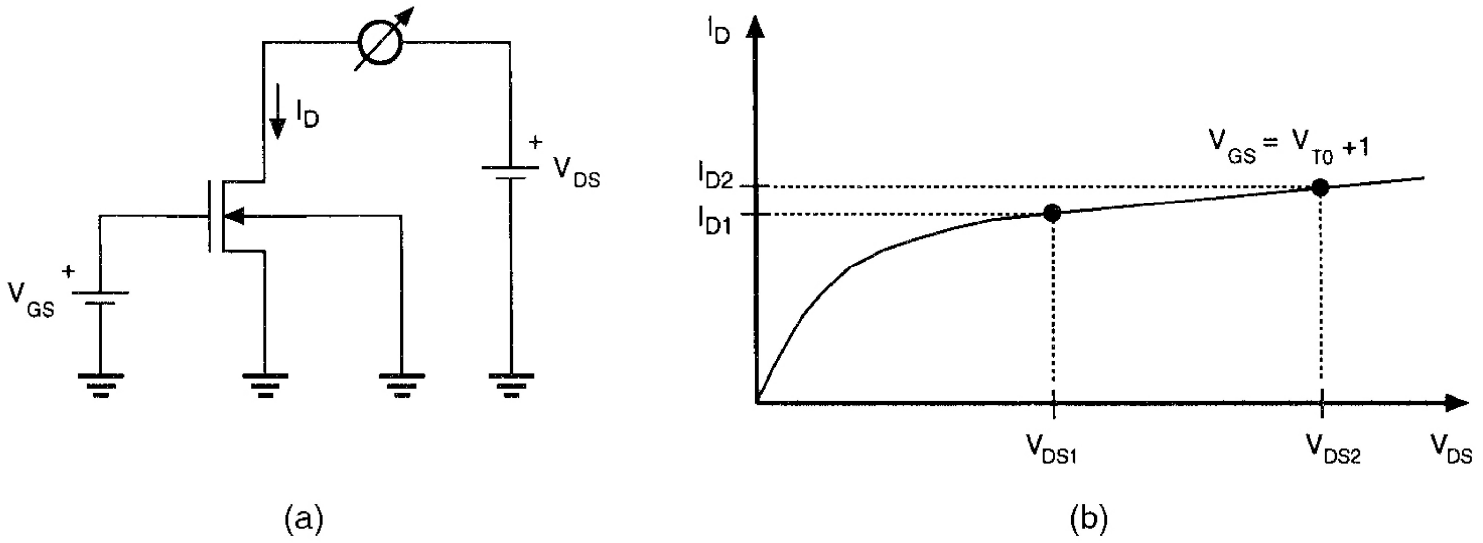


Figure 3.23 (a) Test circuit arrangement and (b) measured data for experimental determination of the channel length modulation coefficient λ.

Example 5

Measured voltage and current data for a MOSFET are given below. Determine the type of the device, and calculate the parameters k_n, V_{T0}, and γ. Assume $\phi_F = -0.3$ V.

V_{GS} (V)	V_{DS} (V)	V_{SB} (V)	I_D (μA)
3	3	0	97
4	4	0	235
5	5	0	433
3	3	3	59
4	4	3	173
5	5	3	347

First, the MOS transistor is on ($I_D > 0$) for $V_{GS} > 0$ and $V_{DS} > 0$. Thus, the transistor must be an n-channel MOSFET. Assume that the transistor is enhancement-type and, therefore, operating in saturation mode for $V_{GS} = V_{DS}$. Neglecting the channel length modulation effect, the saturation mode current is written as

$$I_D = \frac{k_n}{2} \cdot (V_{GS} - V_T)^2 \quad \Leftrightarrow \quad \sqrt{I_D} = \sqrt{\frac{k_n}{2}} \cdot (V_{GS} - V_T)$$

Let (V_{GS1}, I_{D1}) and (V_{GS2}, I_{D2}) be any two current-voltage pairs obtained from the table. Then, the square-root of the transconductance parameter k_n can be calculated.

$$\sqrt{\frac{k_n}{2}} = \frac{\sqrt{I_{D1}} - \sqrt{I_{D2}}}{V_{GS1} - V_{GS2}} = \frac{\sqrt{433\ \mu\text{A}} - \sqrt{97\ \mu\text{A}}}{5\ \text{V} - 3\ \text{V}} = 5.48 \times 10^{-3}\ \text{A}^{1/2}/\text{V}$$

Thus, the transconductance parameter of this n-channel MOSFET is:

$$k_n = 2 \cdot (5.48 \times 10^{-3})^2 = 60 \times 10^{-6}\ \text{A/V}^2 = 60\ \mu\text{A/V}^2$$

The *extrapolated threshold voltage* V_{T0} at zero substrate bias can be found by calculating the x-axis intercept of the *square-root of* (I_D) versus V_{GS} curve.

$$V_{T0} = V_{GS} - \sqrt{\frac{2 \cdot I_D}{k_n}} = 1.2\ \text{V}$$

To find the substrate bias coefficient γ, we must first determine the threshold voltage V_T at the source-to-substrate voltage of 3 V. Using one of the current-voltage data pairs corresponding to $V_{SB} = 3$ V, V_T can be calculated as follows:

$$V_T(V_{SB} = 3\ \text{V}) = V_{GS} - \sqrt{\frac{2 \cdot I_D}{k_n}} = 4\ \text{V} - \sqrt{\frac{2 \cdot 173\ \mu\text{A}}{60\ \mu\text{A/V}^2}} = 1.6\ \text{V}$$

Finally, the substrate bias coefficient is found as:

$$\gamma = \frac{V_T(V_{SB} = 3\ \text{V}) - V_{T0}}{\sqrt{|2\phi_F| + V_{SB}} - \sqrt{|2\phi_F|}} = \frac{1.6\ \text{V} - 1.2\ \text{V}}{\sqrt{0.6\ \text{V} + 3\ \text{V}} - \sqrt{0.6\ \text{V}}} = 0.36\ \text{V}^{1/2}$$