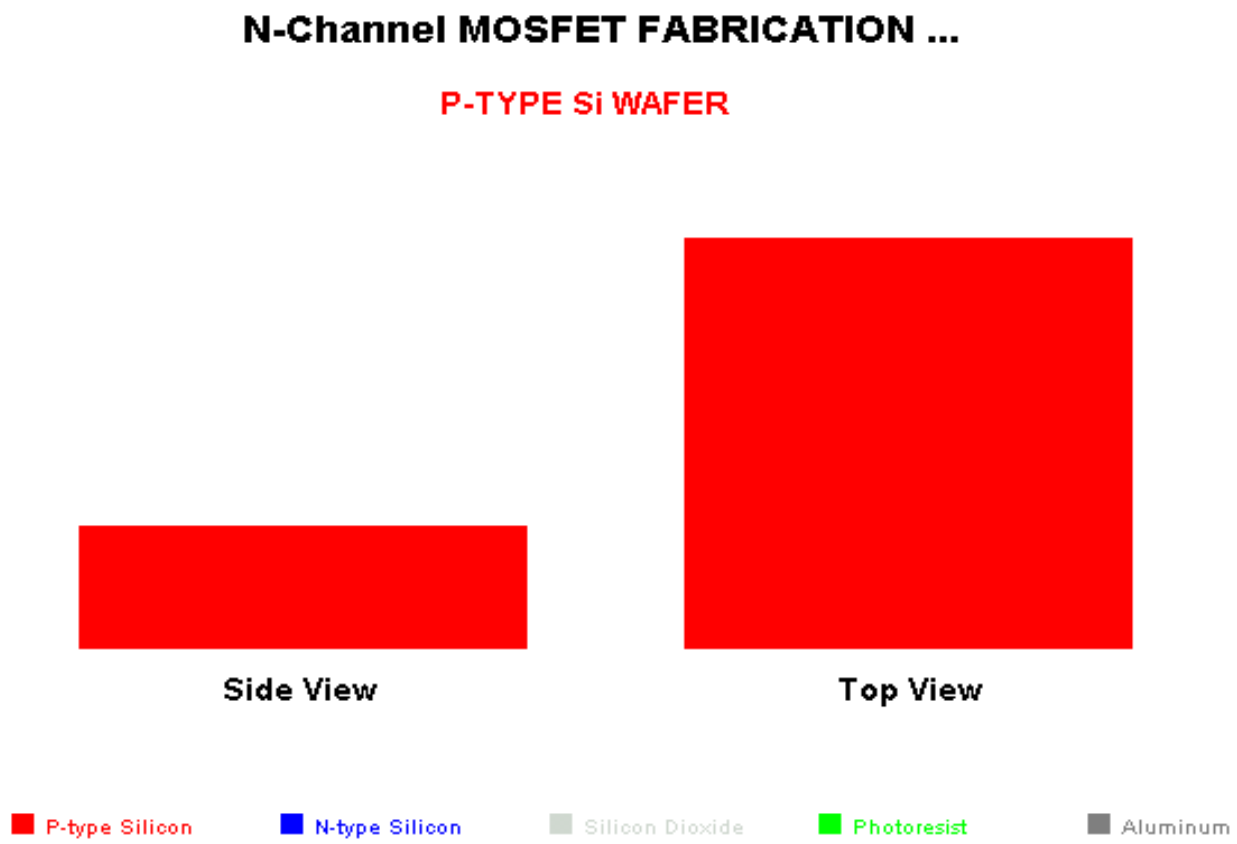
LECTURE-14

Transistor Fabrication

(Step by Step Process)

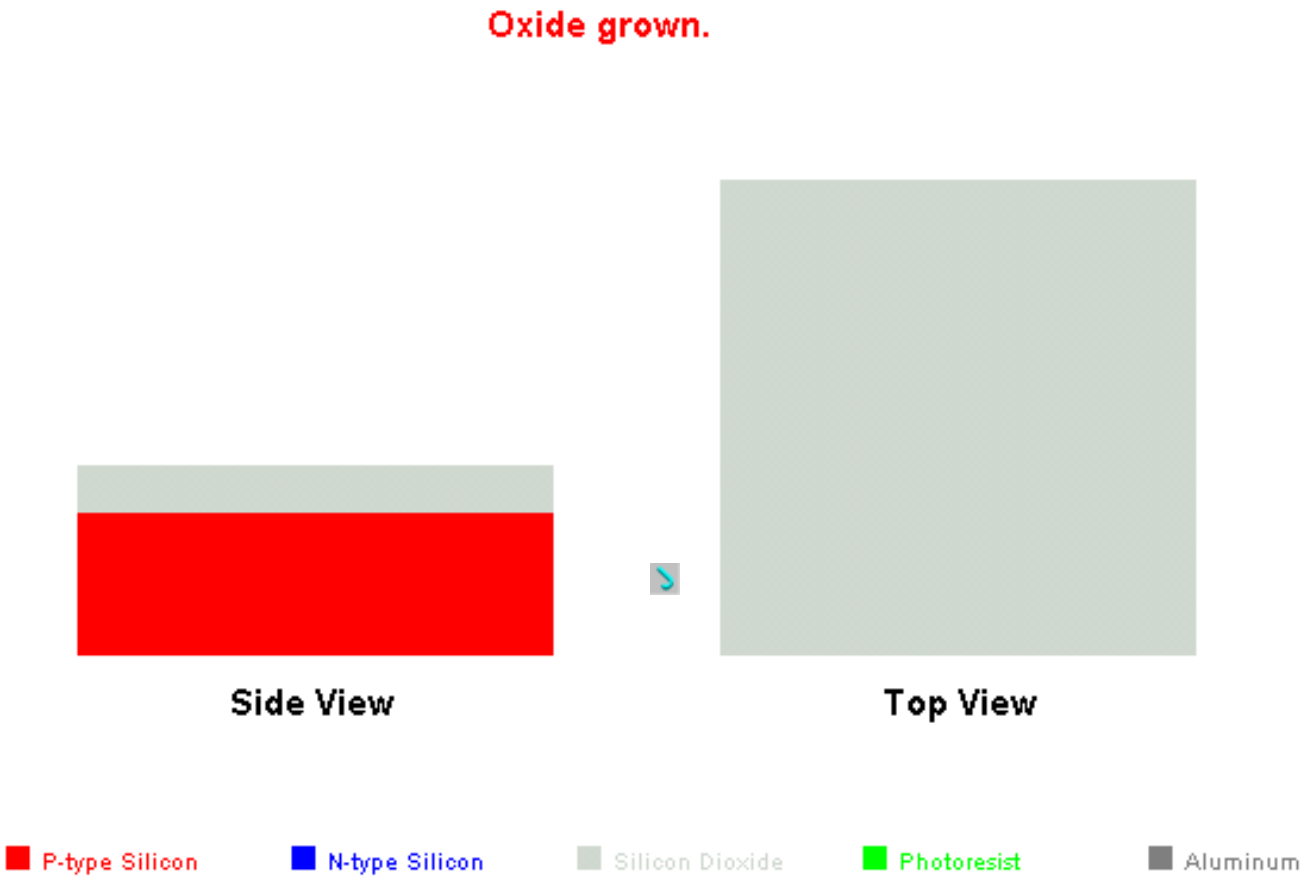
n-channel MOSFET Fabrication

The device fabrication steps are shown for n-channel Metal-Oxide-Semiconductor (MOS) Field Effect Transistor (FET). All photolithography processes are shown by means of animation. The steps shown here are the most detailed and serve as basis for the next few applets showing the device fabrication. A lightly doped p-type Si wafer



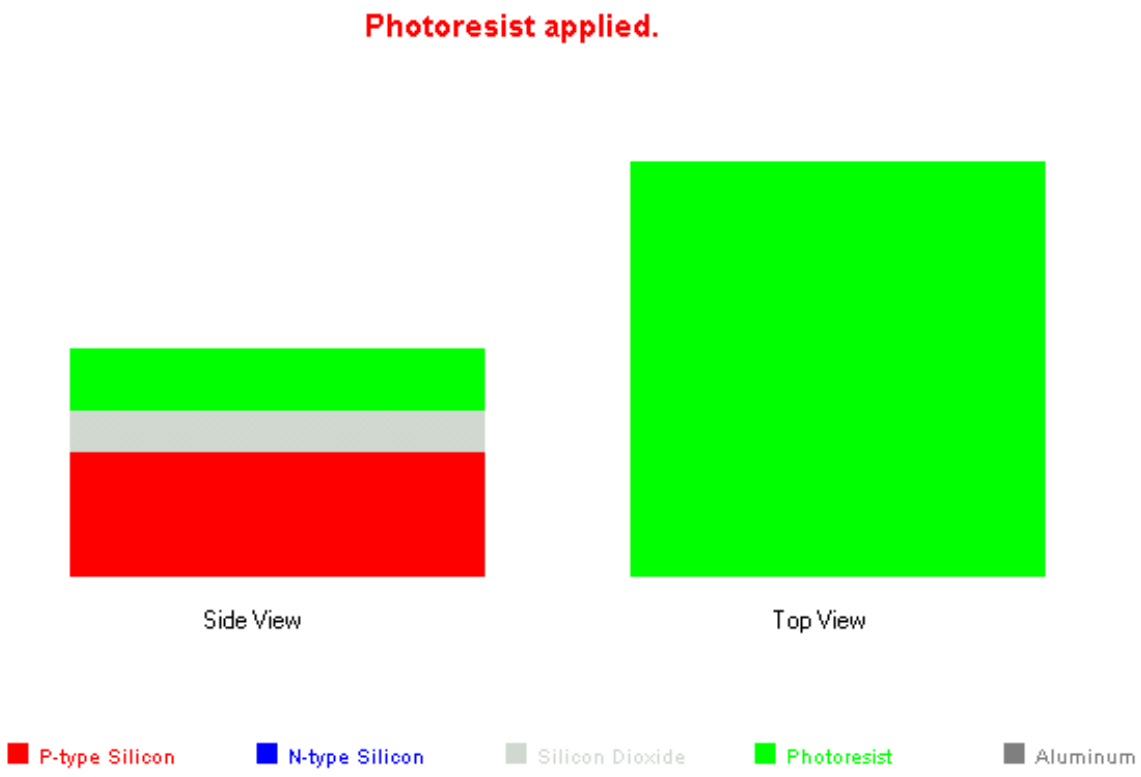
Oxide Grown

For NMOS process, the starting material is a P-type lightly doped, <100>-oriented, polished silicon wafer. The first step is to form the SiO2 layer(0.5 - 1um thick) by thermal oxidation. The oxidation temperature is generally in the range of 900 - 1200 degree C, and the typical gas flow rate is about 1cm/s.



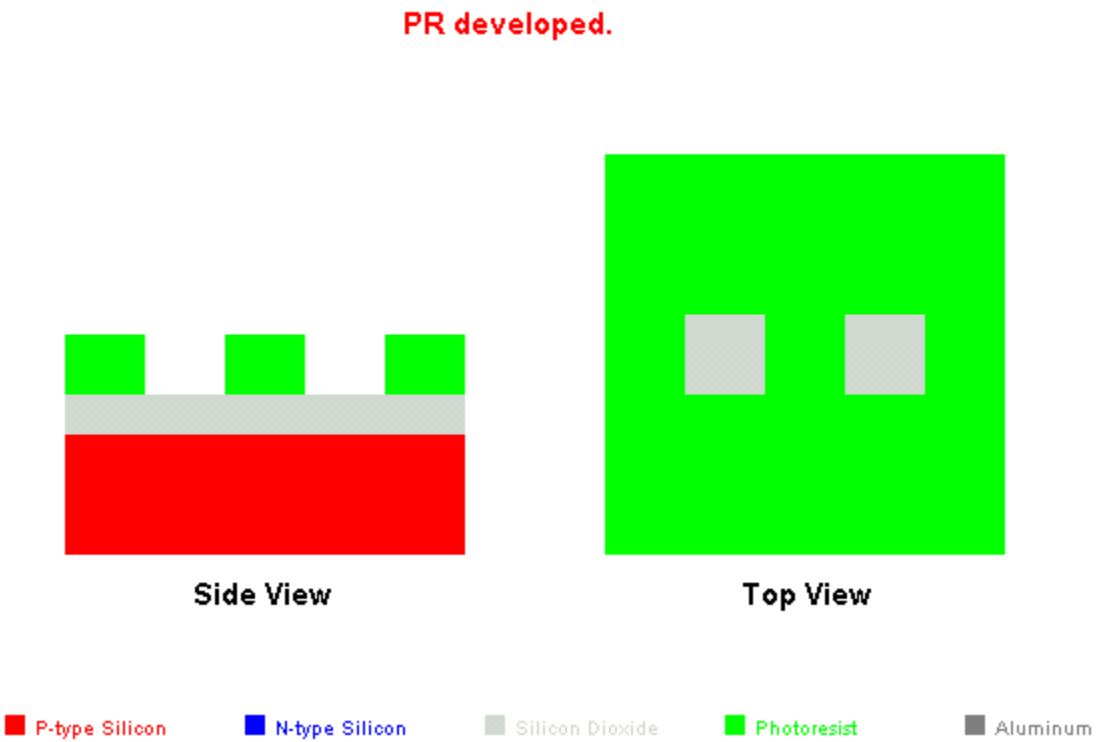
Photoresist Applied

Following oxidation, several drops of positive Photoresist(e.g. Shipley S1818) are dropped on the wafer. The wafer is spun at about 3000rpm to be uniformly spread out.After the spinning step, the wafer is given a pre-exposure baking (80 - 100 degree C) to remove the solvent from the PR film and improve adhesion to the substrate.



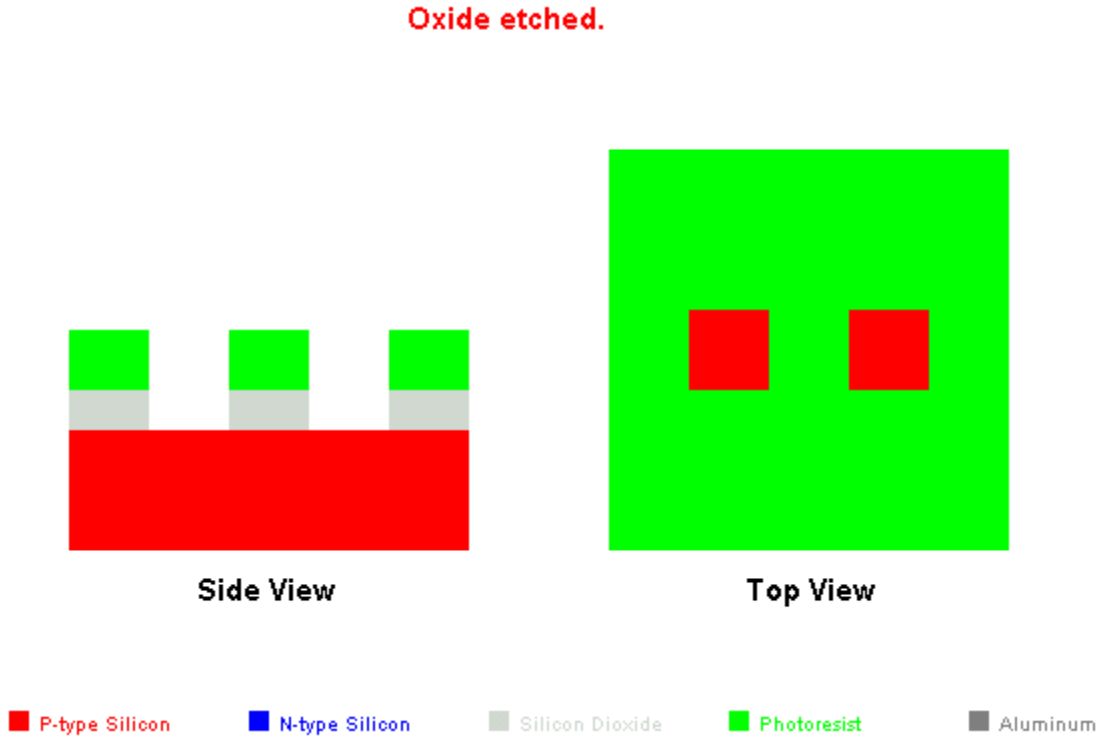
PR Developed

Third step is to define the active area (Drain and Source regions) by photolithography. The PR layer not covered by the mask undergoes a chemical change by UV light and is removed by the spraying the wafer with the developing solution(e.g. Shipley MF319). The final remaining PR is a copy of the pattern on the mask. Finally,the wafer is rinsed and spin-dried, and then baked again so that the PR can resist the strong acid used to etch the exposed oxide layer.



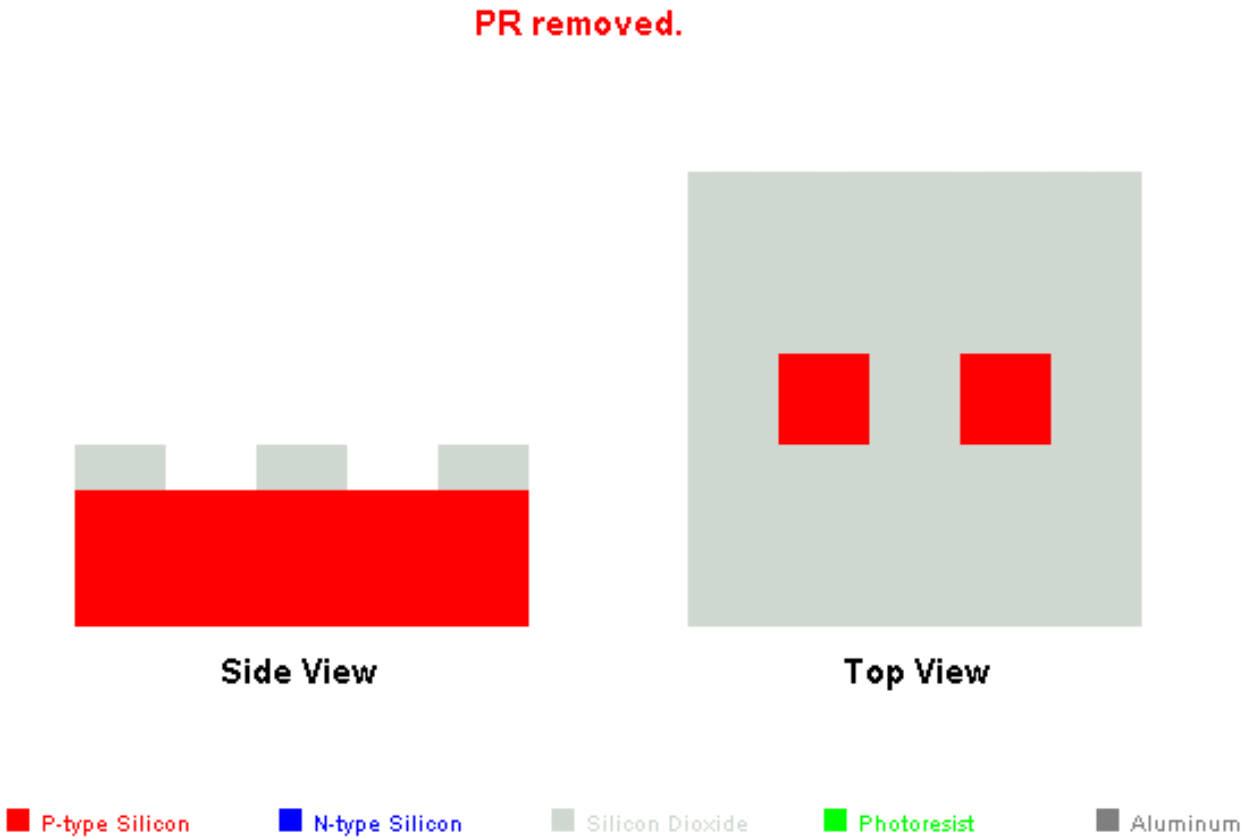
Oxide Etched

For SiO2 etching, HydroFluoric (HF) acid is usually used because it attacks oxide, but not silicon or PR. Therefore, the HydroFluoric(HF) acid etches away the oxide in the openings in the PR, and stops at the silicon surface.



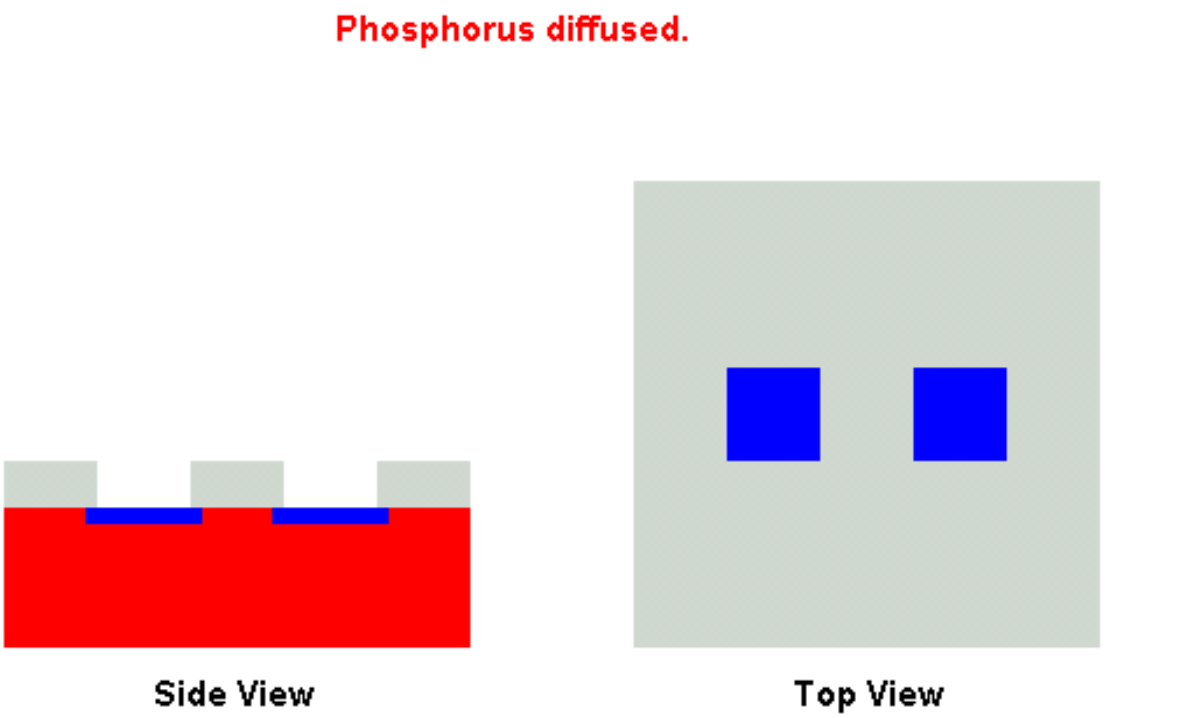
PR Removed

After SiO_2 etching, PR is stripped by using either a solvent (Aceton) or a plasma oxidation, leaving behind an insulator pattern that is the same as the opaque image on the mask.



Phosphorus Diffused

After stripping the PR,a two-step diffusion process is used to form drain and source regions, in which Phosphorus predeposition is first formed under a Constant-Surface-Concentration Condition(CSCC) and then is followed by a drive-in diffusion under a Constant-Total-Dopant Condition(CTDC). Finally, a thin layer of Phosphosilicate Glass on the wafer is removed by HF



Field Oxide Grown

After the forming the drain and source regions, additional oxide layer is grown from thermal oxidation as before. The Phosphorus spreads out by diffusion during this furnace operation, but the concentration are still much higher than that of the substrate doping.