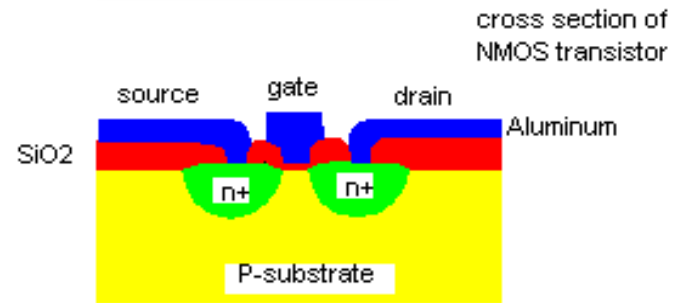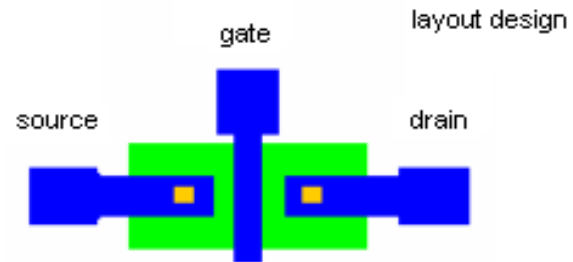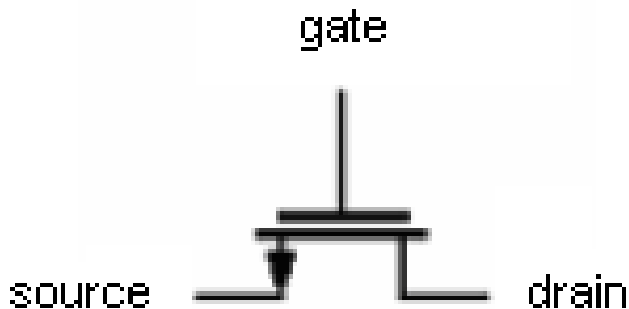# LECTURE-12

Circuit, layout and cross section of NMOS transistor

- In NMOS design, NMOS circuit is transferred to layout design.
- Then, mask can be design to fabricate NMOS transistor.

layout design

gate

source   drain

cross section of NMOS transistor

source   gate   drain

Aluminum

SiO2

n+   n+

P-substrate

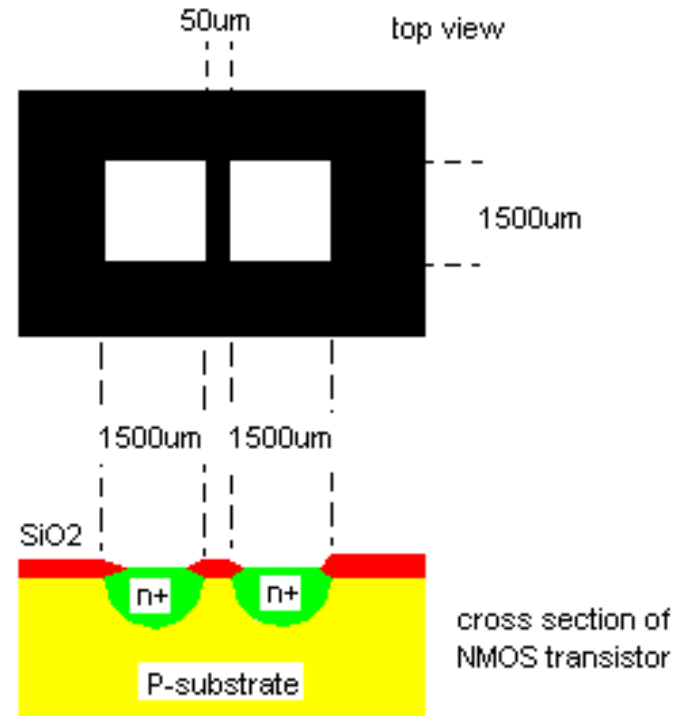NMOS circuit

gate

source   drain

■ mask   ▨ P-substrate
■ oxide silicon   ▨ source drain region
□ uncovered region

MASK 1: Source Drain Mask

- Mask 1 is used to control the heavily phosphorus doped and create the source and drain region of the n_channel device.

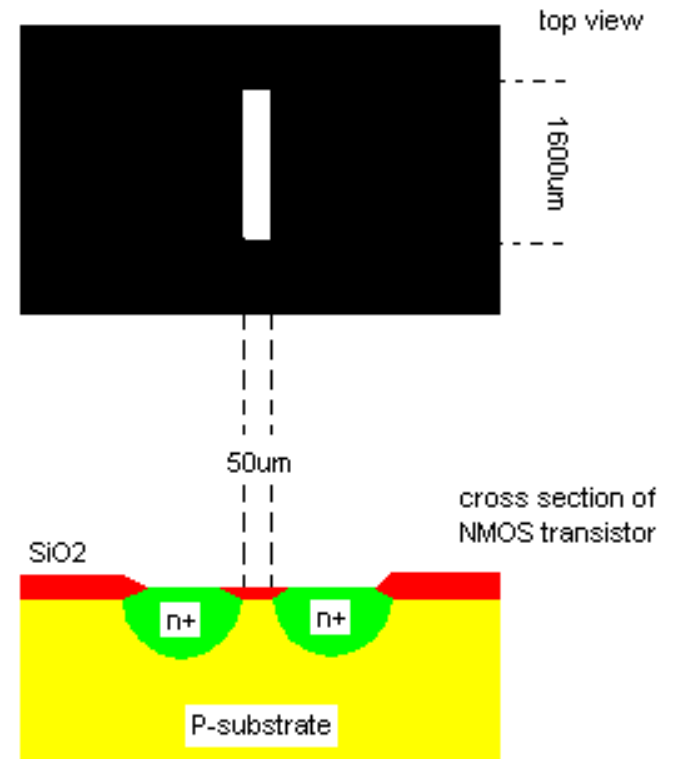**Layout 1: Source and Drain**

active region (source drain)

50um   top view

1500um

1500um   1500um

SiO2

n+   n+

P-substrate

cross section of NMOS transistor

■ mask   ■ P-substrate
■ oxide silicon   ■ source drain region
□ uncovered region

Mask 2: Gate Mask

- Mask 2 is used to remove the thick oxide layer and grow a very high quality of thin oxide.

Layout 2: Layout 1 and gate

top view

1600um

50um

cross section of NMOS transistor

SiO2

n+   n+

P-substrate

- █ active region (source drain)
- █ gate

- █ mask
- █ oxide silicon
- ☐ uncovered region

- █ P-substrate
- █ source drain region
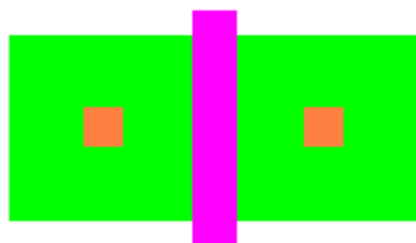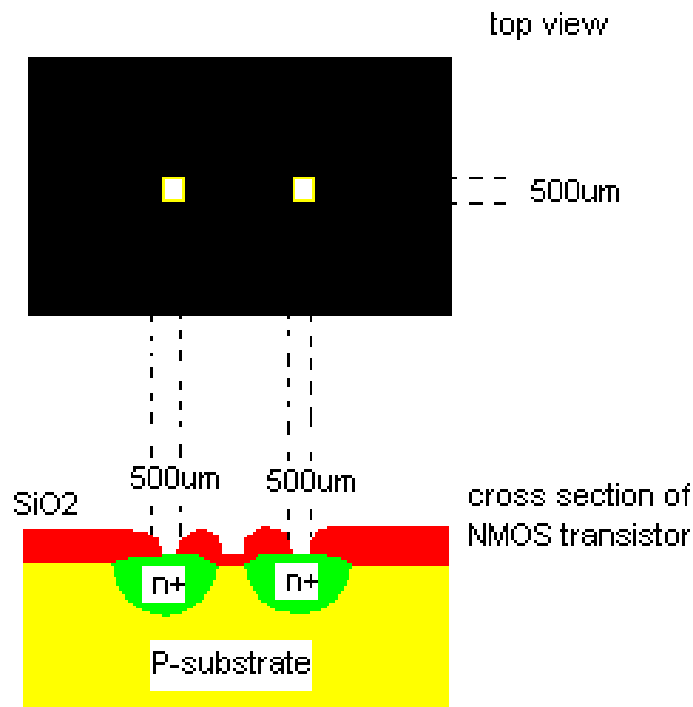
Mask 3: Contact mask

- Mask 3 is used to pattern the contact holes.

- Etching will open the holes.

Layout 3: Layout 2 and contact

active region (source drain)

gate

contact

top view

500um

500um   500um

SiO2   cross section of NMOS transistor

n+   n+

P-substrate

mask   P-substrate

oxide silicon   source drain region

uncovered region

Mask 4: Metallization Mask

- Mask 4 is used to pattern the connection.

- The uncovered Aluminum film will be removed during etching process.

Layout 4: Layout 3 and metallization

top view

700um

1000um

1000um

80um

cross section of NMOS transistor

gate

source   drain

Aluminum

SiO2

n+   n+

P-substrate

- ■ mask
- ■ oxide silicon
- ☐ uncovered region
- ■ P-substrate
- ■ source drain region

gate

source   drain

- ■ active region (source drain)
- ■ contact
- ■ Aluminum